

UNIVERSITY OF LONDON

BSc EXAMINATION 2004

For Internal Students of
Royal Holloway

DO NOT TURN OVER UNTIL TOLD TO BEGIN

CS2320A : COMPUTER ENGINEERING II
PAPER FOR RESIT CANDIDATES

Time Allowed: **TWO** hours

*Answer **FOUR** questions*

No credit will be given for attempting and further questions.

CS2320A

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Question 1

- a) Describe the main features of a *state transition diagram*. List two possible applications of state transition diagrams.
- [6 marks]
- b) A simple clothes washing machine operates as follows:
- The user depresses the “on” button. This causes the door to be locked.
 - The hot water valve is opened and the washing machine is filled with hot water until a level sensor detects it is at the correct level, when the hot water valve is then closed. The hot water travels via the powder compartment in order to mix the powder with the water.
 - If the water is not at the required temperature an internal heater is turned on until the temperature sensor detects the required temperature.
 - A timer is started with a value of 600 seconds and the washing drum is spun back and forth until the timer expires.
 - The timer is started with a value of 60 seconds and the water is drained by opening the drain valve. When the timer expires the drain valve is closed
 - The cold water valve is opened until the level sensor detects the correct level.
 - The timer is started with a value of 600 seconds and the washing machine drum is spun back and forth until the timer expires.
 - The timer is started with a value of 120 seconds and the drain valve is opened. When the timer expires the drain valve is closed and the door unlocked.
- Draw a state transition diagram for this washing machine.
- [10 marks]
- c) If we were to implement this state machine in digital logic how many inputs and outputs would be required?
- [6 marks]
- d) If the washing machine were fitted with an “emergency stop” button what actions should be taken if this button is pressed?
- [3 marks]

Question 2

- a) What instructions have explicitly been included in the MIPS instruction set to support the use of *procedures*? [4 marks]
- b) When a procedure is invoked in the MIPS processor certain registers are used in particular ways, according to compiler conventions. Describe the conventional use of the following sets of registers:
- \$a0 - \$a3
 - \$v0 - \$v1
 - \$t0 - \$t9
 - \$s0 - \$s7
- [8 marks]
- c) If there are a large number of arguments to the procedure then some of them will need to placed on the *stack*. Carefully explain the operation of a stack in the MIPS processor, showing what specific support for stack operations have been included in the MIPS processor.
- [10 marks]
- d) Why does the MIPS processor not implement a specific PUSH or POP instruction?
- [3 marks]

Question 3

- a) Boolean functions are often shown in the form of a *canonical sum-of-products*. Describe this form of representation and explain why is it a useful form?
[4 marks]
- b) Explain the following terms:
- i. minterm
 - ii. prime implicant
 - iii. non-essential prime implicant
- [6 marks]
- c) Describe the Quine-McCluskey minimisation algorithm and its relationship to Karnaugh Map graphical minimisation. Minimise the following function using both Karnaugh Map and Quine-McCluskey minimisation:
- $$f = (\bar{a} + b) \cdot (b + \bar{c}) \cdot (a + \bar{d}) \cdot (\bar{a} + c + \bar{d})$$
- [9 marks]
- d) What are the practical limitations on Karnaugh Map and Quine-McCluskey minimisation? Why is Quine-McCluskey minimisation particularly useful in Computer Aided Design systems for digital logic?
[6 marks]

Question 4

- a) What is the purpose of a *virtual memory system* and how does it differ from a cache memory system?
[5 marks]
- b) Describe the purpose and give examples of the operation of a *Translation Lookaside Buffer* in a virtual memory system.
[9 marks]
- c) The handling of *page faults* in a virtual memory system can be quite complex. List the steps involved in a typical page fault handling process.
[7 marks]
- d) Describe two algorithms that could be used to decide which page to replace when a page fault occurs.
[4 marks]

Question 5

- a) In what ways does a *superscalar* processor differ from a pipelined processor? What are the limitations of the superscalar approach?
[5 marks]
- b) Describe, using a diagram if required, the main components of a processor that uses *dynamic pipeline scheduling* to improve instruction throughput.
[9 marks]
- c) What features of typical program code and data make *caching* a viable approach to improving processor performance?
[4 marks]
- d) Describe the memory hierarchy, including indicative access times and implementation technology, of a typical personal computer.
[7 marks]

Question 6

- a) Why is it necessary to buffer control signals in a pipelined processor?
[3 marks]
- b) What is a *hazard* in a pipelined processor? Why do hazards not occur in a non-pipelined processor?
[4 marks]
- c) How can a *data hazard* be detected in a pipelined processor? Describe two approaches to resolving this type of hazard.
[12 marks]
- d) Explain how a *2 bit prediction scheme* can be used for branch prediction. Why is this better than a single bit prediction scheme?
[6 marks]