UNIVERSITY OF LONDON

BSc EXAMINATION 2004

For Internal Students of
Royal Holloway

DO NOT TURN OVER UNTIL TOLD TO BEGIN

CS2320B : COMPUTER ENGINEERING II

Time Allowed: **TWO** hours

*Answer **FOUR** questions*

No credit will be given for attempting and further questions.

CS2320B

Question 1

a) The designers of the MIPS processor instruction set decided to make all instructions 32 bits long, and for each instruction to conform to one of only three different formats. Describe five of the advantages of this design decision and one disadvantage.

[12 marks]

b) Describe the following two addressing modes of the MIPS processor by giving detailed examples showing the contents of registers before and after an example operation using that addressing mode.

i) Immediate

ii) Base + Index

[8 marks]

c) The MIPS processor implementation includes a *main datapath control* component which receives as input the 6 bits of the *opcode* in the instruction. Explain the purpose of this unit and give some examples of the outputs it produces and their purpose.

[5 marks]

Question 2

A major road aligned is aligned east / west. It meets a second major road coming from the south at a "T" junction. Traffic drives on the left hand side of the road. The junction is to be controlled by traffic lights which will let traffic flow in the following sequence of directions:

- Traffic flows from the east may flow to the west, and may also turn left onto the southerly direction. At the same time traffic may flow from west to east. Traffic wishing to travel from the west turning right onto the southerly direction is held in a filter lane.
- Traffic in the filter lane may now turn right and head south. At the same time, north facing traffic may also turn left to head west.
- North facing traffic may turn left or right to travel west or east
- (the sequence repeats)

a) Draw a state transition diagram for the traffic lights, including the correct sequencing of traffic lights (red → red / amber → green → amber)

[15 marks]

b) What is the minimum of outputs that the system will require?

[3 marks]

c) Explain what changes would be required to provide pedestrian controlled crossings across both roads.

[7 marks]

Question 3

a) What is the *canonical sum-of-products* form of a Boolean equation. Why is it a useful representation for such functions?

[4 marks]

b) Explain the following terms:

i. minterm
ii. essential prime implicant
iii. redundant prime implicant

[6 marks]

c) Describe the Quine-McCluskey minimisation algorithm and its relationship to Karnaugh Map graphical minisation. Minimise the following function using both Karnaugh Map and Quine-McCluskey minisation:

$$f = (a + \overline{b}) \cdot (b + \overline{c}) \cdot (a + \overline{d}) \cdot (\overline{a} + c + \overline{d})$$

[9 marks]

d) Describe how Quine-McCluskey minimisation is used in Computer Aided Design of complex programmable logic devices. Why are Karnaugh maps not used for this purpose?

[6 marks]

Question 4

a) *Interrupts* or *Exceptions* can be complicated to handle in a pipelined processor. Explain why this is so. What options are there for handling exceptions caused by a specific instruction and exceptions from external events such as interrupt from an external I/O device?

[7 marks]

b) Pipelining a processor increases *throughput* it does not reduce *execution time*. Explain why this is so. A longer pipeline has more potential for increasing throughput, however more problems arise. What are the problems that come from using ever longer processor pipelines?

[6 marks]

c) Define the following terms related to *cache memory systems:*

i. Cache Hit
ii. Hit Time
iii. Miss Penalty

[6 marks]

d) Describe, using a diagram if required, how a *direct mapped cache* is implemented.

[6 marks]

Question 5

a) Describe the architecture of a *Programmable Logic Array* (PLA). How does this differ from a *Programmable Array Logic* (PAL) device?

[7 marks]

b) Draw a diagram to show how a PAL can be used to implement a state machine. What are the advantages of using a PAL rather than a ROM?

[8 marks]

c) *Field Programmable Gate Arrays* FPGA are made up of the following components:

- I/O Blocks
- Logic Blocks
- Interconnection switches

Describe the purpose of each component and draw a diagram to show how these components are arranged in a typical FPGA. Describe some of the applications of FPGAs.

[10 marks]

Question 6

a) A single cycle processor can be implemented quite simply using digital logic. What is the main problem with this approach? What compromises must be made when implementing a *multi-cycle* approach to processor design?

[10 marks]

b) A multi-cycle processor design can be further extended to implement a pipelined datapath. Draw a block diagram of such a datapath and describe its operation.

[10 marks]

c) A pipelined implementation exhibits problems known as *hazards*. Describe *control hazards* and explain why the MIPS *branch delay slot* partly addresses this type of hazard.

[5 marks]