# Consensus Form

Date: 3/11/2020

Members Present: Felicia F
Jacques C
Segev Adler
Siddhanta Barola
Karn Watcharasupat

**Time meeting began:** 4:30 pm

**Time meeting ended:** 6:05 pm

◈ *This form is to be completed after each group meeting (both in and out of lab). Therefore, each group should complete a minimum of two consensus forms per week.*

**You may use the back of this form if additional space is needed.**

**Today We Discussed:**
(Describe the main topics discussed, worked on, or completed during the meeting.)

- settle admin matters
- summarized tasks
- planning our approach
- create read_cycle & write_cycle
  1) set CTRL to READ ($\overline{WE} \leftarrow$ '1', $\overline{CE} \leftarrow$ '0')
     set Addr
     NUM ADDR
     5 11
     upside
  2) read_cycle
  3) write_cycle

IO_CYCLE & Addr

000: R00 4. W00
001: R01 5. W01
010: R10 6. W10
011: R11 7. W11

8 - F

LOAD addr-low
OUT SRAM_( )
I/O DATA
down to be decoded

IO_ADDR → decoder
SRAM_CTRL SRAM_ADDR
$\overline{WE}$ $\overline{CE}$
1 0
all = scomp_CLK, IO_DATA, IO_WRITE
in to SRAM

EQU SRAM_READ 011
CLOCK @ 50 MHz
3 cycles ✓

AC ← data(addr-low) → OUT SRAM_READ → IO_ADDR ← SRAM_READ

**Action Items:**
(List the tasks being worked on for the next meeting. In parenthesis next to each action item, write the name of the team member responsible for completing the task)

◈ IO_DECODER = Felicia & Segev

◈ SRAM_READ = Jacques & Siddhanta
+ UML

◈ SRAM_skeleton = Karn

◈

# Consensus Form

**Date:** 03/10/20

**Time meeting began:** 6:15 pm

**Time meeting ended:** 7:45 pm

**Members Present:** Felicia E
Karn Watcharasupat
Segev Aptek
Jacques G
Siddhanta Panda

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**Today We Discussed:**
(Describe the main topics discussed, worked on, or completed during the meeting.)

- Created group
- Completed lab exercise to familiarize ourselves with the SRAM and SCOMP (modified)
- Established first external meeting, 03/11/20, to discuss implementation, deadlines, divide work, and to try working on the VHDL & asm code.
- Current ideas
  - SRAM interface with SCOMP → aim to skip the decoder if possible and implement assembly I/O directly to SRAM
  - bulk of work will likely be in VHDL or asm
    - hold execute for longer
    - how to control read vs write?

**Action Items:**
(List the tasks being worked on for the next meeting. In parenthesis next to each action item, write the name of the team member responsible for completing the task)

◈ Devise a set method of approach / proposal for the project - All members

◈ Determine meeting days and deadlines - All members

◈ Divide work / create shared folders / git project / methods of communication - All members

◈ Begin code portion of project - All members

# Consensus Form

Date: 17 Mar 2020

Members Present: Karn Watcharasupat, Felicia E, Siddhanta Panda, Segev Apter

**Time meeting began:** 18:00 EDT

**Time meeting ended:** 20:30 EDT

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**Today We Discussed:**
(Describe the main topics discussed, worked on, or completed during the meeting.)

- Review of previous week's work on IO_DECODER and read cycle for SRAM
- Address allocation for IO_DECODER
- Added tristate bus to SRAM controller
- Write cycle timing, states, and assembly instructions
- Delegate work for write cycle

**Action Items:**
(List the tasks being worked on for the next meeting. In parenthesis next to each action item, write the name of the team member responsible for completing the task)

◈ IO_DECODER control signal and address allocation in VHDL (Karn)

◈ Write cycle UML and synchronization diagram (Felicia & Segev)

◈ Add write cycle to SRAM Controller VHDL (Siddhanta & Jacques)

◈

# Consensus Form

Date: 04/01/2020

Members Present: Siddhanta Panda, Felicia E, Karn Watcharasupat, Jacques Crawford, Segev Apter

**Time meeting began:** 18:00

**Time meeting ended:** 20:00

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**Today We Discussed:**

(Describe the main topics discussed, worked on, or completed during the meeting.)

## Proposal

Introduction
- -Problem statement
- -Requirements

Technical Approach
- -Assembly and User Interaction.
- -Read Cycle
- -Write Cycle

Project Timeline
- -Current progress
- -Future work
- -Contingency plan

-Minor fix to UML

-Assembly code for verification of read cycle

**Action Items:**

(List the tasks being worked on for the next meeting. In parenthesis next to each action item, write the name of the team member responsible for completing the task)

- Proposal slides: Introduction -Felicia
- Assembly and User interaction - Felicia and Karn Read Cycle - Siddhanta and Jacques
  Write Cycle - Siddhanta and Segev
- Minor fix to UML – Felicia
- Simulation