# Consensus Form

Date: 17 Mar 2020

Members Present: Karn Watcharasupat, Felicia E, Siddhanta Panda, Segev Apter

**Time meeting began:** 18:00 EDT

**Time meeting ended:** 20:30 EDT

◈ *This form is to be completed after each group meeting (both in and out of lab). Therefore, each group should complete a minimum of two consensus forms per week.*

**You may use the back of this form if additional space is needed.**

**Today We Discussed:**
(Describe the main topics discussed, worked on, or completed during the meeting.)

- Review of previous week's work on IO_DECODER and read cycle for SRAM
- Address allocation for IO_DECODER
- Added tristate bus to SRAM controller
- Write cycle timing, states, and assembly instructions
- Delegate work for write cycle

**Action Items:**
(List the tasks being worked on for the next meeting. In parenthesis next to each action item, write the name of the team member responsible for completing the task)

◈ IO_DECODER control signal and address allocation in VHDL (Karn)

◈ Write cycle UML and synchronization diagram (Felicia & Segev)

◈ Add write cycle to SRAM Controller VHDL (Siddhanta & Jacques)

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