Single-PORT SRAM
2048 WORDS X 8 BITS, MUX 8
SMIC .13um LL Process

Version v0p2

OVERVIEW

The Single-Port synchronous is designed for SMIC's 0.13um CMOS LL Process. The memory is optimized for speed, power and area. It operates at a voltage range of 1.35V to 1.65V and a temperature range of -40^{o} C to 125^{o}C.

The write enable (WEN), chip enable(CEN), address(A[n:0]) and data in (D[i:0]) signals are latched on the rising-edge of the clock(CLK). When CEN is low and WEN is high the menory will be in read oprarion. Through A[n:0] the data is read and output on the output port Q[i:0]. When CEN and WEN are both low the word on the data port D[i:0] will be written into the memory and then the data will appear on the output port Q[i:0].

When CEN is high the memory is in standby mode. Meanwhile, the data stored in memory is retained but cannot be read or written.

CONFIGURATION:

PARAMETER	VALUE
Mux	8
Words	2048
Bits	8
Width	182.34um
Height	559.045um
Area	101936.265um^2

PIN DEFINITION:

PIN	DIRECTION	DEFINITION
A[10:0]	Input	Address Inputs
D[7:0]	Input	Data Inputs
WEN	Input	Write Enable
CEN	Input	Chip Enable
CLK	Input	Clock Input
Q[7:0]	Output	Data Outputs

TIMING:

PARAMETER	DESCRIPTION	SS CORNER 1.35V, -40°C		SS CORNER 1.35V, 125°C		FF CORNER 1.65V, -40°C		FF CORNER 1.65V, 0°C		FF CORNER 1.65V, 125°C		TT CORNER 1.5V, 25°C	
(ns)		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Tcyc	Cycle Time	4.649		5.384		1.117		1.187		1.401		2.915	
Ta	Access Time[1]		3.576		4.141	0.859		0.913		1.078			2.242
Tas	Address Setup	0.669		0.717		0.246		0.257		0.290		0.489	
Tah	Address Hold	0.682		0.717		0.307		0.315		0.336		0.546	
Tds	Data Setup	0.498		0.610		0.224		0.244		0.302		0.453	
Tdh	Data Hold	0.380		0.318		0.143		0.134		0.107		0.301	
Tws	Write Enable Setup	0.150		0.150		0.042		0.042		0.043		0.173	
Twh	Write Enable Hold	0.748		0.803		0.324		0.334		0.362		0.583	
Tcs	Chip Enable Setup	0.214		0.235		0.103		0.103		0.124		0.150	
Tch	Chip Enable Hold	0.000		0.000		0.000		0.000		0.000		0.000	
Tckh	Clock High	0.380		0.400		0.200		0.200		0.200		0.300	
Tckl	Clock Low	0.440		0.550		0.220		0.220		0.220		0.330	
Tckr	Clock Rise Skew	1.500		1.500		0.750		0.750		0.750		1.000	

Timing simulation conditions:

1. Access time = best case for fast corner and worst case for slow/typical corners

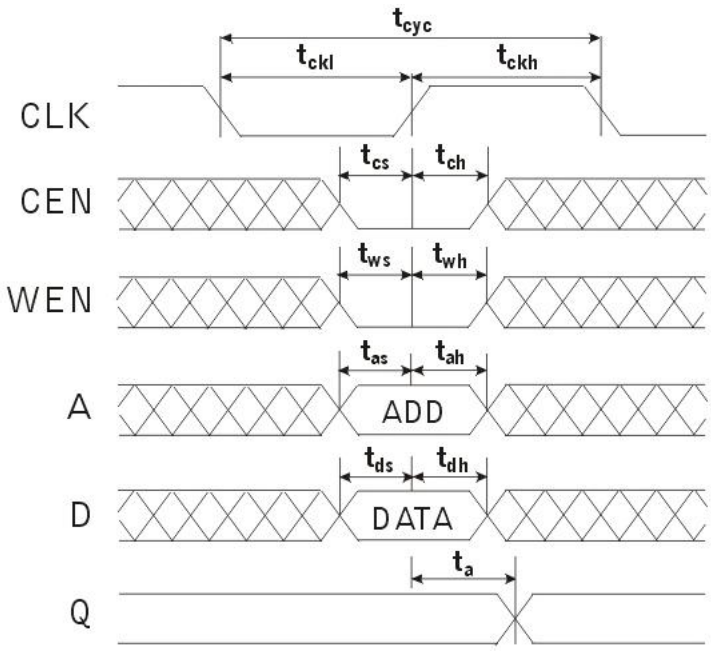
POWER:(UNITS=uA/Mhz)

PARAMETER	SS CORNER 1.35V, -40C	SS CORNER 1.35V, 125C	FF CORNER 1.65V, -40C	FF CORNER 1.65V, 0°C	FF CORNER 1.65V, 125°C	TT CORNER 1.5V, 25°C
AC Current	20.970	20.483	25.907	26.060	26.460	22.830
Read AC Current	19.039	18.438	23.091	23.118	23.516	20.438
Write AC Current	22.901	22.529	28.722	29.002	29.404	25.222
Standby Power (mW)	0.000255	0.002161	0.000400	0.000621	0.071058	0.000414

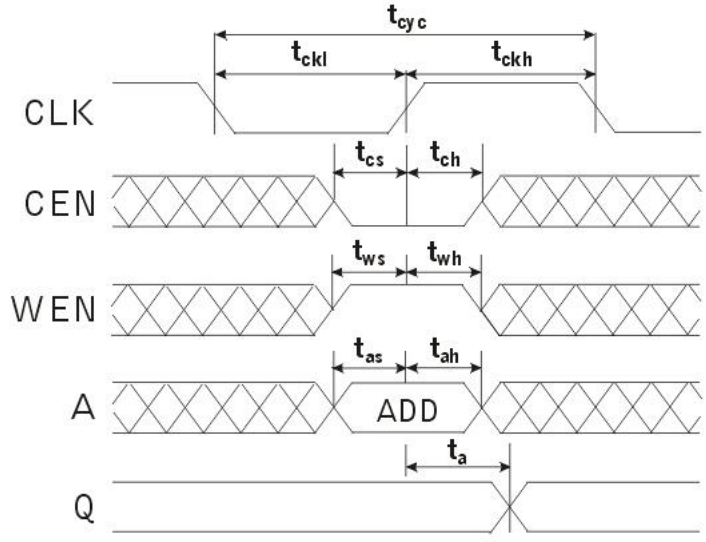
Power simulation conditions:

1. 50% read / 50% write operations, all addresses and 50% of input pins toggle at 1Mhz

WRITE CYCLE TIMING:



READ CYCLE TIMING:



Datasheet Revision History

Date	Version	Changes
	v0p2	

Semiconductor Manufacturing International Corporation
No. 18 Zhangjiang Road
Pudong New Area
Shanghai 201203
The People Republic of China
Email: Design_Service@smics.com
URL: www.smics.com