5

Power Conditioning

Power conditioning is required to interface the PV source circuit for power processing. The key functional blocks of a typical two-stage conversion system for AC grid interconnection is shown in Figure 5.1.

The PV link is the interface between the PV source circuit and the PV-side converter (PVSC). It provides a filtering function to maintain a steady voltage at the link. The PVSC is a DC/DC power interface, the input of which is coupled to the PV link and is usually controlled by the maximum power point tracking (MPPT) algorithm so that maximum energy harvesting is achieved. Throughout the book, it is occasionally referred to the "PV-side power interface." The grid link is the interface between the grid and the grid-side converter (GSC). It provides a filtering function to guarantee the power quality required by the grid. A transformer can be implemented at this stage for the purpose of galvanic isolation and voltage conversion. The GSC is the power interface between the DC link and the AC grid link. It converts DC to AC for grid interconnection. The DC link is commonly formed by capacitors, which maintain a steady DC-link voltage between the two conversion stages.

In systems with single-stage conversion, one centralized power converter is used, as shown in Figure 5.2. Thanks to the simplicity of its configuration, the system gives higher efficiency and lower costs than a two-stage-conversion system. To avoid confusion, the DC/AC converter for single-stage conversion is considered the GSC. The PV link is merged with the DC link, as shown in Figure 5.2. The design and analysis of the GSC in single-stage conversion systems is generally the same as in two-stage conversion systems.

Shown in Figure 1.16 and described in Section 1.11, a DC microgrid is composed of the power interfaces for energy storage units. Bidirectional DC/DC converters are usually required to interface batteries with a DC bus. Therefore, one section in this chapter is about the battery-side converters (BSCs) that are required for the charge and discharge operations of battery storage units.

The inductance and capacitance parameters in the following design examples are theoretically sized and based on the ideal converter system. They are considered as minimal values for proof of concept and simulation. They are also the reference and the starting point for practical designs in which all constraints are considered. When all the parameters are re-tuned to meet all requirements, they can be again used for simulation to prove the upgraded design concept. The modeling and simulations in this chapter are based on the basic functions of Simulink rather than circuit-based modeling methods, such as Simscape Power Systems.

Photovoltaic Power System: Modeling, Design, and Control, First Edition. Weidong Xiao.

Companion Website: www.wiley.com/go/xiao/pvpower

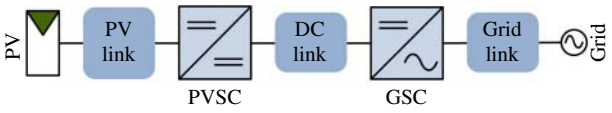

Figure 5.1 Block diagram of a grid-connected PV system with two-stage power conversion. PVSC, PV-side converter; GSC, grid-side converter.

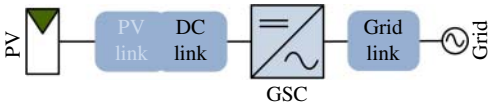

Figure 5.2 Block diagram of grid-connected PV system with single-stage power conversion. GSC, grid-side converter.

5.1 PV-side Converters

The PVSC is the DC/DC power-conditioning circuit, the input of which is connected to the PV link. In standalone systems, the PVSC can be used as the power interface to charge batteries or supply power to local loads. The common DC/DC topologies used for PVSCs can include buck, boost, buck–boost, flyback, tapped-inductor, and full-bridge isolated DC/DC converters. It is important to design a topology that gives maximum power yield, without increasing the circuit complexity. Figure 5.3 illustrates the procedure that is recommended to design, simulate, and evaluate the PVSC in order

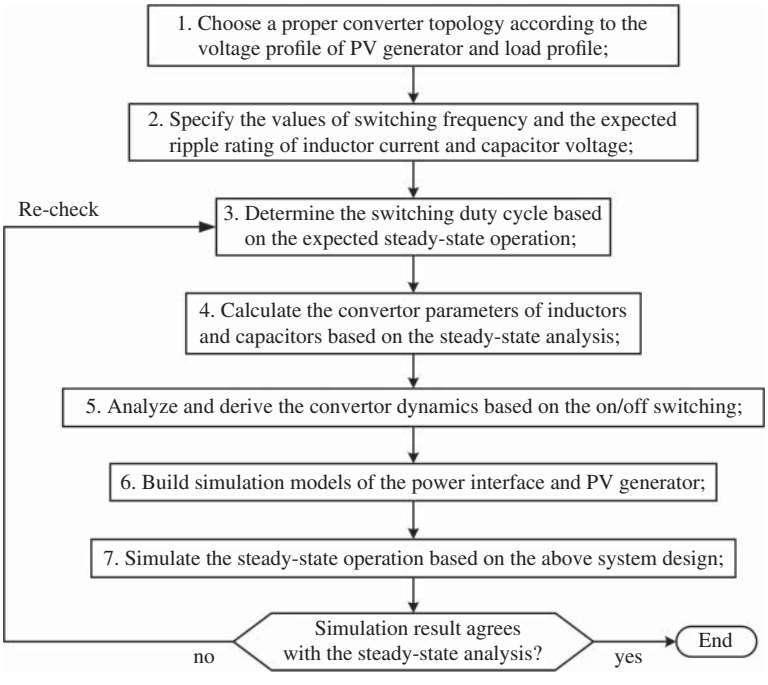

Figure 5.3 Recommended procedure to design, simulate, and evaluate PV-side power interface.

to meet the system specification and give the correct performance rating. The procedure follows the sequence of

- topology selection
- specification
- steady-state analysis
- design
- simulation modeling
- simulation evaluation.

Simulation is an effective tool and widely used to prove the design concepts of PVSCs and the effectiveness of models.

5.1.1 PV Module for Case Study

In the following study, one specific PV module is used to demonstrate PVSC design and simulation. Its electrical characteristics at STC are shown in Figure 5.4. The PV module is constructed from 72 multi-crystalline cells and is used for demonstration purposes only. The simulation model is based on the ISDM that is introduced in Section 4.1. The short-circuit current and open-circuit voltage are 8.34 A and 44.17 V respectively. The maximum power point (MPP) is at (37.0 V, 7.79 A). The peak power is 288.3 W, as indicated in the plot.

5.1.2 Buck Converter

A buck converter circuit, as shown in Figure 5.5, can be used for the PVSC. The converter is controlled by pulse width modulation (PWM), of which the switching duty cycle is the control-input variable. A step-down topology should be considered if the converter-output voltage is never higher than the PV terminal voltage (v_{pv}) at the MPP, V_{MPP}, when the normal voltage variation of both sides has been considered. The condition can be expressed as: $V_{O(max)} \leq V_{MPP(min)}$. The lowest value of the PV terminal voltage at the MPP, $V_{MPP(min)}$, can be estimated from the highest ambient temperature

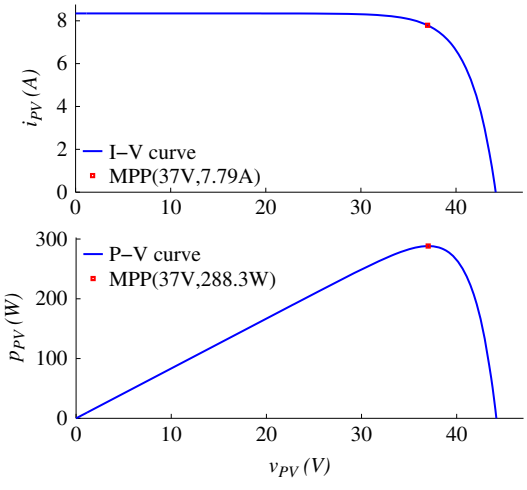

Figure 5.4 I–V and P–V curves of PV module output.

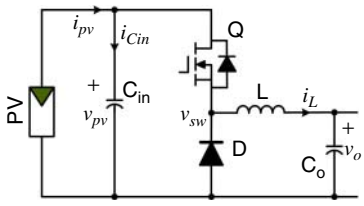

Figure 5.5 Buck converter used for PV power interface.

and the minimum irradiance for the converter to operate. The highest value of the output voltage, $V_{O(max)}$, can be determined from the load profile. For battery-charging applications, the battery voltage becomes the converter-output voltage, v_o, which varies from the cut-off voltage at 0% state of charge (SOC) to the highest level: the open-circuit voltage at 100% SOC. In this case, the value of $V_{O(max)}$ is equivalent to the open-circuit voltage of the battery at 100% SOC.

One additional concern of the buck topology is that the input current is always pulsing or "chopped," so significant input capacitance is required to smooth the PV-link voltage. This generally affects the dynamics of the PV-link voltage and causes significant ripple in the capacitor current, i_{Cin}. The output current is smooth in the buck topology because the inductor appears on the output side.

At STC and the predefined switching frequency, f_{sw}, the inductor ripple current and ripple voltage at the PV link should be specified by the peak-to-peak values, ΔI_L and ΔV_{PV}, respectively. Steady-state analysis can determine the duty cycle at the nominal load operating condition. At STC, the PV source circuit should be operated at the MPP, which is represented by V_{MPP} and I_{MPP}. The duty cycle can be calculated from:

$$D_o = \frac{V_{O-NOM}}{V_{MPP}} \tag{5.1}$$

with the assumption that the converter is operated in continuous conduction mode (CCM). The symbol V_{O-NOM} represents the nominal output voltage, which can be specified from the load profile. The value of the inductance, L, and the capacitance, C_{in}, can be calculated from (5.2) and (5.3), respectively.

$$L = \frac{V_{O-NOM}(1 - D_o)}{\Delta I_L f_{sw}} \tag{5.2}$$

$$C_{in} = \frac{I_{MPP}(1 - D_o)}{\Delta V_{PV} f_{sw}} \tag{5.3}$$

In this system, the capacitor C_{in} represents the PV link between the PV source circuit and the PVSC.

It should be noted that the thermal characteristics should be evaluated and considered for capacitor selection. Significant current ripple can be expected for filtering the pulsing current at the input side of the buck converter. Each capacitor is constrained by the allowable ripple current. The intrinsic equivalent series resistance (ESR) results in power loss when significant ripple current is conducted. High temperature is related to the early failure of capacitors. To evaluate the power loss and estimate the core temperature, the RMS value of the ripple current in i_{Cin} should be determined (see discussion in Section 5.6). In general, thermal analysis is considered as one of the most important aspects of the selection of capacitors and the design of power electronics.

When switch Q is "on," the system dynamics can be represented as in (5.4) and (5.5).

$$i_L = \frac{1}{L}\int (v_{pv} - v_o)dt \tag{5.4}$$

$$v_{pv} = \frac{1}{C_{in}}\int (i_{pv} - i_L)dt \tag{5.5}$$

When Q is "off," the system dynamics are as in (5.6) and (5.7).

$$i_L = \frac{1}{L}\int (-v_o)dt \tag{5.6}$$

$$v_{pv} = \frac{1}{C_{in}}\int i_{pv}dt \tag{5.7}$$

From the on/off states and the integral operation, a simulation model can be built by Simulink, as shown in Figure 5.6a. The model is based on the ideal buck converter, in which loss is not considered. Two single-pole–double-throw (SPDT) switches are utilized in the Simulink model for the switching between the on-state, (5.4) and (5.5), and the off-state, (5.6) and (5.7). The model includes three inputs:

- the pulse width modulation (PWM) command signal for the switches
- the output voltage determined by the load condition (v_o)
- the PV output current (i_{pv}).

It outputs two signals: the inductor current (i_L) and the PV-link voltage (v_{pv}). The dynamic interaction is simulated by the integral operation, which is defined by (5.4)–(5.7). The saturation signs are shown in the Simulink blocks for integration, which constrains the inductor current (i_L) and the PV-link voltage (v_{pv}) to be always positive. All components can be packed together to form a single block to represent the buck converter, as shown in Figure 5.6b. The correspondence of the PV-link voltage (v_{pv})

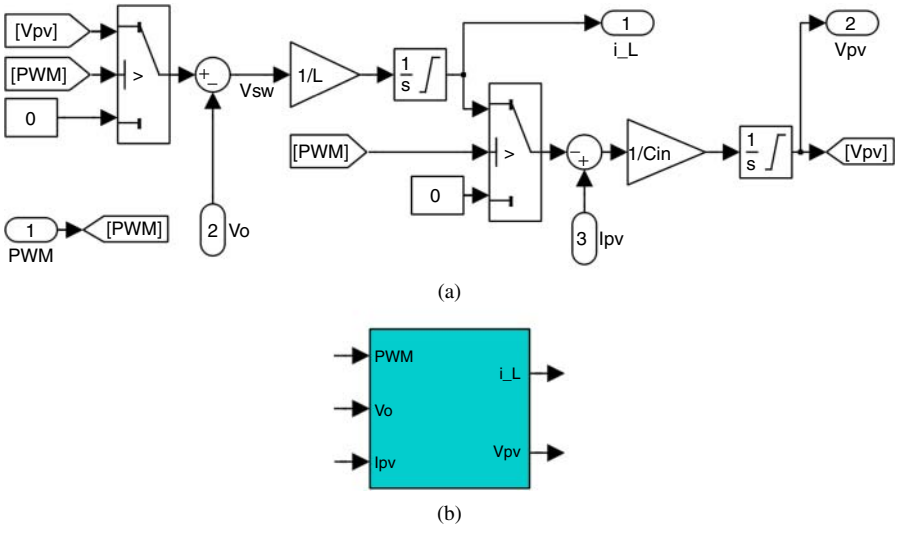

Figure 5.6 Simulink model of buck converter used for PV power interface: (a) model composition; (b) integrated block.

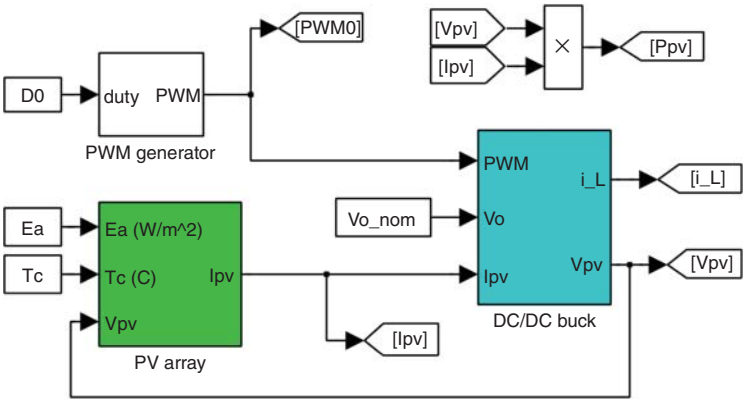

Figure 5.7 Simulink system using the buck converter for PV-side converter.

and the PV output current (i_{pv}) should follow the PV source circuit model discussed in Chapter 4 and shown in Figure 4.25. The steady-state analysis and design can be simulated and verified using the Simulink model.

An example is given of charging a battery module with a nominal voltage of 24 V. The open-circuit voltage is 28 V when the battery module is fully charged. The power source is the PV module that was introduced in Section 5.1.1. Since the V_{MPP} is significantly higher than 28 V, a buck converter is selected for the power conditioning. The switching frequency is designed to be 50 kHz; the peak-to-peak ripple voltage of the PV module is specified as 0.2 V; and the peak-to-peak ripple of the inductor current is specified as 1 A. Based on the nominal battery voltage (24 V) and the STC of the PV module, the nominal duty cycle of the PWM can be calculated as 64.9% according to (5.1). Then the values of L and C_{in} can be calculated as 167 µH and 272 µF, by following (5.2) and (5.3), respectively. The system simulation model, as shown in Figure 5.7, is constructed together with the blocks of the PV module and the PWM generator.

The simulation result is shown in Figure 5.8, including the waveforms of i_L, v_{pv}, i_{pv}, and p_{pv}. When PWM signals are applied to the converter with its nominal duty cycle of 64.9%, the value of v_{pv} drops from the open-circuit voltage, 44.17 V, to the value of V_{MPP}, which is 37.0 V at the steady state. The signal of i_{pv} increases from zero to the value of I_{MPP}, which is 7.79 A at the steady state. The PV power (p_{pv}) reaches the value of the MPP with the corresponding voltage and current, the same as the rating shown in Figure 5.8.

Figure 5.9 provides a zoom-in look at the waveform that was presented in Figure 5.8. The peak-to-peak ripple of the inductor current is measured as 1 A, corresponding to the specification. The peak-to-peak ripple of the PV-link voltage is also measured to match the specified value of 0.2 V. The fixed step-size of the numerical solver is chosen as 20 ns, which indicates that the simulation resolution is 1000 sampling points in each PWM switching cycle. The MPP is 288.3 W, the same as the PV module specification. The simulation verifies the system design and demonstrates the model's performance in the steady state. The same sizing and design principles can be applied to cases with different electrical ratings from the example.

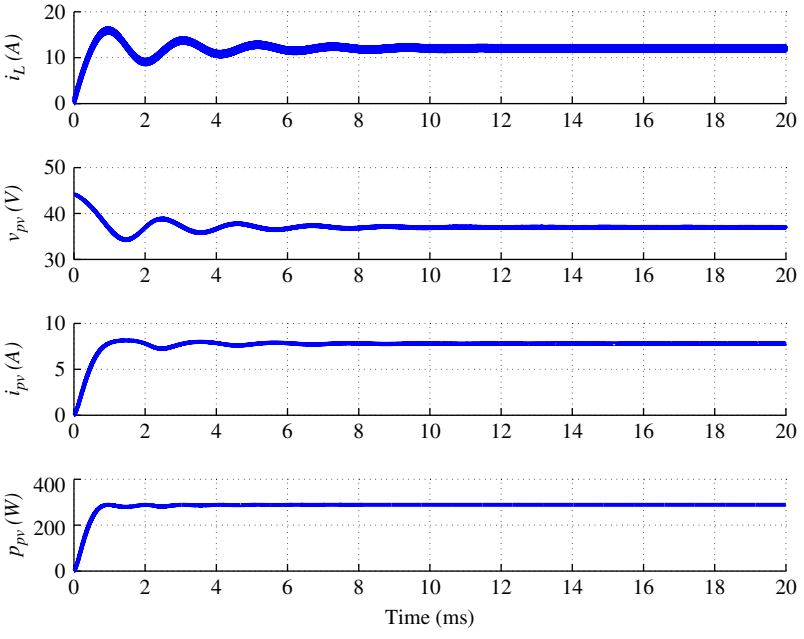

Figure 5.8 Simulated waveforms of the PV power charger in the steady state.

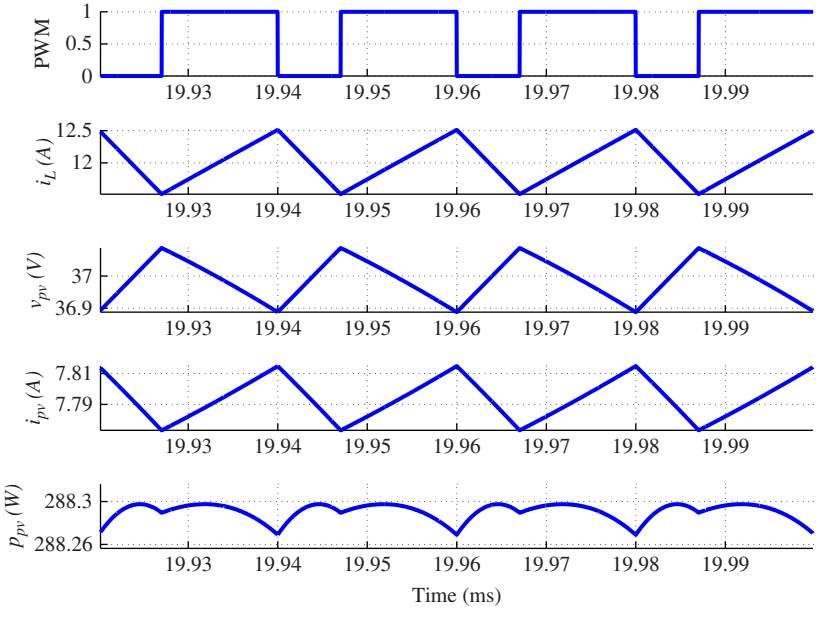

Figure 5.9 Simulated waveforms of the PV power charger in the steady state.