Embedded Software Essentials

Development Kits and Documentation

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Silicon Manufacturers

Microcontroller chips are a type of

Integrated Circuit (IC) --or--

Application-Specific Integrated Circuit (ASIC)

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MSP432p401r ARM Cortex-M4 ASIC[2]

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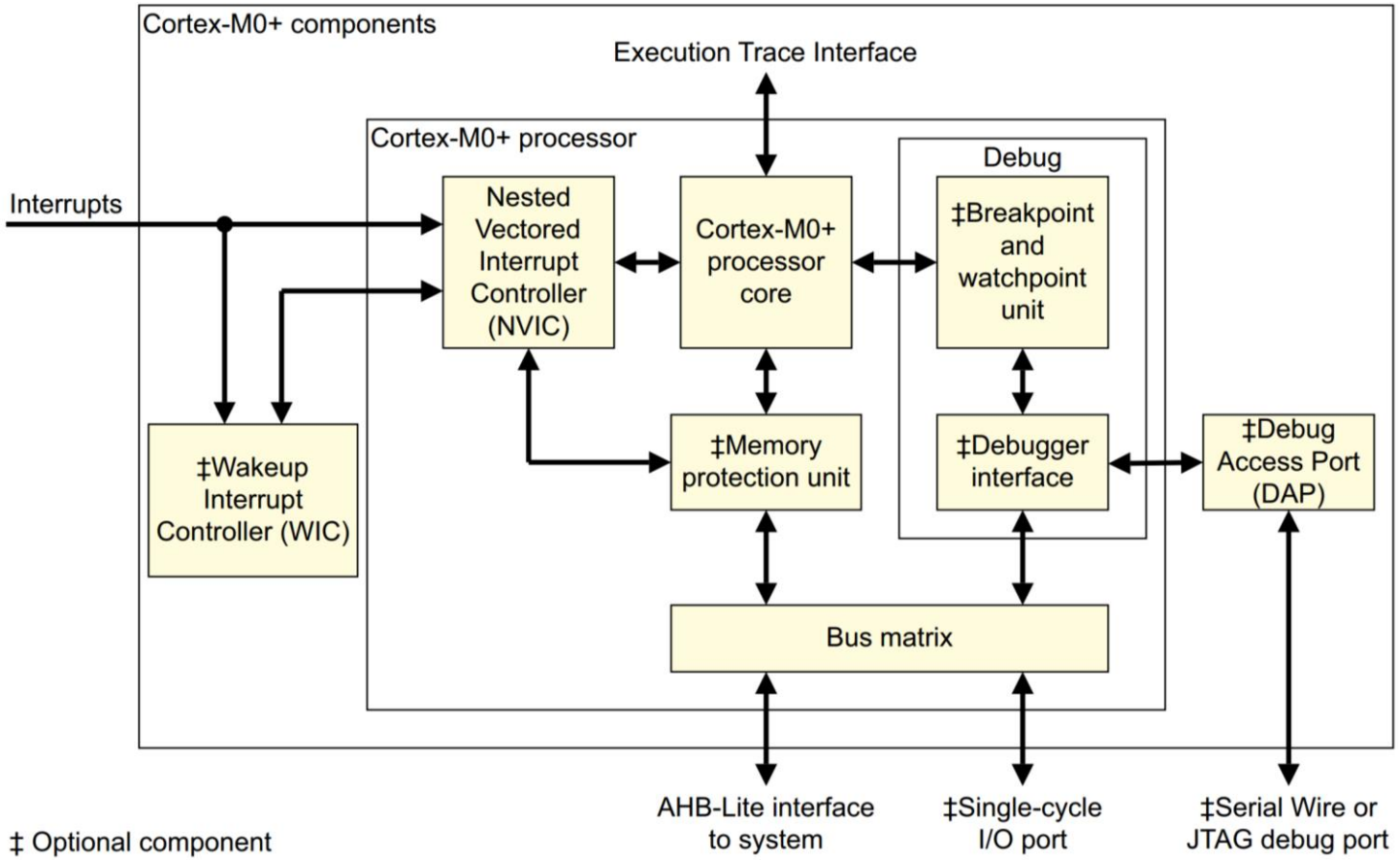
ARM Cortex-M0+

ARM Cortex-M0+ is Inside the NXP MKL25Z Chip

MKL25Z128 Integrated Circuit[1]



ARM Cortex-M0+

ARM Cortex-M0+ is Inside the NXP MKL25Z Chip

MKL25Z128 Integrated Circuit[1]

- Some Important Features
  - Word Size
  - Number of registers
  - Flash/RAM sizes
  - Branch Prediction Support
  - Instruction/Data Cache Support
  - Floating Point Arithmetic Support
  - DMA Support

Questions to Ask

- How much memory will I need for my application?
- How fast does the application need to run?
- What kind of mathematical support do I need?

Selector Guide

- Full Processor Family for KL2x Devices

- Each sub-family have different features from other sub-families
- Each device varies slightly in a sub-family

Sub-Family	Part Number	CPU (MHz)	Memory		Features															Package							
																				FM	FT	DA	LH	LK	LL	MP	MC
			Flash (KB)	SRAM (KB)	DMA	Low-Power UART	UART	ISO7 816-3	SPI	I²C	TSI	I²S	Flex IO	RTC	12-bit DAC	16-bit ADC w/DP Ch.	12-bit ADC	Total I/Os	Other	32 QFN (5 x 5, 0.5 mm)	48 QFN (7 x 7, 0.5 mm)	36X FBGA (3.5 x 3.5, 0.5 mm)	64 LQFP (10 x 10, 0.5 mm)	80 LQFP (12 x 12, 0.5 mm)	100 LQFP (14 x 14, 0.5 mm)	64 MAPBGA (5 x 5, 0.5 mm)	121 MAPBGA (8 x 8, 0.65 mm)
KL24	MKL24Z32xxx4	48 MHz	32	4	√	1	2		2	2				√			√	23~66	USB 2.0 FS OTG/ Host/Device	√	√	√	√				
	MKL24Z64xxx4	48 MHz	64	8	√	1	2		2	2				√			√	23~66	USB 2.0 FS OTG/ Host/Device	√	√	√	√				
KL25	MKL25Z32xxx4	48 MHz	32	4	√	1	2		2	2	√			√	√	√		23~66	USB 2.0 FS OTG/ Host/Device	√	√	√	√				
	MKL25Z64xxx4	48 MHz	64	8	√	1	2		2	2	√			√	√	√		23~66	USB 2.0 FS OTG/ Host/Device	√	√	√	√				
	MKL25Z128xxx4	48 MHz	128	16	√	1	2		2	2	√			√	√	√		23~66	USB 2.0 FS OTG/ Host/Device	√	√	√	√				
KL26	MKL26Z32xxx4	48 MHz	32	4	√	1	2		2	2	√	√		√	√	√		23~50	USB 2.0 FS OTG/ Host/Device	√	√	√					
	MKL26Z64xxx4	48 MHz	64	8	√	1	2		2	2	√	√		√	√	√		23~50	USB 2.0 FS OTG/ Host/Device	√	√	√					
	MKL26Z128xxx4	48 MHz	128	16	√	1	2		2	2	√	√		√	√	√		23~80	USB 2.0 FS OTG/ Host/Device	√	√	√		√		√	√
	MKL26Z256xxx4	48 MHz	256	32	√	1	2		2	2	√	√		√	√	√		50~80	USB 2.0 FS OTG/ Host/Device			√		√		√	√
KL27	MKL27Z128xxx4	48 MHz	128	32	√	2	1	1	2x 16b	2		√	√	√	√	√		23~50	USB 2.0 FS Device, with crystal-less USB	√	√	√					√
	MKL27Z256xxx4	48 MHz	256	32	√	2	1	1	2x 16b	2		√	√	√	√	√		23~50	USB 2.0 FS Device, with crystal-less USB	√	√	√					√
	MKL27Z32xxx4	48 MHz	32	8	√	2	1	1	2x 16b	2			√	√		√		23~50	Crystal-less USB, Device Only, Low Power Keep Alive	*	*	√	√			*	
	MKL27Z64xxx4	48 MHz	64	16	√	2	1	1	2x 16b	2			√	√		√		23~50	Crystal-less USB, Device Only, Low Power Keep Alive	*	*	√	√			*	

Product Brief

- Concise overview of a product
- Talks about use cases
- Gives more detailed feature specifications
- Nice on the eyes

Datasheet

- An Informative Dense Read

- Contains detailed Technical Specifications
  - Electrical
  - Timing
  - Environmental
  - Physical Package

Datasheet

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- Contains detailed Technical Specifications
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1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V

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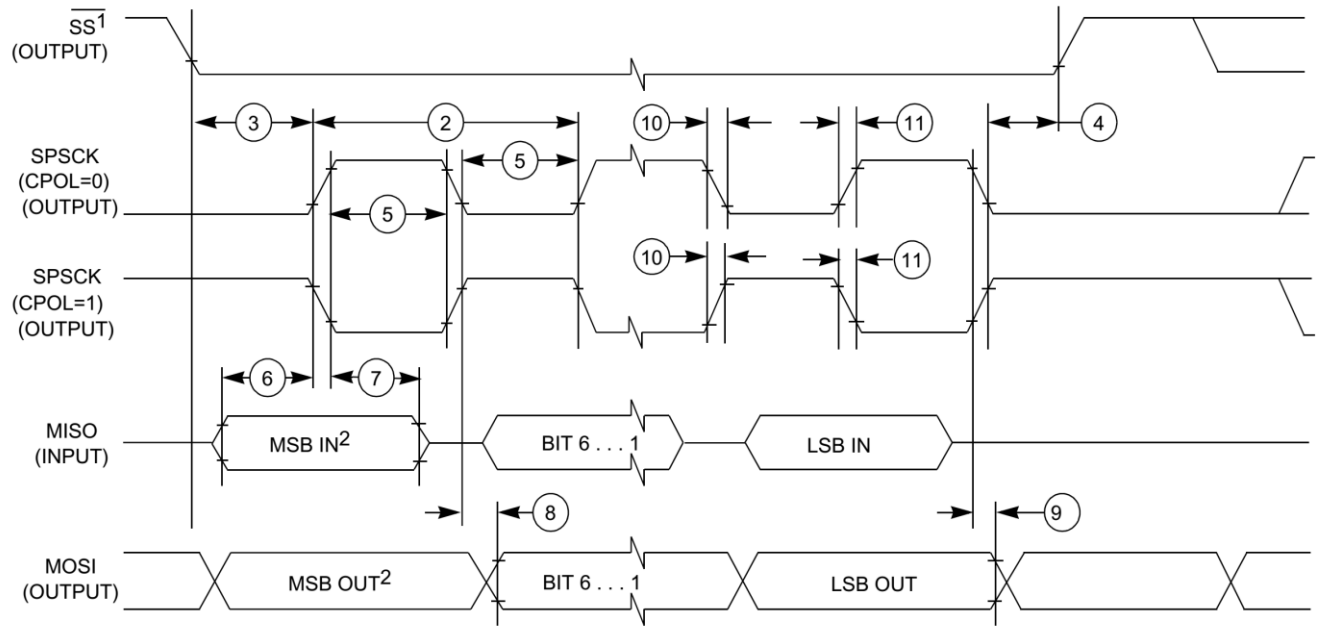

1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA = 0)

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Datasheet

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- Contains detailed Technical Specifications
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  - Timing
  - **Environmental**
  - Physical Package

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

2.4.2 Thermal attributes

Table 16. Thermal attributes

Board type	Symbol	Description	80 LQFP	64 LQFP	48 QFN	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	70	71	84	92	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	52	28	33	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	—	59	69	75	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	—	46	22	27	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	34	34	10	12	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	20	2.0	1.8	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.6	5	5.0	8	°C/W	4

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  - Timing
  - Environment
  - **Physical Package**

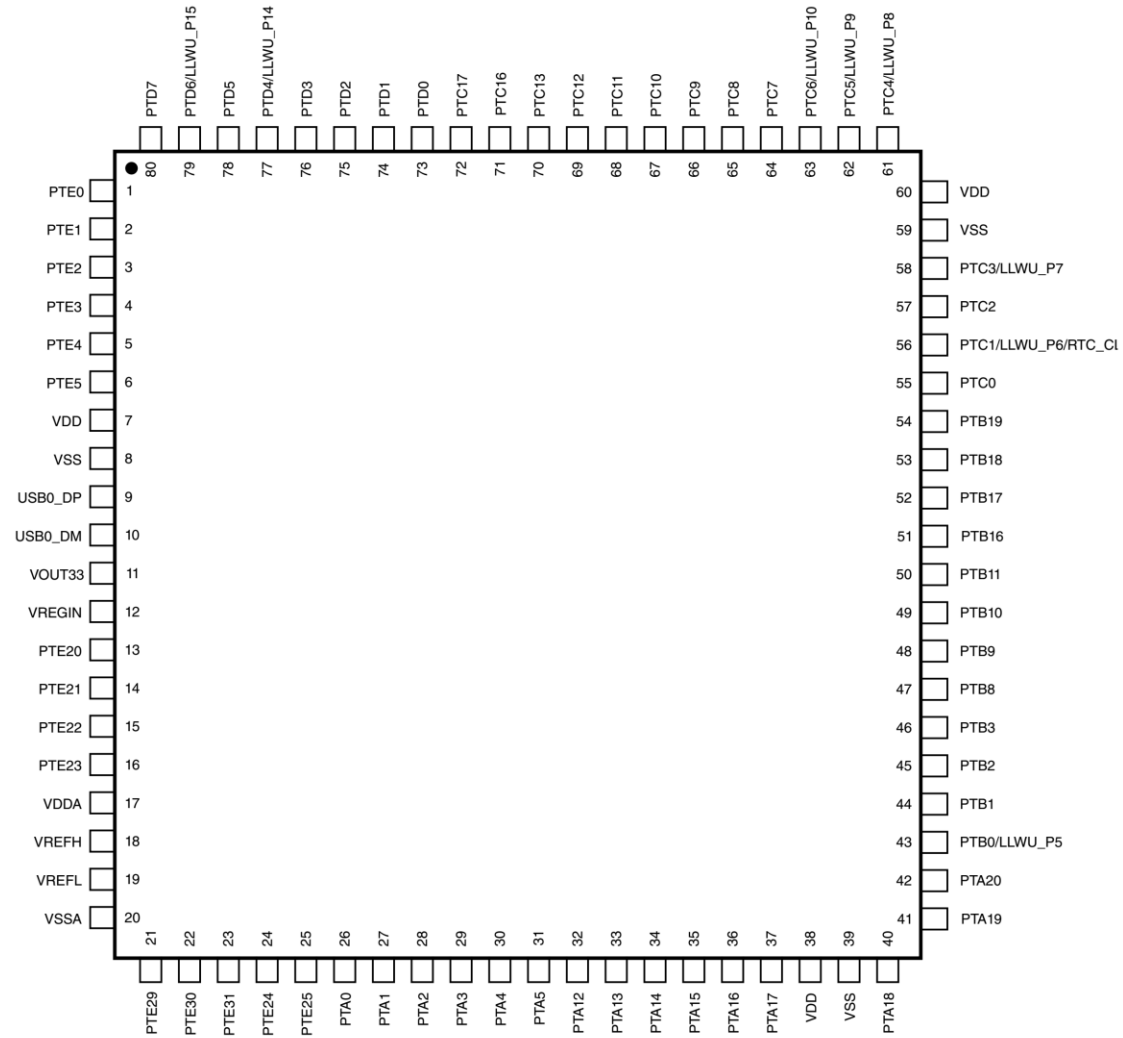


Figure 19. KL25 80-pin LQFP pinout diagram

Family Technical Reference Manuals

- Configuration details
- Operation descriptions
- Used to write Bare-Metal Firmware

11.2.2 Modes of operation

11.2.2.1 Run mode

In Run mode, the PORT operates normally.

11.2.2.2 Wait mode

In Wait mode, PORT continues to operate normally and may be configured to exit the Low-Power mode if an enabled interrupt is detected. DMA requests are still generated during the Wait mode, but do not cause an exit from the Low-Power mode.

11.2.2.3 Stop mode

In Stop mode, the PORT can be configured to exit the Low-Power mode via an asynchronous wakeup signal if an enabled interrupt is detected.

11.2.2.4 Debug mode

In Debug mode, PORT operates normally.

Address: Base address + 0h offset + (4d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0							ISF	0				IRQC			
W								w1c								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0					MUX			0	DSE	0	PFE	0	SRE	PE	PS
W																
Reset	0	0	0	0	0	x*	x*	x*	0	x*	0	x*	0	x*	x*	x*

* Notes:
- x = Undefined at reset.

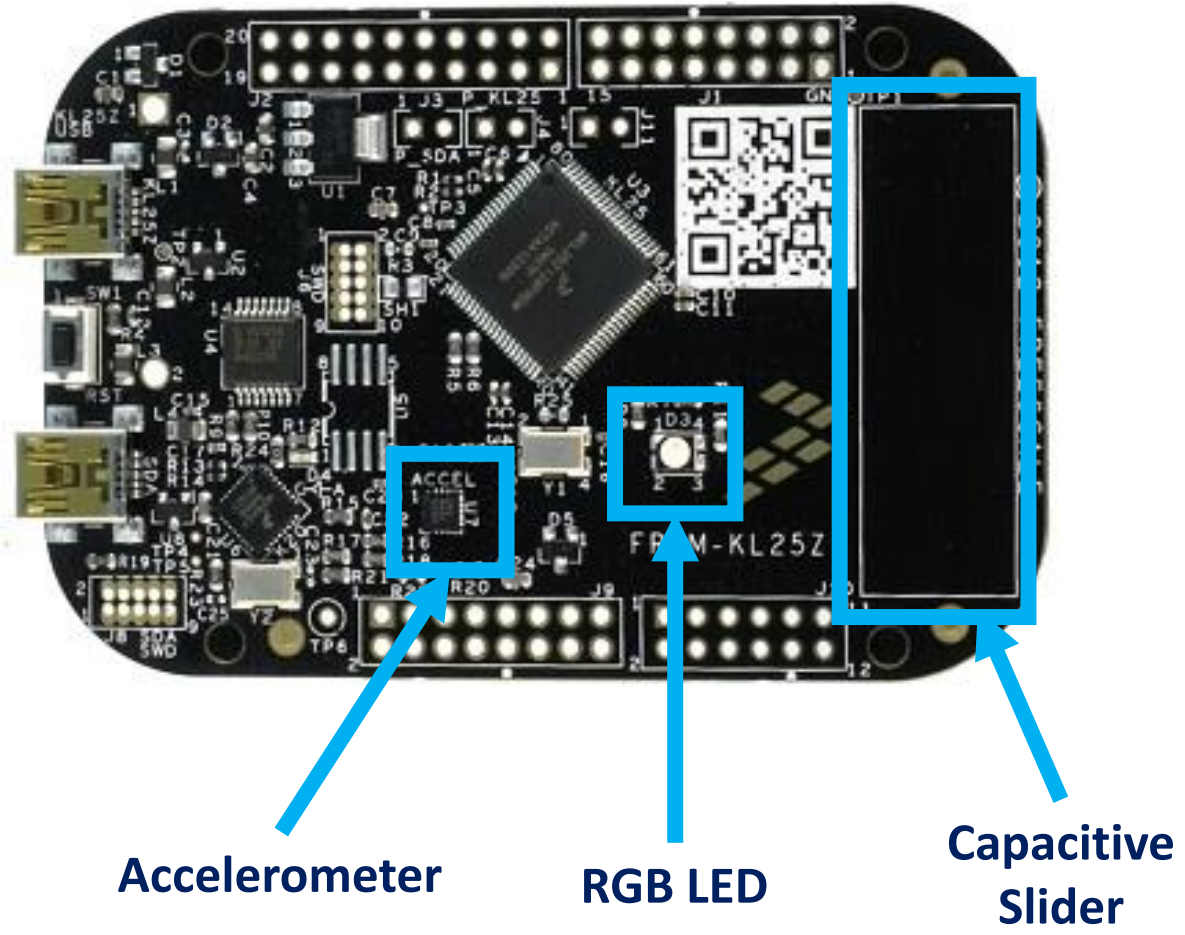
Chip Errata

- Integrated Circuits are not perfect
- Error descriptions
- Provides corrective information or workaround to issue

Errata ID	Errata Title
3863	ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage
5751	FTFx: Launching the Read 1's Section command (RD1SEC) on an entire flash block results in access error (ACCER).
6070	I2C: Repeat start cannot be generated if the I2Cx_F[MULT] field is set to a non-zero value
5746	PIT: When using the PIT to trigger DMA transfers using cycle steal mode, two data transfers per request are generated
5666	PMC: Maximum current consumption in VLPR, VLPW, VLPS, LLS and VLLS modes may be higher than data sheet specification.
5667	PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes
5472	SMC: Mode transition VLPR->VLLS0(POR disabled)->RUN, will cause POR & LVD.
5745	SPI1: Back to back DMA data transfers are not possible if the core:bus frequency ratio is greater than 4:1
5490	SPI1: DMA data transfers at the maximum baud rate can result in corrupted data
5515	TSI: The end of scan flag is not automatically cleared when continuously scanning
5744	UART0: Receiver wakeup control bit cannot be set immediately after a wakeup event
5563	UART0: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly
5753	UART1 / UART2: When the Receiver Wake Up control bit is set, an IDLE condition is not detected correctly
5928	USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases

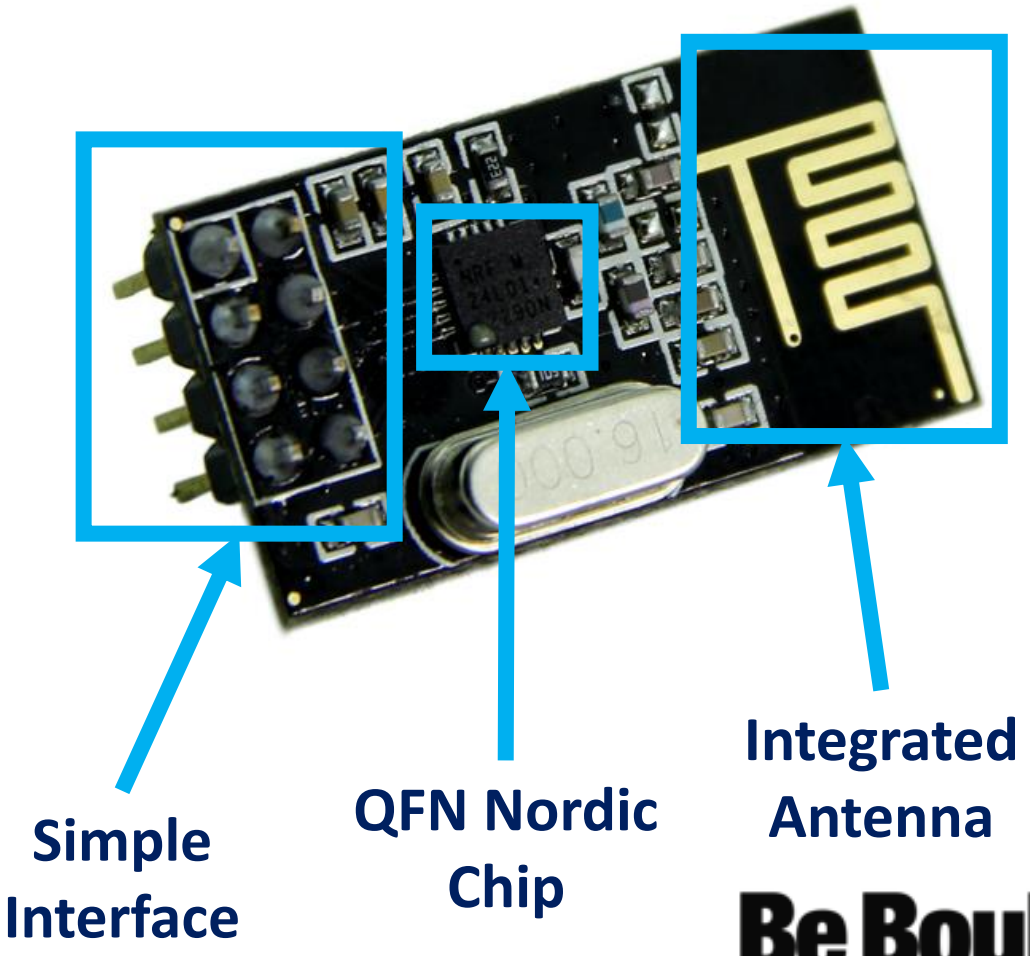
Development Kits

- FRDM-KL25Z from NXP
- ARM Cortex-M0+ Processor
- Supplemental Hardware
  - Capacitive Touch Slide
  - RGB LED
  - Accelerometer

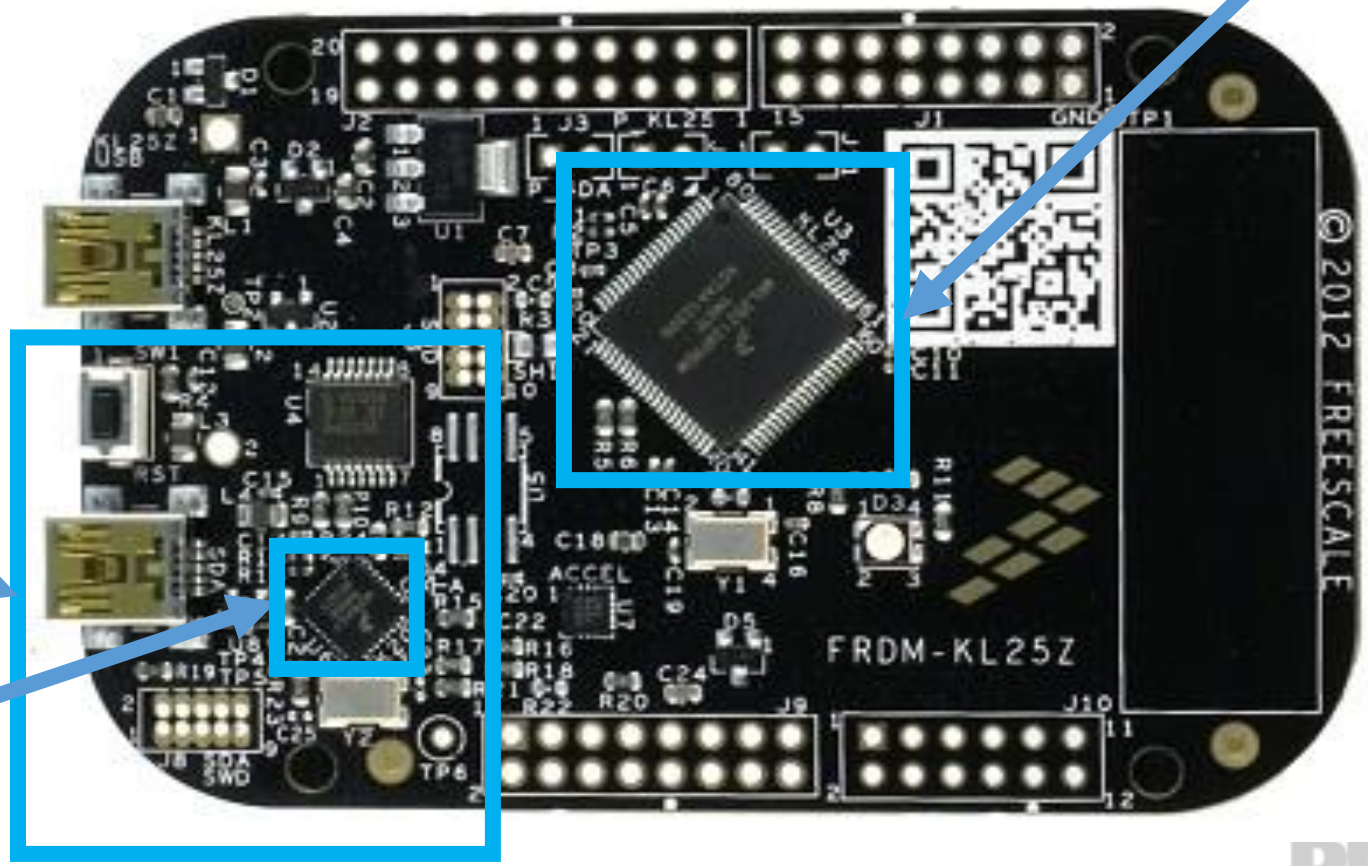


Development Kits

- nRF24L01+ Wireless Module
- Nordic Chipset in QFN Package
  - Hard to solder
- Requires specific PCB layout

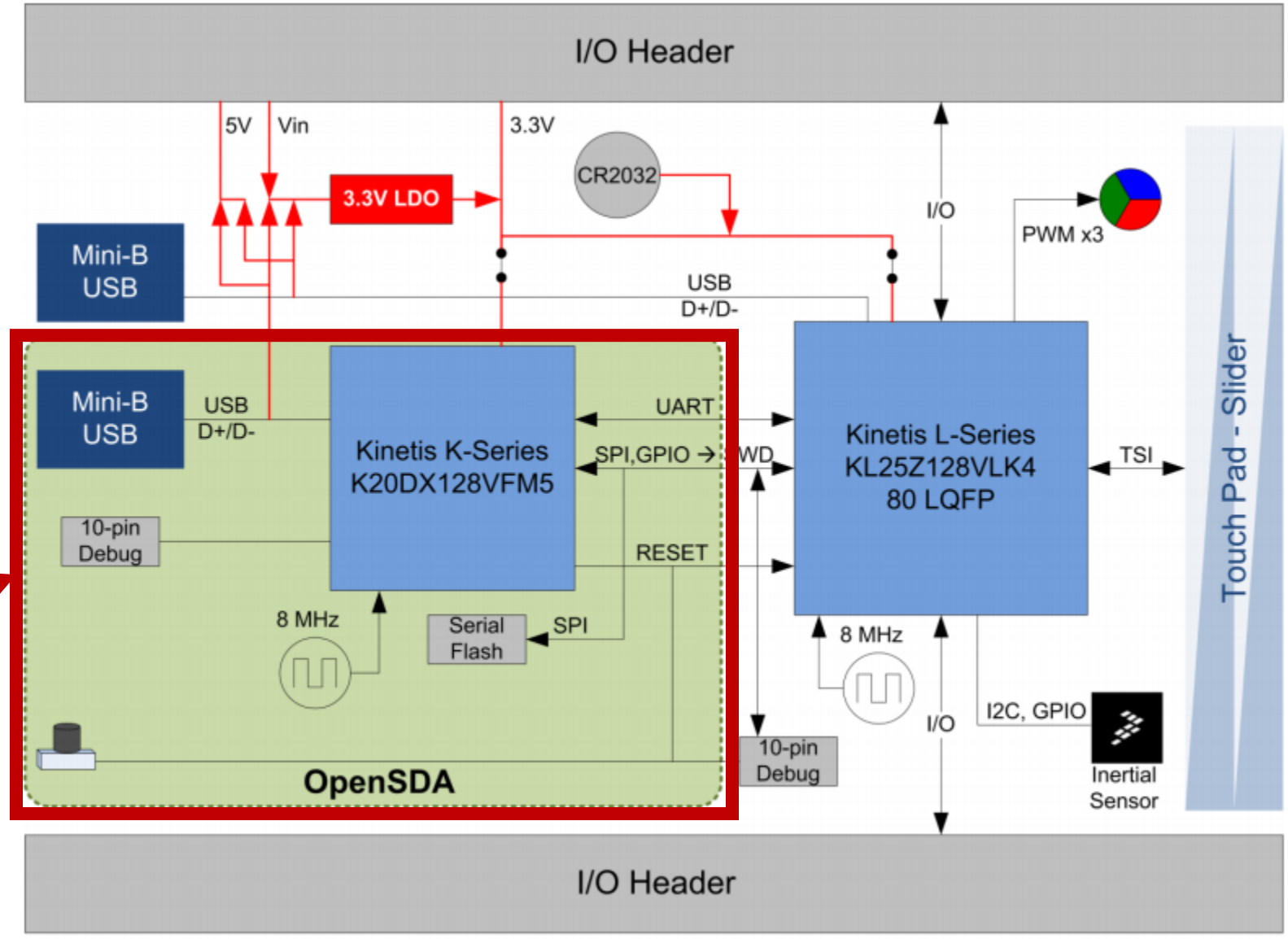


On-board Programmer/Debugger Support



KL25z On-board Development support

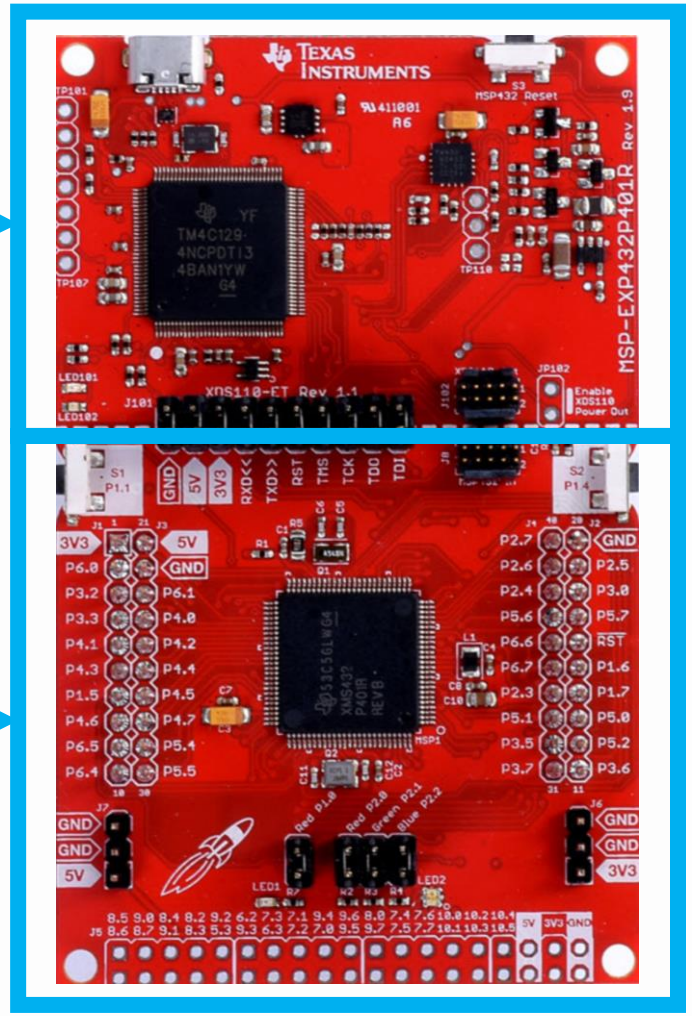
OpenSDA (Open Standard Serial Debug Adapter)



On-board Programmer/Debugger Support

XDS110-ET On-board Emulator

Target Processor MSP432



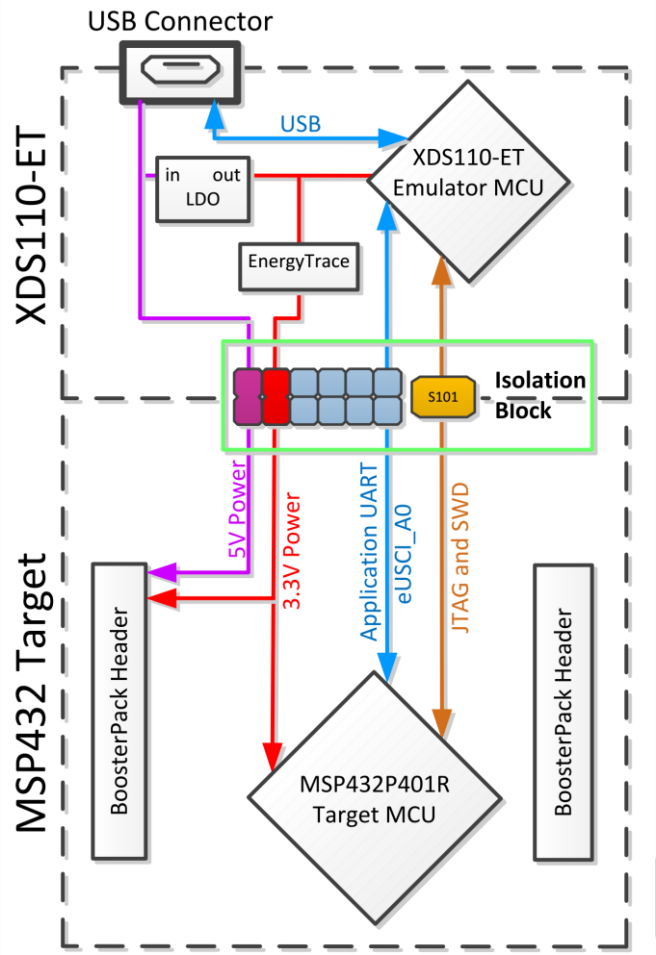


Figure 6. XDS110-ET Isolation Block