The instruction set of Intel® 8080 / 8085 microprocessors

One byte transfers

MOV R1, R2.	R1 ← R2.
MOV R, M.	R ← M[HL].
MOV M, R.	M[HL] ← R.
MVI R, D8.	R ← D8.
MVI M, D8.	M[HL] ← D8.
STAX RP.	M[RP] ← A.
LDAX RP.	A ← M[RP].
STA ADR.	M[ADR] ← A.
LDA ADR.	A ← M[ADR].

Input and output instructions

IN PORT.	A ← PORT.
OUT PORT.	PORT ← A.

Two bytes transfers

LXI RP, D16.	RPL ← D16L, RPH ← D16H.
SHLD ADR.	M[ADR] ← L, M[ADR+1] ← H.
LHLD ADR.	L ← M[ADR], H ← M[ADR+1].
PUSH RP.	M[SP – 1] ← RPH, M[SP – 2] ← RPL, SP ← SP – 2.
PUSH PSW.	M[SP – 1] ← A, M[SP – 2] ← F, SP ← SP – 2.
POP RP.	RPL ← M[SP], RPH ← M[SP + 1], SP ← SP + 2.
POP PSW.*	F ← M[SP], A ← M[SP + 1], SP ← SP + 2.
SPHL.	SP ← HL.

Exchange of bytes

XCHG.	H ↔ D, L ↔ E.
XTHL.	L ↔ M[SP], H ↔ M[SP + 1].

Arithmetic and logic instructions with one operand

8-bit instructions

CMC.**	CY ← ¬CY.	INR R.***	R ← R + 1.	Decimal adjust	
STC.**	CY ← 1.	DCR R.***	R ← R – 1.		
CMA.	A ← ¬A.	INR M.***	M[HL] ← M[HL] + 1.	DAA.*	If $A_{3-0} > 9$ or AC = 1,
		DCR M.***	M[HL] ← M[HL] – 1.		then $A_{3-0} \leftarrow A_{3-0} + 6$;
		INX RP.	RP ← RP + 1.		if $A_{7-4} > 9$ or CY = 1,
		DCX RP.	RP ← RP – 1.		then $A_{7-4} \leftarrow A_{7-4} + 6$.

Arithmetic and logic instructions with two operands

8-bit instructions

ADD R.*	A ← A + R.	ADI D8.*	A ← A + D8.	ADD M.*	A ← A + M[HL].
ADC R.*	A ← A + R + CY.	ACI D8.*	A ← A + D8 + CY.	ADC M.*	A ← A + M[HL] + CY.
SUB R.*	A ← A – R.	SUI D8.*	A ← A – D8.	SUB M.*	A ← A – M[HL].
SBB R.*	A ← A – (R + CY).	SBI D8.*	A ← A – (D8 + CY).	SBB M.*	A ← A – (M[HL] + CY).
ANA R.*	A ← A ∧ R.	ANI D8.*	A ← A ∧ D8.	ANA M.*	A ← A ∧ M[HL].
ORA R.*	A ← A ∨ R.	ORI D8.*	A ← A ∨ D8.	ORA M.*	A ← A ∨ M[HL].
XRA R.*	A ← A ∀R.	XRI D8.*	A ← A ∀D8.	XRA M.*	A ← A ∀M[HL].
CMP R.*	A – R.				
CMP M.*	A – M[HL].				
CPI D8.*	A – D8.				

16-bit instructions

DAD RP.** HL ← HL + RP.

Accumulator content rotation instructions

RLC.** $A_{n+1} \leftarrow A_n$, n = 0–6, $A_0 \leftarrow A_7$, CY ← A_7. Rotate to left.
RRC.** $A_n \leftarrow A_{n+1}$, n = 0–6, $A_7 \leftarrow A_0$, CY ← A_0. Rotate to right.
RAL.** $A_{n+1} \leftarrow A_n$, n = 0–6, A_0 ← CY, CY ← A_7. Rotate left through carry flag CY.
RAR.** $A_n \leftarrow A_{n+1}$, n = 0–6, A_7 ← CY, CY ← A_0. Rotate right through carry flag CY.

Branch instructions

PCHL.	PC ← HL.
JMP ADR.	PC ← M[ADR].
Jcc ADR.	PC ← M[ADR].

Call to subroutine and return from subroutine instructions

CALL ADR.	M[SP] ← PC + 3, SP ← SP – 2, PC ← ADR.
Ccc ADR.	M[SP] ← PC + 3, SP ← SP – 2, PC ← ADR.
RST N.	PC ← 8 × N (N = 0, 1, …, 7). 8 × N = ADR. ADR = 0_{16}, 8_{16}, 10_{16}, 18_{16}, 20_{16}, 28_{16}, 30_{16}, 38_{16}.
RET.	PC ← M[SP], SP ← SP + 2.
Rcc.	PC ← M[SP], SP ← SP + 2.

Microprocessor control instructions

EI	Enable interrupts.	
DI	Disable interrupts.	
HLT	Halt.	
NOP	PC ← PC + 1.	No operation.

Format of flags register F

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	0	AC	0	P	1	CY

Notes:
***** – instruction affects all flags.
****** – instruction affects only flag **CY**.
******* – instruction affects all flags except **CY**.
R, **R1**, **R2** – the contents of registers **A**, **B**, **C**, **D**, **E**, **H** or **L** (8-bits);
M – memory location, whose address is in register pair **HL**;
M[HL] – content of the memory location, whose address is in register pair **HL** (8-bits);
D8 – 8-bit immediate data or direct operand (second byte of the instruction);
D16 – 16-bit immediate data or direct operand (second and third byte of the instruction);
D16L and **D16H** – lower and higher byte of 16-bit immediate data or direct operand;

ADR – 16-bit address of memory location (second and third byte of the instruction);
M[ADR] – content of the memory location, whose address is specified in second and third byte of the instruction (8-bits);
RP – register pair **BC**, **DE**, **HL** or content of stack pointer **SP** (16-bits);
RPL and **RPH** – low and high order register of register pair;
M[RP] – content of the memory location, whose address is in register pair **BC** or **DE** (8-bits);
M[SP] – stack;
SP – 16-bit stack pointer;
PC – 16-bit program counter;
PSW – 16-bit processor status word (contents of register **A** and flags register **F**);
PORT – 8-bit number (address) of input or output port (second byte of the instruction);
N – interrupt maintenance subroutine number;
n – bit number (bits are numbered from right to left from 0 to 7);
cc – branch condition (must be replaced by **NZ**, **Z**, **NC**, **C**, **PO**, **PE**, **P** or **M**);
CY – carry bit of flags register **F**;
P – parity bit of flags register **F**;
AC – auxiliary carry bit of flags register **F**;
Z – zero bit of flags register **F**;
S – sign bit of flags register **F**;
$\wedge$ – logical AND;
$\vee$ – logical inclusive OR;
$\forall$ – logical exclusive OR;
$\neg$ – complement;
$\leftarrow$ – transfer;
$\leftrightarrow$ – exchange.

The instructions hexadecimal codes of Intel® 8080 / 8085 microprocessors

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	NOP	LXI B, D16	STAX B	INX B	INR B	DCR B	MVI B, D8	RLC	–	DAD B	LDAX B	DCX B	INR C	DCR C	MVI C, D8	RRC	**0**
1	–	LXI D, D16	STAX D	INX D	INR D	DCR D	MVI D, D8	RAL	–	DAD D	LDAX D	DCX D	INR E	DCR E	MVI E, D8	RAR	**1**
2	RIM[1]	LXI H, D16	SHLD ADR	INX H	INR H	DCR H	MVI H, D8	DAA	–	DAD H	LHLD ADR	DCX H	INR L	DCR L	MVI L, D8	CMA	**2**
3	SIM[1]	LXI SP, D16	STA ADR	INX SP	INR M	DCR M	MVI M, D8	STC	–	DAD SP	LDA ADR	DCX SP	INR A	DCR A	MVI A, D8	CMC	**3**
4	MOV B, B	MOV B, C	MOV B, D	MOV B, E	MOV B, H	MOV B, L	MOV B, M	MOV B, A	MOV C, B	MOV C, C	MOV C, D	MOV C, E	MOV C, H	MOV C, L	MOV C, M	MOV C, A	**4**
5	MOV D, B	MOV D, C	MOV D, D	MOV D, E	MOV D, H	MOV D, L	MOV D, M	MOV D, A	MOV E, B	MOV E, C	MOV E, D	MOV E, E	MOV E, H	MOV E, L	MOV E, M	MOV E, A	**5**
6	MOV H, B	MOV H, C	MOV H, D	MOV H, E	MOV H, H	MOV H, L	MOV H, M	MOV H, A	MOV L, B	MOV L, C	MOV L, D	MOV L, E	MOV L, H	MOV L, L	MOV L, M	MOV L, A	**6**
7	MOV M, B	MOV M, C	MOV M, D	MOV M, E	MOV M, H	MOV M, L	HLT	MOV M, A	MOV A, B	MOV A, C	MOV A, D	MOV A, E	MOV A, H	MOV A, L	MOV A, M	MOV A, A	**7**
8	ADD B	ADD C	ADD D	ADD E	ADD H	ADD L	ADD M	ADD A	ADC B	ADC C	ADC D	ADC E	ADC H	ADC L	ADC M	ADC A	**8**
9	SUB B	SUB C	SUB D	SUB E	SUB H	SUB L	SUB M	SUB A	SBB B	SBB C	SBB D	SBB E	SBB H	SBB L	SBB M	SBB A	**9**
A	ANA B	ANA C	ANA D	ANA E	ANA H	ANA L	ANA M	ANA A	XRA B	XRA C	XRA D	XRA E	XRA H	XRA L	XRA M	XRA A	**A**
B	ORA B	ORA C	ORA D	ORA E	ORA H	ORA L	ORA M	ORA A	CMP B	CMP C	CMP D	CMP E	CMP H	CMP L	CMP M	CMP A	**B**
C	RNZ	POP B	JNZ ADR	JMP ADR	CNZ ADR	PUSH B	ADI D8	RST 0	RZ	RET	JZ ADR	–	CZ ADR	CALL ADR	ACI D8	RST 1	**C**
D	RNC	POP D	JNC ADR	OUT PORT	CNC ADR	PUSH D	SUI D8	RST 2	RC	–	JC ADR	IN PORT	CC ADR	–	SBI D8	RST 3	**D**
E	RPO	POP H	JPO ADR	XTHL	CPO ADR	PUSH H	ANI D8	RST 4	RPE	PCHL	JPE ADR	XCHG	CPE ADR	–	XRI D8	RST 5	**E**
F	RP	POP PSW	JP ADR	DI	CP ADR	PUSH PSW	ORI D8	RST 6	RM	SPHL	JM ADR	EI	CM ADR	–	CPI D8	RST 7	**F**
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**	

[1] Instruction is only supported on the Intel® 8085 microprocessor.