1 INSTRUCTION SET OF MICROPROCESSOR INTEL 8080 (КР580ИК80А)

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One Byte Transfers
                                                                  Two Bytes Transfers
MOV R1, R ;5/7;
                                                                                                  D16---->YZ.
                             R \longrightarrow R1
                                                                  LXI YZ,D16
                                                                                 :10:
            ;7/10;
                                                                                                  H\longrightarrow M(ADR+1), L\longrightarrow M(ADR).
MVI R, D8
                             D8---->R.
                                                                  SHLD ADR
                                                                                  ;16;
                             A \longrightarrow M(YZ).
STAX YZ
                                                                  LHLD ADR
                                                                                  ;16;
                                                                                                  M(ADR) \longrightarrow L, M(ADR+1) \longrightarrow H.
                                                                  PUSH YZ
                                                                                                  YZ \longrightarrow M(SP-1) M(SP-2),
LDAX YZ
             :7:
                             M(YZ)\longrightarrow A.
                                                                                 ;11;
                                                                                                  SP-2->SP.
STA ADR
                             A \longrightarrow M(ADR).
             ;13;
LDA ADR
            ;13;
                             M(ADR) \longrightarrow A
                                                                  POP, YZ
                                                                                  ;10;
                                                                                                  M(SP) M(SP+1) \longrightarrow YZ
                                                                  (POP' PSW)
                                                                                                  SP+2\longrightarrow SP
Input and Output Instructions
                                                                                                  HL--->SP.
                                                                  SPHL
                                                                                  ;5;
IN N
             ;10;
                     (N) \longrightarrow A.
                                                                  Exchange of Bytes
OUT N
             ;10;
                     A--->(N).
                                                                  XCHG
                                                                                  ;4;
                                                                                                  HL<--->DE.
                                                                                                  H < \longrightarrow M(SP+1), L < \longrightarrow M(SP).
                                                                  XTHL
                                                                                  :18:
Arithmetic and Logic Instructions with One Operand
                     C---> C .
CMC''
                                                  INR''' R
             :4:
                                                               ;5/10; R+1--->R.
STC"
             ;4;
                         ->C.
                                                  DCR" R
                                                               ;5/10; R-1--->R.
             ;4;
CMA
                     A----> A .
                                                  INX
                                                           YZ ;5
                                                                       YZ+1\longrightarrow YZ.
                                                                       YZ-1--->YZ.
DAA'
             ;4;
                     Decimal Adjust
                                                  DCX
                                                          YZ ;5
Arithmetic and Logic Instructions with Two Operands
8 bit Instructions
                                                                                                  CPI' D8 ;7; Flags Fixing
ADD'R
                                       ADI' D8
             ;4/7; A+R---->A.
                                                          A+D8\longrightarrow A.
                                                                                                  CMP' R
                                                                                                            ;4/7; accordingly to
ADC' R
             ;4/7; A+R+CY—>A.
                                       ACI' D8
                                                     ;7;
                                                          A+D8+CY--->A.
                                                                                                                  A-D8 or A-R
SUB' R
             ;4/7; A-R—>A.
                                       SUI' D8
                                                     ;7;
                                                          A-D8---->A.
SBB' R
             ;4/7; A-R-CY->A.
                                       SBI' D8
                                                     ;7;
                                                          A-D8-CY--->A.
ANA' R
             ;4/7; A∩R—>A.
                                       ANI' D8
                                                     ;7;
                                                          A∩D8—->A.
                                                                                                  16 bit Instructions
ORA' R
                                       ORI' D8
                                                          A \cup D8 \longrightarrow A.
             ;4/7; AUR-->A.
                                                                                                  DAD" YZ ;10;
                                                                                                                      HL+YZ --->HL
XRA' R
             :4/7; A⊕R—->A.
                                       XRI' D8
                                                          A⊕D8——>A.
Accumulator Content Rotation Operations
                                                                          Control Transfer Instructions
RLC";4;
RAL";4;
            Rotate Left.
                                                                                       ;5; HL—>PC
                                                                          PCHL
                                                                                       ;10; ADR->PC.
             Rotate Left Through Carry Flag CY.
                                                                          JMP ADR
RRC'' ;4;
                                                                          J-CON ADR ;10; ADR->PC.
             Rotate Right.
RAR'' ;4;
             Rotate Right Through Carry Flag CY.
Microprocessor Control Instructions
             Enable Interrupts.
                                               Instructions of Subroutine Call and Return from It
ΕI
DΙ
        ;4;
             Disable Interrupts.
                                               CALL ADR
                                                               :17:
                                                                          PC--->M(SP-1) M(SP-2);ADR---->PC.
                                                                          PC--->M(SP-1) M(SP-2);ADR---->PC.
HLT
             Halt.
                                               C-CON ADR
                                                               ;11(17);
        ;4;
                                                                          PC—>M(SP-1) M(SP-2);ADR—>PC, where X=0,1,...,7
NOP
            No Operations.
                                               RST X
                                                               ;11;
                                                                          ADR accordingly equal to 0H, 8H, 10H, 18H, 20H, 28H, 30H, 38H.
Format of Flags Register F
                                               RET
                                                               :10:
                                                                          M(SP) M(SP+1) \longrightarrow PC.
D7 D6 D5 D4 D3 D2 D1 D0
                                               R-CON
                                                                ;5(11);
                                                                          SP+2---->SP.
              AC 0 P
     Z
          0
Notes
             - Instruction Affect All Flags.
             - Instruction Affect Flag CY.
,,,
             - Instruction Affect All Flags Except CY.
R, R1
             - Contents of Registers A, B, C, D, E, H, L or Content of Memory Cell M(HL).
             - Register Pairs BC, DE, HL, SP or Content of PSW.
YZ.
SP
             - Content of Stack Pointer Before Instruction Execution.
D8
             - 8 bit Immediate Data (Content of Second Byte of Two Bytes Instruction).
             - Content of Input or Output Port, which Number N (N=0, 1, ..., 255).
(N)
D16
             - 16 bit Operand (Content of Second and Third Byte of Instruction).
ADR

    16 bit Address of Three Bytes Instruction.

M()
             - Content of Memory Cell (In Brackets are Address of Memory Cell).
-CON
             - Condition (-CON Must be Replaced by NZ, Z, NC, C, PO, PE, P or M).
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