CISE ADIC Lab 2023

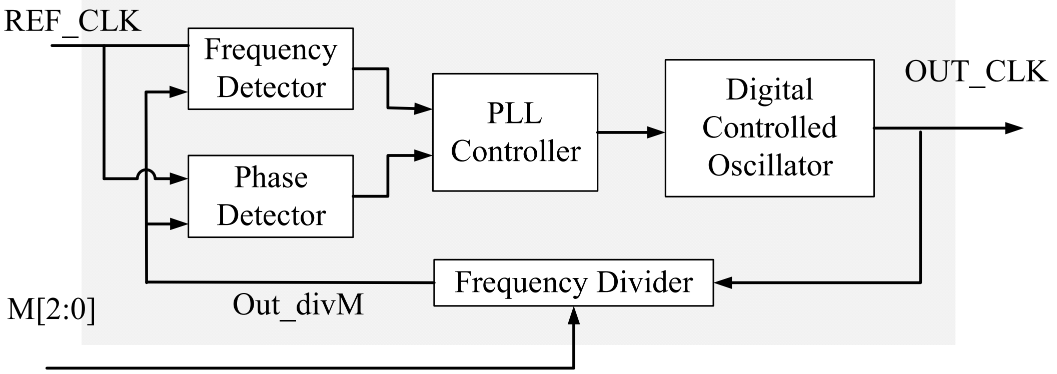
Final Project – Design an All-Digital Phase-Locked Loop

Due on: 17:00, Jan. 02, 2024

Before starting to work on this project, please carefully read the following description, including system I/O ports, specifications, and requirements. Then, following the given instructions, don’t hesitate to contact TA if you find any ambiguity in the note or project description.

All-Digital Phase-Locked Loop:

The general architecture of an All-Digital Phase-Locked Loop (ADPLL) is shown in the following figure. First, the Phase and Frequency Detector (PFD) compares the phase and frequency error between the reference clock (REF_CLK) and the output divided clock (Out_divM). Then, it outputs a control signal to the PLL controller to update the output frequency of the Digital-Controlled Oscillator (DCO) for tracking the reference clock. Finally, when ADPLL is locked, it turns into phase and frequency maintenance mode and keeps tracking the phase and frequency of the reference clock.



Project Description:

The topic of this project is to design an All-Digital Phase-Locked Loop (ADPLL) and perform Analog and Mixed-Mode Simulation using ADE-L to verify your design. The architecture specifications and system requirements are given as follows:

1. Input Ports: ***REF_CLK, M [2:0], RESET***
2. Output Ports: ***OUT_CLK, LOCK***
3. ***RESET*** is the reset signal for the PLL.
4. ***REF_CLK*** is the reference clock of the PLL.

5. ***M[2:0]*** means frequency divider ratio, ranging from 3’d1 to 3’d7.
6. ***OUT_CLK*** is the output clock of the PLL.
7. ***LOCK***=1’b0 when PLL is not locked, and it should assert ***LOCK***=1’b1 when PLL is locked.
8. When PLL is locked, the frequency of ***OUT_CLK*** is ***REF_CLK* × *M*** and the phase error between ***REF_CLK*** and ***OUT_CLK*** should be minimized.
9. **You must design a digital loop filter in the PLL controller to reduce the jitter of the output clock (*OUT_CLK*).**
10. You must build up the DCO Verilog behavior model and PFD Verilog behavior model and perform PLL behavior simulation first to prove the functional correctness of your PLL.
11. You must then use **ADE-L** to simulate your PLL with both PFD and DCO using SPICE circuits, and the PLL controller and frequency divider use digital Verilog models in ADE-L simulation.
12. **You must determine the specifications of your PLL.**
13. **You should hand over one report for TA (in PDF format). You are required to describe the architecture/circuit of your design as detailed as possible. In addition, the final specifications of your PLL are also required to be listed in the report. (Please see 02_All-Digital_PLL.pdf, page 7, to write your PLL specifications)**
14. **DON’T INCLUDE YOUR VERILOG CODES OR SPICE NETLISTS IN THE REPORT UNLESS IT IS NECESSARY.**
15. **Illustrate your design and how you can prove your design is correct or not.**

Demo:

1. **Demo1:** You must complete the PLL behavior simulation to demonstrate the function of your PLL is correct.
2. **Demo2:** You must complete the ADE-L simulation with PFD and DCO using SPICE circuits. In addition, the performance degraded of your PLL when the real circuits are added to the ADE-L simulation should be discussed.
3. **Demo3:** Final project report. If your ADPLL has some special features, for example, low jitter or fast lock-in time, you will get a higher grade than the other students.

Grade:

Demo1: Correct PLL Behavior Simulation (30%)

Demo2: Correct AMS-Ultra PLL Simulation (45%)

Demo3: Final Project Report (25%)

Note: The final project must be finished before **17:00 Jan. 02, 2024.**