CSIE ADIC Lab 2023

Lab06D. Design a FSK Modem with ADE-L

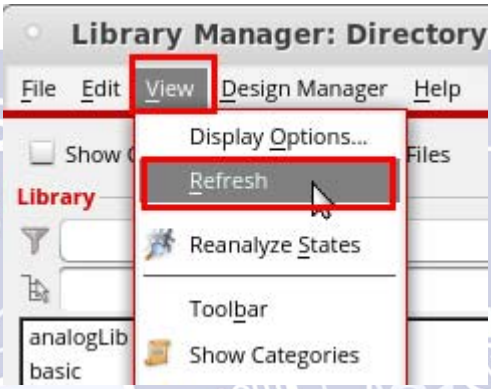
1. Data Preparation

1. Extract LAB data from TA's directory:
   % tar xzvf ~adicta/lab06d.tar.gz
2. The extracted LAB directory (**lab06d**) contains:
   a. 00_library/ : HSPICE Models and Cell circuits
   b. Demo1/ : ADE-L Example 1
   c. Demo2/ : ADE-L Example 2
   d. Demo3/ : ADE-L Example 3
   e. Demo4/ : ADE-L Example 4
   f. Exercise/ : FSK Modem design

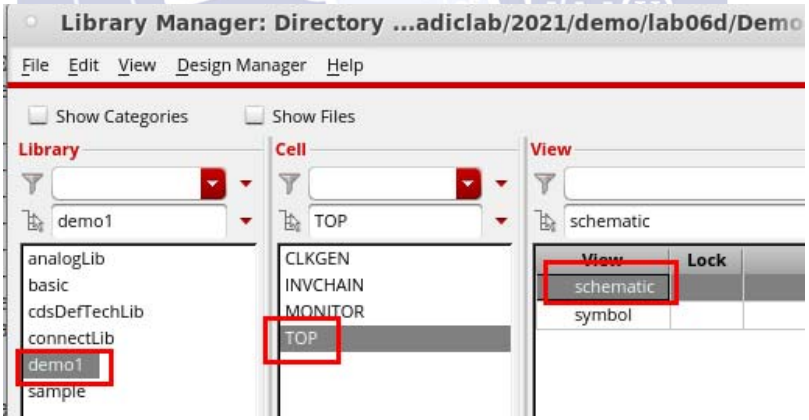
2. Run ADE-L Demo1: Full Behavior

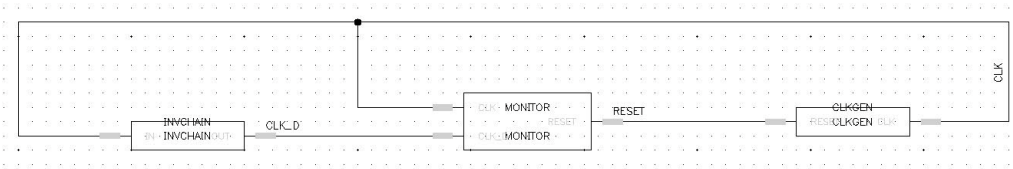
1. Change to directory: **Demo1**
2. Open and reading the demo1 verilog codes.
   % gedit *.v &
   This is a simple circuit which uses a behavior model (CLKGEN.v) to generate a 100MHz clock as reference clock (REF_CLK), then it is delayed by a delay line which has 0.5ns delay (INVCHAIN.v). The top module of demo1 is TOP (TOP.v), and the MONITOR module (MONITOR.v) is a test module to give reset inputs and dump the digital output waveform.
3. Execute Virtuoso environment to perform AMS simulation of demo1
   % virtuoso &
   A CIW (Command Input Window) is opened, and it creates a log file (CDS.log) in your home directory.
4. In CIW menu, open ***File -> Import -> Verilog***

5. In the **Verilog In [Import Options]** tab, fill up the following field:
   a. Verilog Files To Import: **TOP.v**
   b. Target Library Name: **demo1**
6. In the **Verilog In [Global Net Options]** tab, fill up the following field:
   a. Power Net Name: **VDD**
   b. Ground Net Name: **GND**
   c. Click **OK** button
7. In Library Manager, open ***View -> Refresh*** to update the Library list.

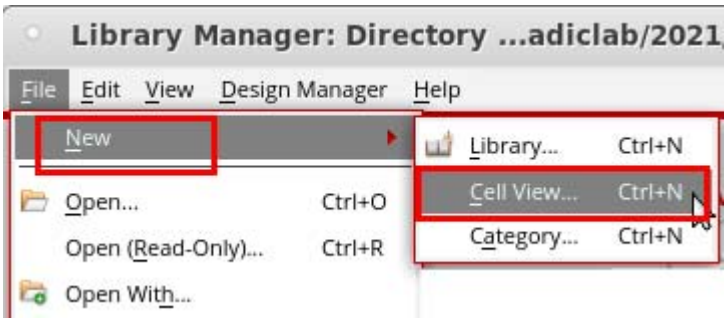


8. The top-level design for this lab is Library: **demo1**, Cell: **TOP**, View: **schematic**. Double click on **schematic** view to open the schematic view of this design.



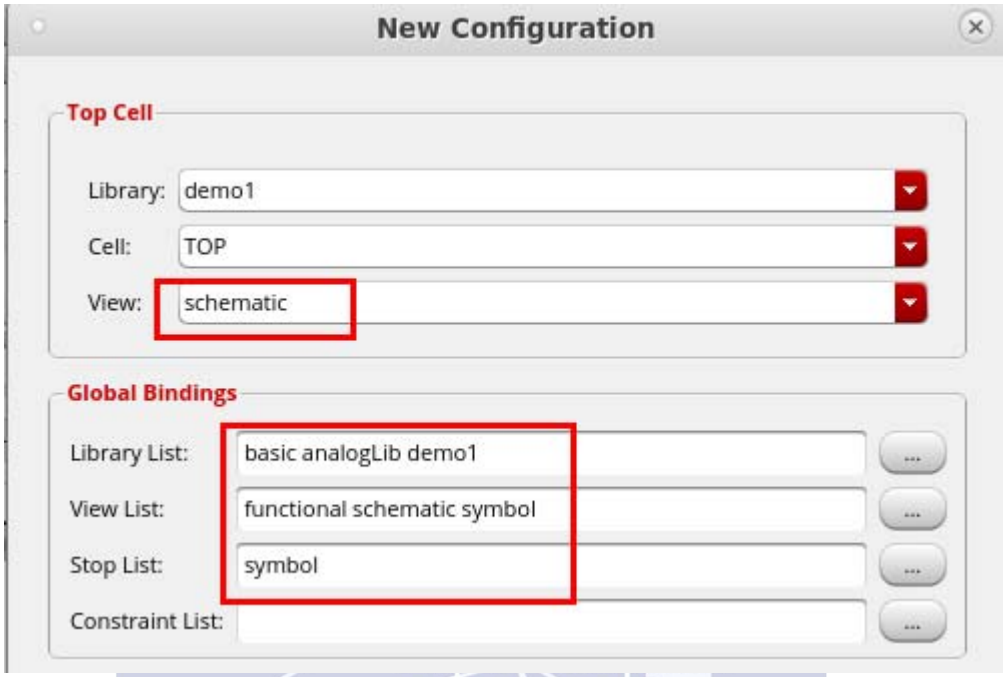


9. In the **Virtuoso Schematic Editor**, we can see that the top-level design is composed of three cells. To perform AMS simulation, we need to setup this schematic by using the **hierarchy editor**. Now, you can close the schematic view.
10. In Library Manger, open ***File -> New -> Cell View***



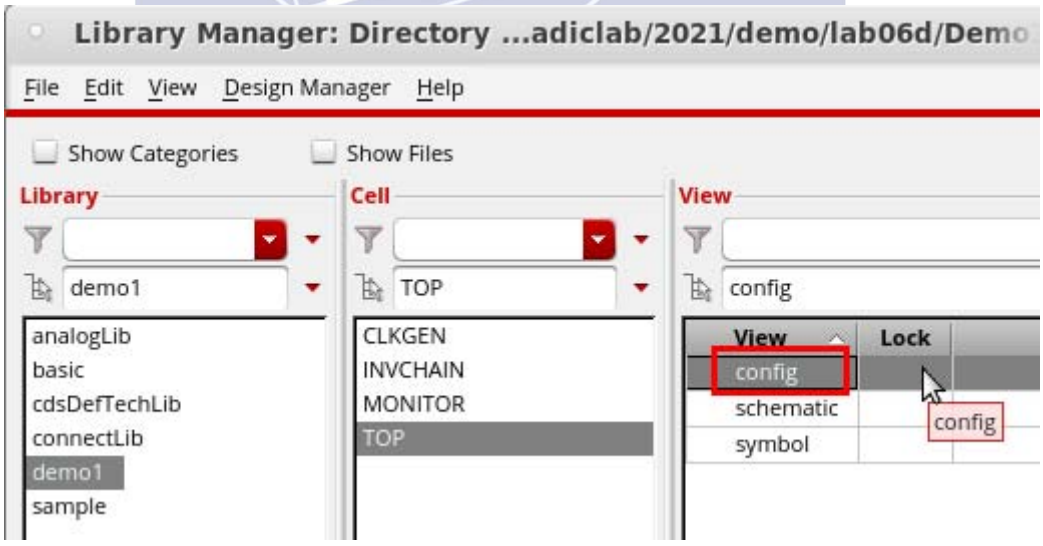
11. In the **New File** tab, fill up the following field:
    a. Library: **demo1**
    b. Cell: **TOP**
    c. View: **config**
    d. Type: **config**
    e. **[Application Tab]** Open with: **Hierarchy-Editor**
    f. Click **OK** button

12. In **New Configuration** window, **[Top Cell]** tab, fill up the following field:
    a. Library: **demo1**
    b. Cell: **TOP**
    c. View: **schematic**
13. In **[Global Bindings]** tab, fill up the following field:
    a. Library List: **basic analogLib demo1**
    b. View List: **functional schematic symbol**
    c. Stop List: **symbol**
    d. Click **OK** button



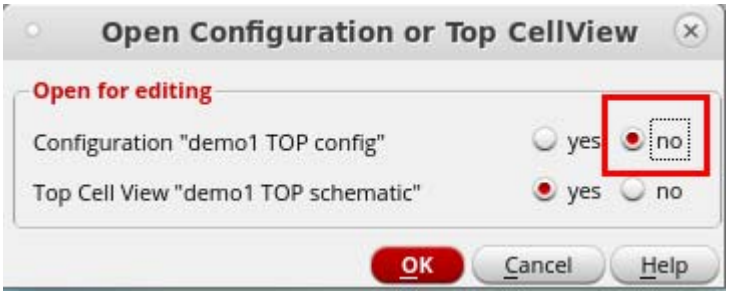
14. In **Virtuoso Hierarchy Editor** window, click on **Save** button and then close the hierarchy editor:

15. From step 10 to step 14, the new **config** view is created.
16. In Library Manger, double click on **config** view of cell **TOP**

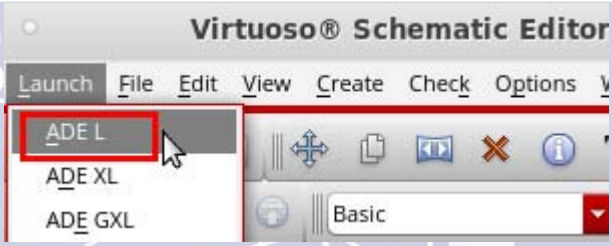


17. An **Open Configuration for Top Cell View** window will ask you that if you want to change the configuration of this design or not. Click **OK** button to open the **config** view. If you want to change the configuration of this design, you can select **yes** button, and modify the configuration in **hierarchy editor**

again.

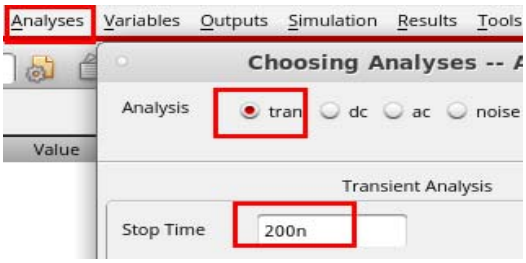


18. In **Virtuoso Schematic Editor** window menu, open ***Launch -> ADE L***. Then Analog Design Environment (ADE-L) will start.

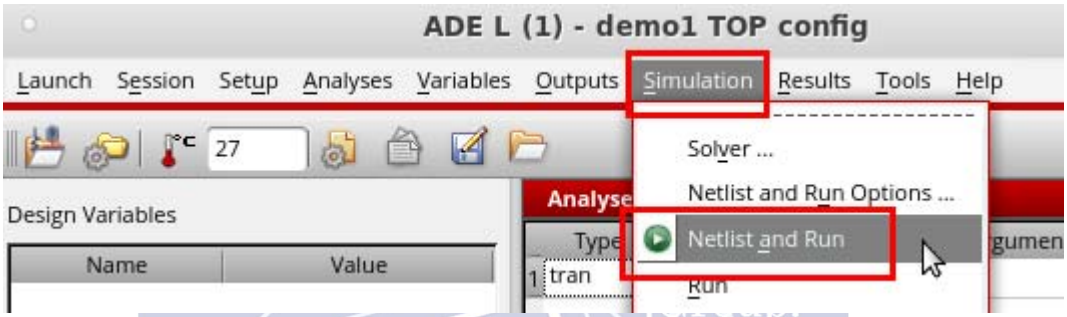


19. In **ADE L** window, open ***Setup -> Simulator/Directory/Host*** . Then fill up the following field:
    a. Simulator: **ams**
    b. Project Directory: **./simulation**
    c. Click **OK** button

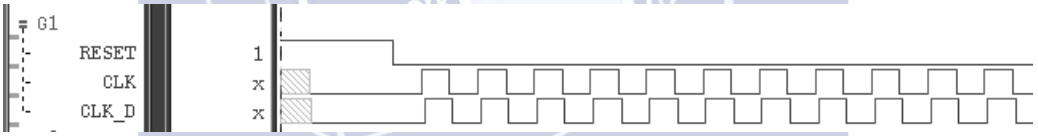
20. In **ADE L** window, open ***Analyses -> Choose***, Then fill up the following field:
    a. Analysis: **tran**
    b. Stop Time: **200n**
    c. Enabled: ☑
    d. Click **OK** button



21. In **ADE L** window, open ***Simulation -> Netlist and Run***, Then AMS simulator will start simulation.



22. After AMS simulation is done, start Verdi to debug the output waveform:
    % nWave &
23. In nWave, open **demo1.vcd** which linked from the **./simulation** directory, and restore the saved signal file **demo1.rc**. Then you can see the simulation results.

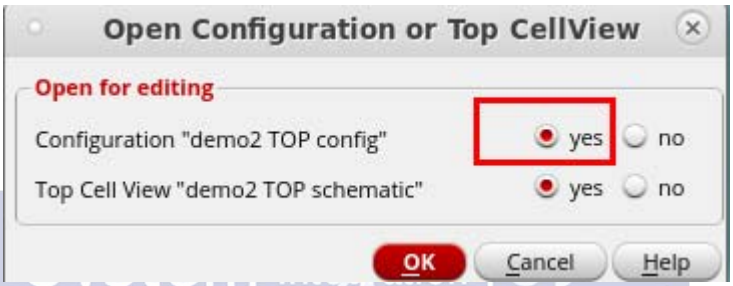


24. Close Virtuoso environment. (Exit virtuoso)

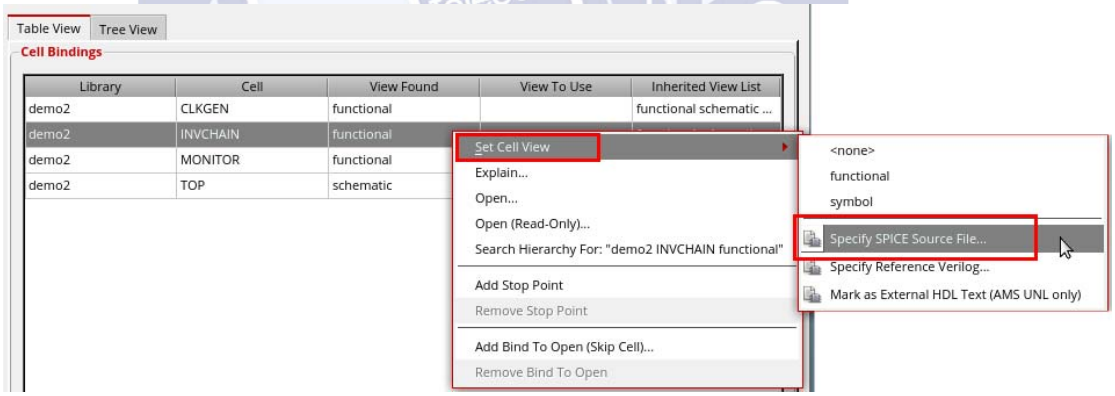
3. Run ADE-L Demo2: Simulation with SPICE File

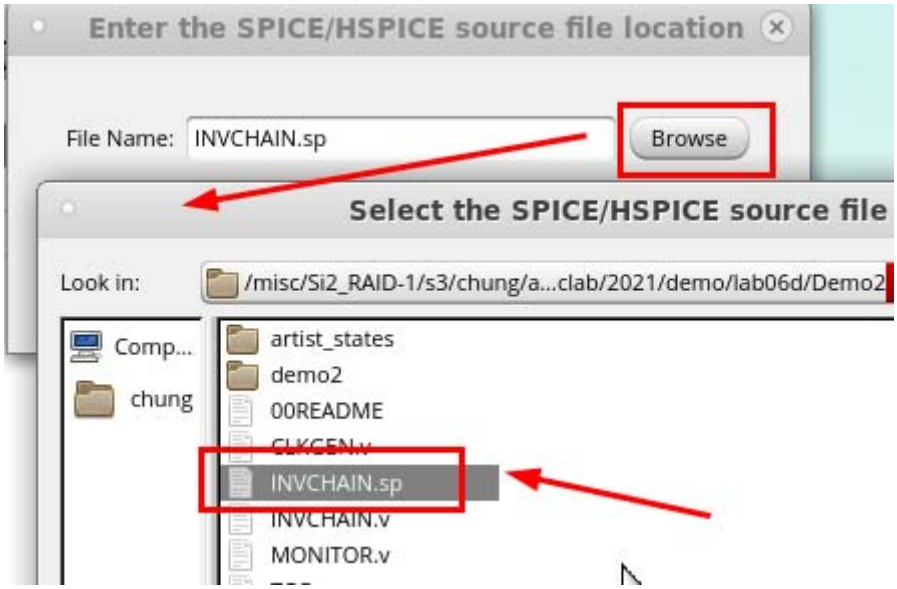
1. Change to directory: **Demo2**
2. Open the spice file for cell: **INVCHAIN**. This spice file will be used in this AMS simulation to replace the **functional** view of cell: **INVCHAIN** in DFII library:
   % gedit INVCHAIN.sp &
3. Start Virtuoso environment:
   % virtuoso &
4. The top-level design for this lab is Library: **demo2**, Cell: **TOP**, View: **schematic**.
5. This design is the same as you done in previous demo1. Thus we already have a **config** view on top level design, and we want to modify it for different simulation condition.

6. In **Library Manger**, double click on **config** view of cell **TOP**
7. In **Open Configuration or Top CellView** window, select **yes** button in **Configuration "demo2 TOP config"**. Click **OK** button. The hierarchical editor will be opened for modification configuration while opening **config** view.



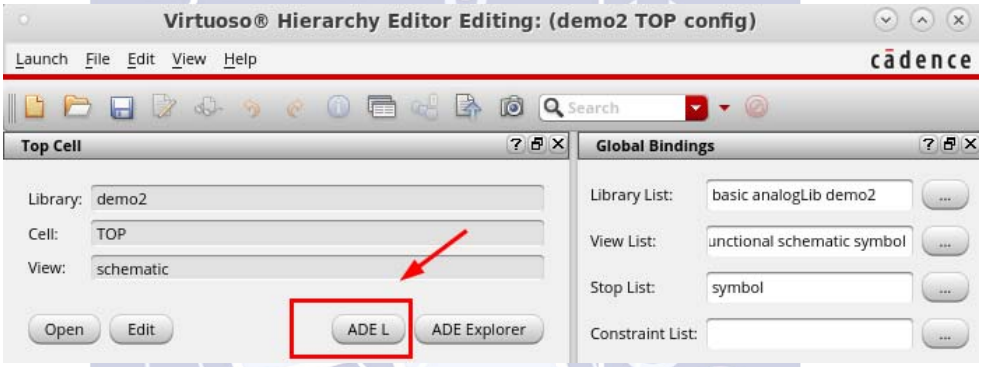
8. In **Virtuoso Hierarchy Editor** window, the default *View Found* of Cell INVCHAIN is **functional** view. Select this cell, and then click your right mouse button to set the cell view to **Specify SPICE Source File**. In **Enter the SPICE/HSPICE source file location** menu, click **Browse** button, and then select **INVCHAIN.sp** file as source file.



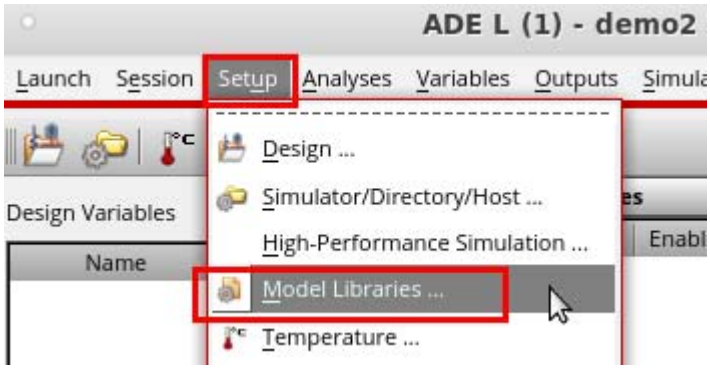


9. In **Virtuoso Hierarchy Editor** window, click on **Save** button then close hierarchy editor:

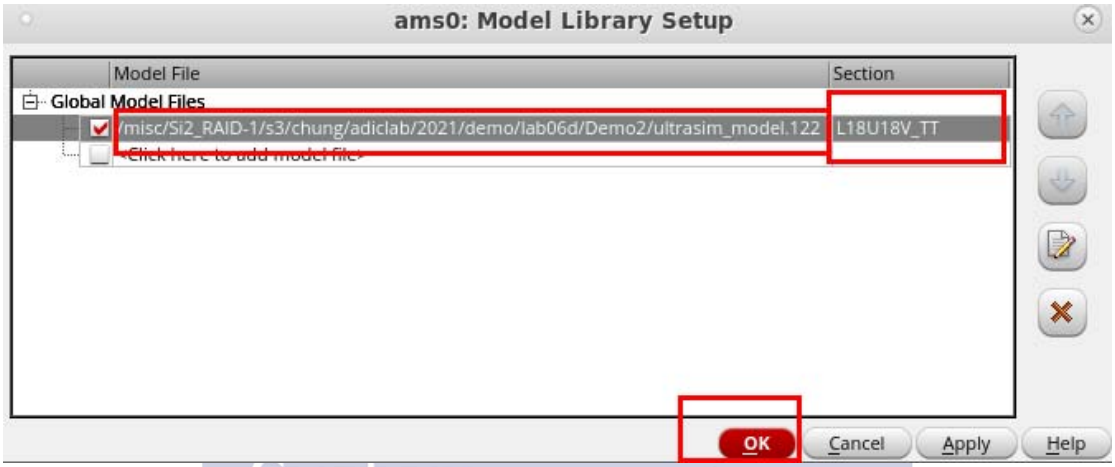
10. In step 8, you select the required SPICE source file of cell: **INVCHAIN** for this simulation.
11. In **Virtuoso Schematic Editor** window menu, open ***Launch -> ADE L***. Then Analog Design Environment (ADE-L) will start. Or you can click on the **ADE-L** button in **Virtuoso Hierarchy Editor** window.



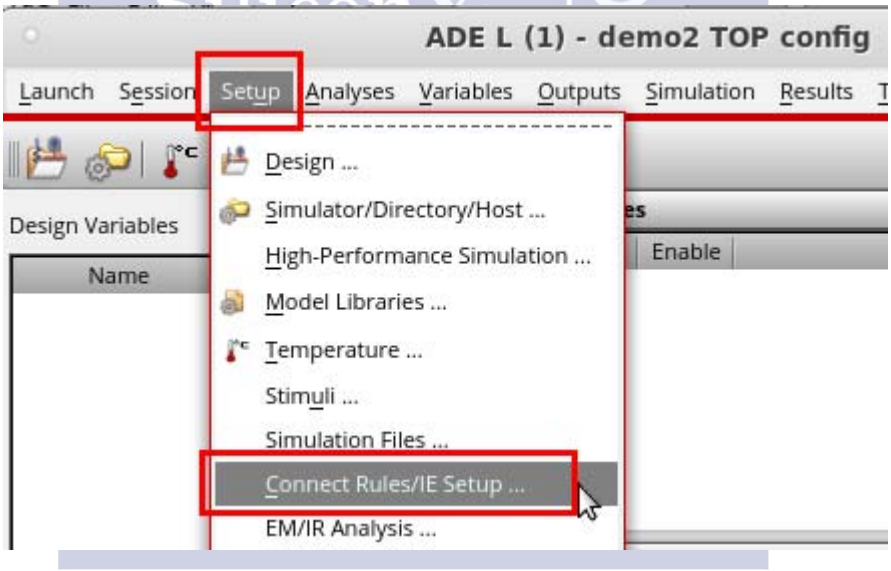
12. In **ADE L** window, open ***Setup -> Simulator/Directory/Host*** . Then fill up the following field:
    a. Simulator: **ams**
    b. Project Directory: **./simulation**
    c. Click **OK** button
13. In **ADE L** window, open ***Setup -> Model Libraries***. Then fill up the following field:

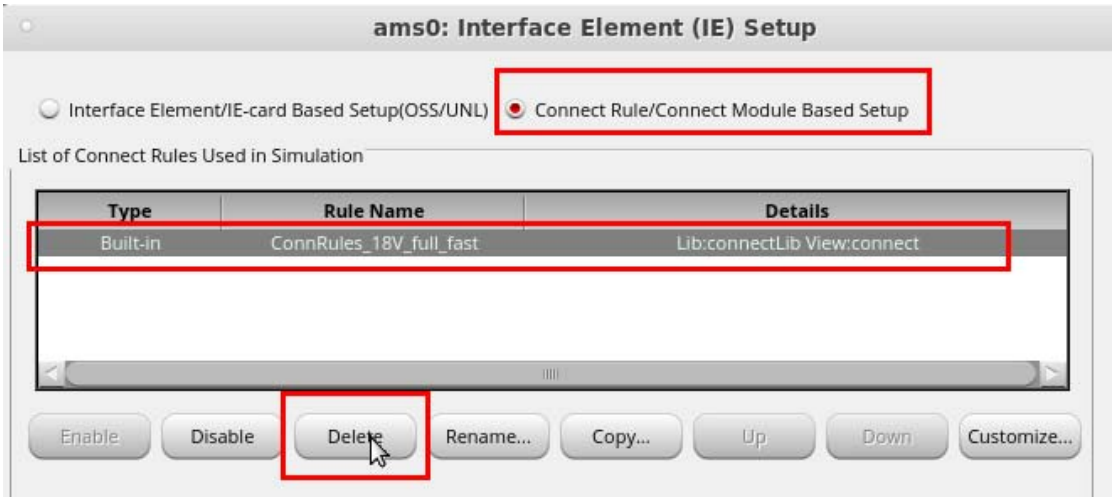


    a. Click on **Browse** button to select the SPICE model file: **ultrasim_model.122**
    b. Section: **L18U18V_TT**
    c. Click **OK** button to add this SPICE model.



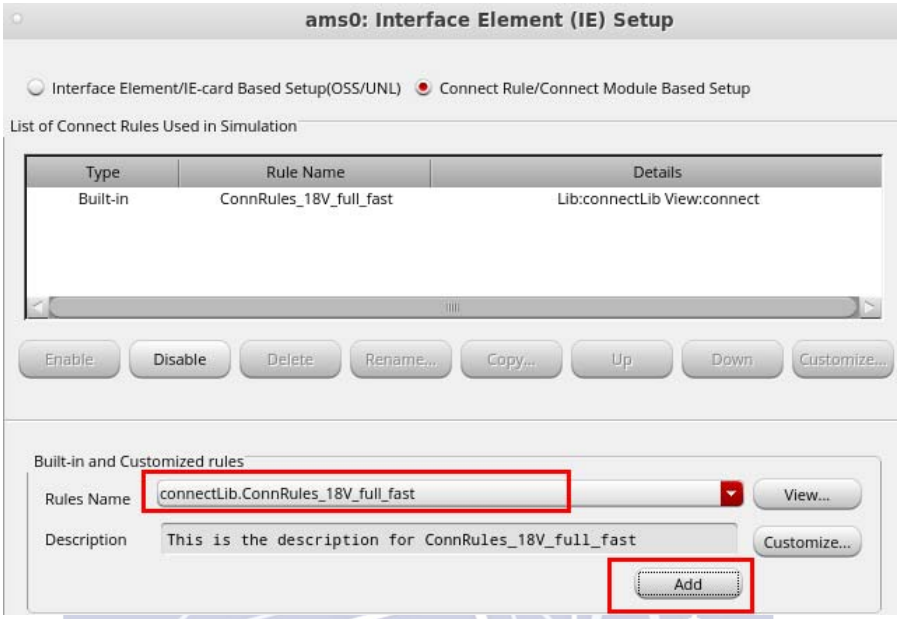
14. In **ADE L** window, open ***Setup -> Connect Rules/IE Setup***. In **Interface Element (IE) Setup** menu, first delete the default connection rule.



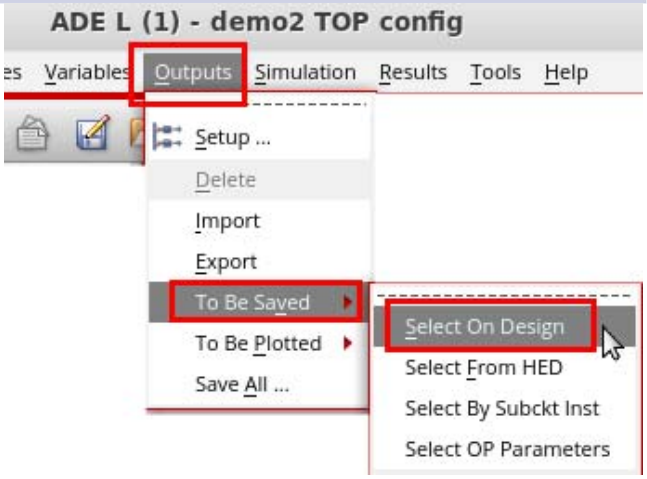


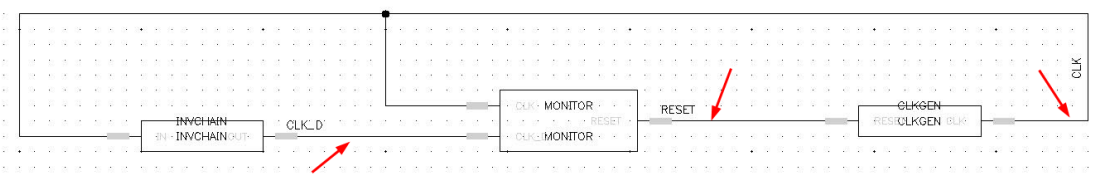
15. Then select Rules Name: **connectLib.ConnRules_18V_full_fast**, and click **Add** button to add 1.8V connection Lib to this simulation. In this simulation, the analog signal in INVCHAIN.sp is 1.8V, thus we use 1.8V connection Lib

to provide digital-to-analog and analog-to-digital conversion between SPICE circuit and verilog models. Click **OK** button and return to **ADE L** window.

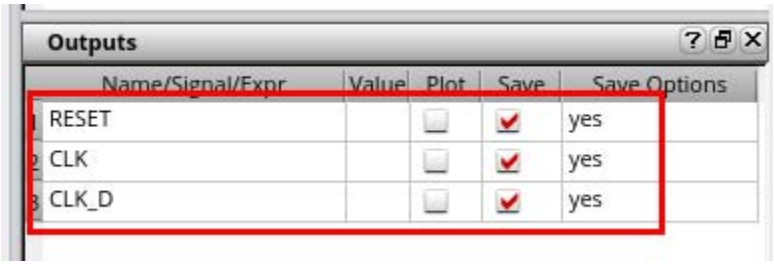


16. In **ADE L** window, open ***Analyses -> Choose***, Then fill up the following field:
    - **a.** Analysis: **tran**
    - **b.** Stop Time: **200n**
    - **c.** Enabled:
    - **d.** Click **OK** button
17. In **ADE L** window, open ***Outputs -> To Be Saved -> Select On Schematic***, then use mouse arrow to click on wire to select **CLK** net ,**CLK_D** net and **RESET** net on the **config** view.

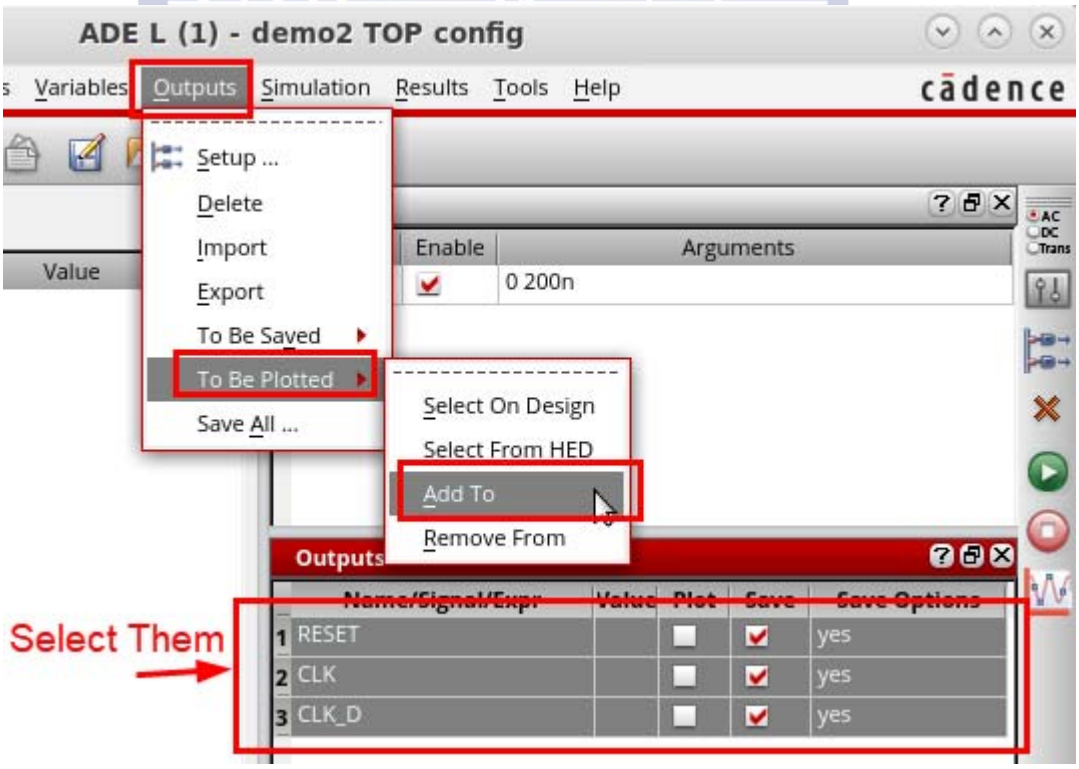




18. In **ADE L** window, the RESET, CLK, and CLK_D signals will be listed in the Outputs to Save list.

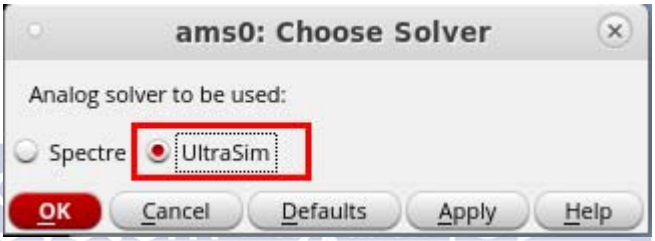


19. In **ADE L** window, select RESET, CLK, and CLK_D, then open ***Outputs -> To Be Plotted -> Add To***, then AMS simulator will save those signals and plotted them after simulation is done.

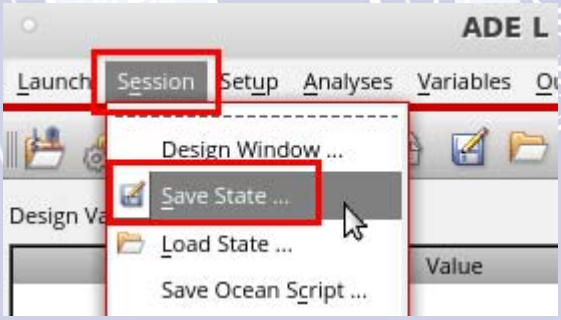


20. In **ADE L** window, the CLK, CLK_D and RESET signals will be listed in the Outputs to Plot and Save list.

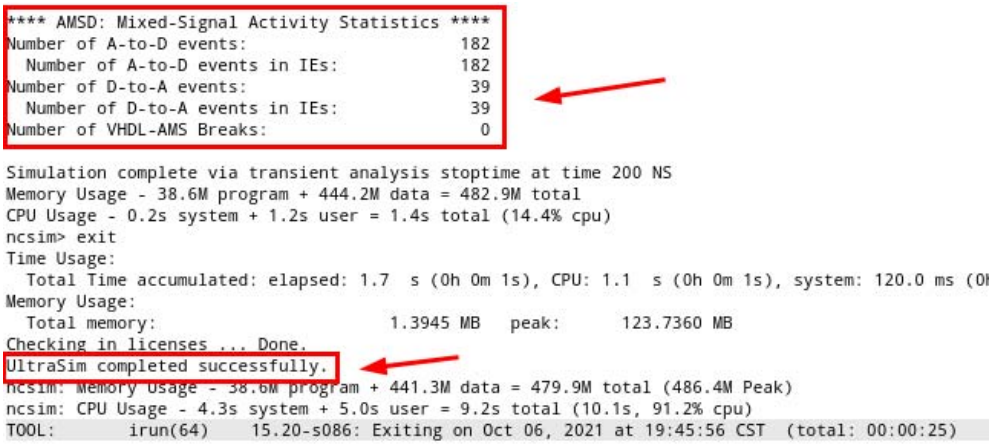
21. In **ADE L** window, open ***Simulation -> Solver***, then select Analog solver to be used: **UltraSim**. We will use UltraSim in this simulation.



22. In **ADE L** window, open ***Session -> Save State***, then fill up the following field:
    - **a.** State Save Directory: **./artist_states**
    - **b.** Save As: **state1**
    - **c.** Click **OK** button
    - **d.** You can restore the setup when next time you re-start the ADE-L.

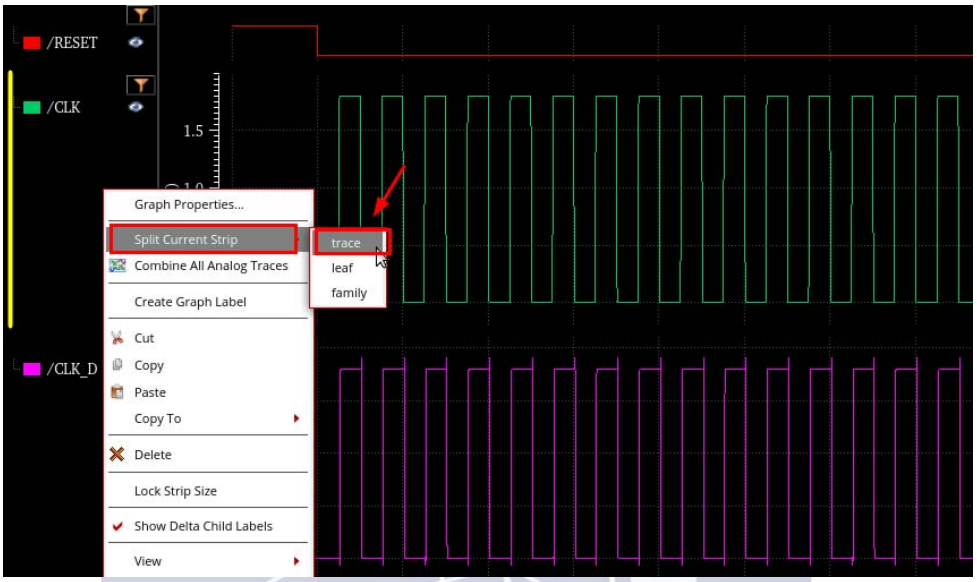


23. In **ADE L** window, open ***Simulation -> Netlist and Run***, then AMS simulator will start to simulation. The simulation log file is shown as follows.

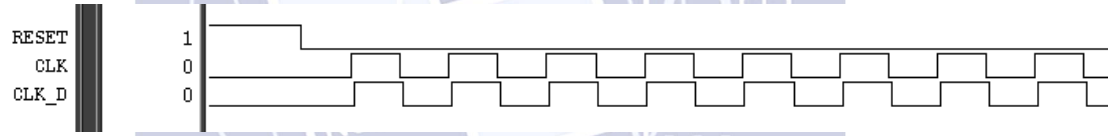


27. After AMS simulation, the plotted analog signals are shown in **Virtuoso Visualization & Analysis XL** window. In waveform viewer, select the panel

combines CLK and CLK_D signals by clicking left mouse button, and then click on your right mouse button to split analog traces.



28. You can also use Verdi to debug the output waveform:
    % nWave &
29. In nWave, open **demo2.vcd**, and restore the save signal file **demo2.rc**. Then you can see the simulation results in digital waveform.

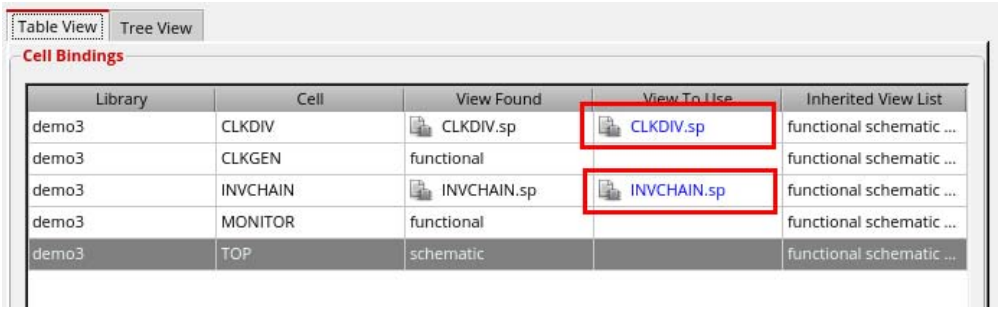


30. Close Virtuoso environment. (Exit virtuoso)

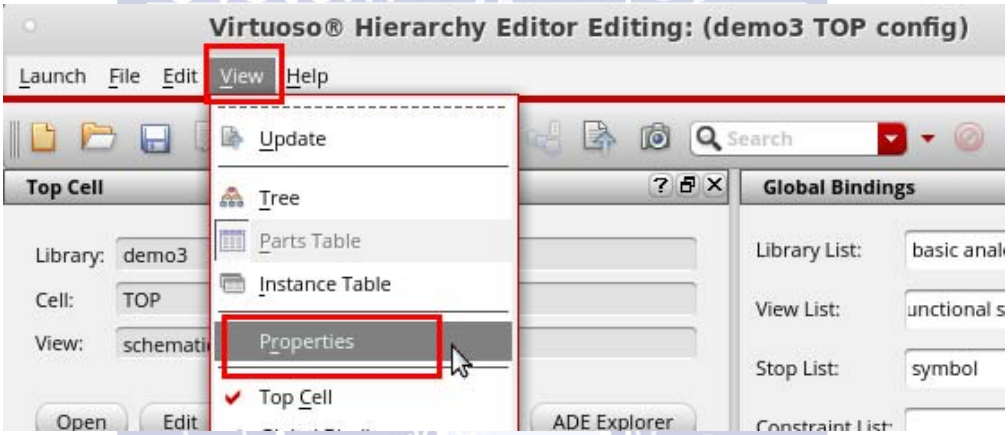
4. Run ADE-L Demo3: SIM_MODE

1. Change to directory: **Demo3**
2. Open and reading the demo3 verilog codes.
   % gedit *.v *.sp &
   This is a simple circuit which uses a behavior model (CLKGEN.v) to generate a 100MHz clock as the reference clock (REF_CLK), and then it is divided by 2 (CLKDIV.v) and is delayed by a delay line which has 0.5ns delay (INVCHAIN.v). The top module in demo3 is TOP (TOP.v), and the MONITOR module (MONITOR.v) is a test module to give reset inputs and dump the digital output waveform.
3. Execute Virtuoso environment to perform AMS simulation of demo3
   % virtuoso &
   A CIW (Command Input Window) is opened, and it creates a log file (CDS.log) in your home directory.
4. In CIW menu, open ***File -> Import -> Verilog***

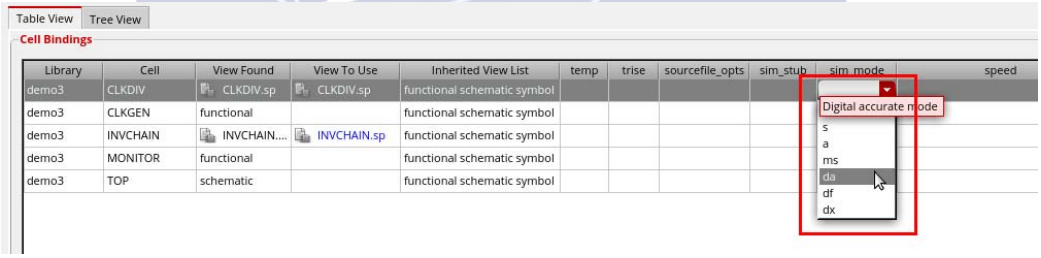
5. In the **Verilog In [Import Options]** tab, fill up the following field:
   a. Verilog Files To Import: **TOP.v**
   b. Target Library Name: **demo3**
6. In the **Verilog In [Global Net Options]** tab, fill up the following field:
   a. Power Net Name: **VDD**
   b. Ground Net Name: **GND**
   c. Click **OK** button
7. In Library Manager, open ***View -> Refresh*** to update the Library list.
8. The top-level design for this lab is Library: **demo3**, Cell: **TOP**, View: **schematic**.
9. In Library Manger menu, open ***File -> New -> Cell View***
10. In the **New File** tab, fill up the following field:
    a. Library: **demo3**
    b. Cell: **TOP**
    c. View: **config**
    d. Type: **config**
    e. **[Application Tab]** Open with: **Hierarchy-Editor**
    f. Click **OK** button
11. In **New Configuration** window, **[Top Cell]** tab, fill up the following field:
    a. Library: **demo3**
    b. Cell: **TOP**
    c. View: **schematic**
12. In **[Global Bindings]** tab, fill up the following field:
    a. Library List: **basic analogLib demo3**
    b. View List: **functional schematic symbol**
    c. Stop List: **symbol**
    d. Click **OK** button
13. From step 9 to step 12, the new **config** view is created.
14. In **Virtuoso Hierarchy Editor** window, the default *View Found* of Cell INVCHAIN is **functional** view. Select this cell, and then click your right mouse button to set the cell view to **Specify SPICE Source File**. In **Enter the SPICE/HSPICE source file location** menu, click **Browse** button, and then select **INVCHAIN.sp** file as source file.
15. In **Virtuoso Hierarchy Editor** window, the default *View Found* of Cell CLKDIV is **functional** view. Select this cell, and then click your right mouse button to set the cell view to **Specify SPICE Source File**. In **Enter the SPICE/HSPICE source file location** menu, click **Browse** button, and then select **CLKDIV.sp** file as source file.



16. In step 14 and step 15, you select the required SPICE source file of cell: **CLKDIV** and **INVCHAIN** for this simulation.
17. In **Virtuoso Hierarchy Editor** window, turn on ***View -> Properties***. Then you will see the property table is shown in hierarchy editor.



18. Select Cell: **CLKDIV**, and then click your right mouse button on **sim_mode** table to set the UltraSIM sim_mode of this cell to **da** .



19. In step 18, you select the required sim_mode only for the cell: **CLKDIV**.
20. In **Virtuoso Hierarchy Editor** window, click on **Save** button then close hierarchy editor:

21. In Library Manger, double click on **config** view of cell **TOP**
22. An **Open Configuration for Top Cell View** window will ask you that if you want to change the configuration of this design or not. Click **OK** button to

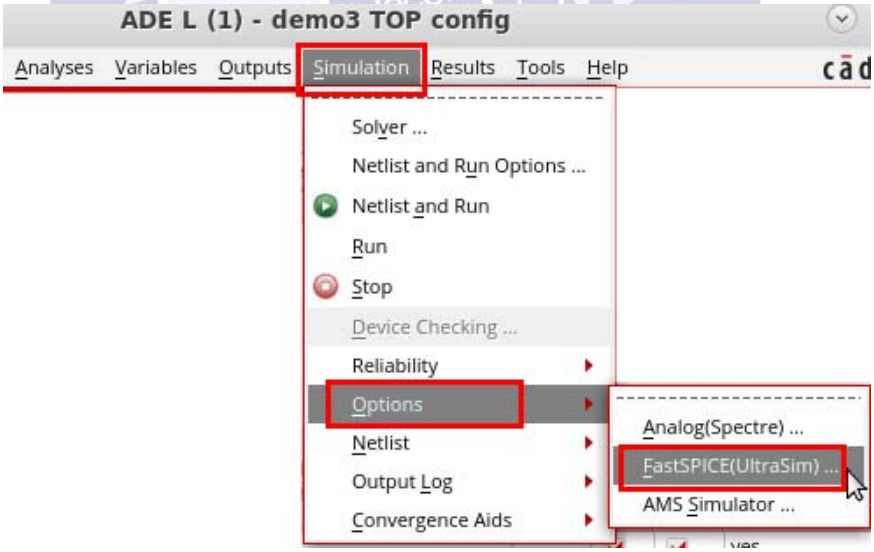
open the **config** view. If you want to change the configuration of this design, you can select **yes** button, and modify the configuration in **hierarchy editor** again.

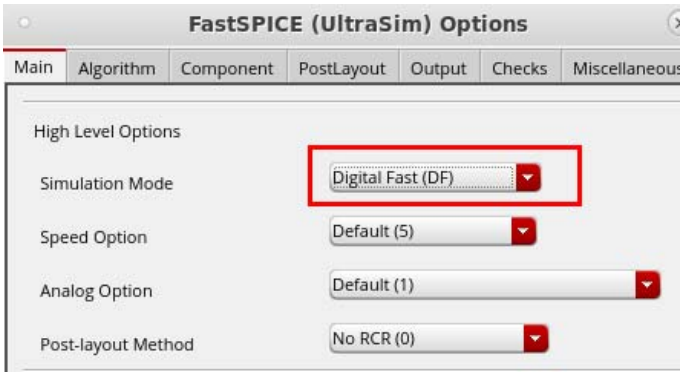
23. In **Virtuoso Schematic Editor** window menu, open ***Launch -> ADE L***. Then Analog Design Environment (ADE-L) will start. Or you can click on the **ADE-L** button in **Virtuoso Hierarchy Editor** window.
24. In **ADE L** window, open ***Setup -> Simulator/Directory/Host*** . Then fill up the following field:
    a. Simulator: **ams**
    b. Project Directory: **./simulation**
    c. Click **OK** button
24. In **ADE L** window, open ***Setup -> Model Libraries***. Then fill up the following field:
    a. Click on **Browse** button to select the SPICE model file: **ultrasim_model.122**
    b. Section: **L18U18V_TT**
    c. Click **OK** button to add this SPICE model.
25. In **ADE L** window, open ***Setup -> Connect Rules/IE Setup***. In **Interface Element (IE) Setup** menu, first delete the default connection rule.
26. Then select Rules Name: **connectLib.ConnRules_18V_full_fast**, and click **Add** button to add 1.8V connection Lib to this simulation. In this simulation, the analog signal in INVCHAIN.sp is 1.8V, thus we use 1.8V connection Lib to provide digital-to-analog and analog-to-digital conversion between SPICE circuit and verilog models. Click **OK** button and return to **ADE L** window.
27. In **ADE L** window, open ***Analyses -> Choose***, Then fill up the following field:
    a. Analysis: **tran**
    b. Stop Time: **600n**
    c. Enabled: 
    d. Click **OK** button
28. In **ADE L** window, open ***Outputs -> To Be Saved -> Select On Schematic***, then use mouse arrow to click on wire to select **CLK** net , **CLK_2** net, **CLK_D** net and **RESET_** net on the **config** view.
29. In **ADE L** window, the RESET_, CLK, CLK_2, and CLK_D signals will be listed in the Outputs to Save list.
30. In **ADE L** window, select RESET_, CLK, CLK_2, and CLK_D, then open ***Outputs -> To Be Plotted -> Add To***, then AMS simulator will save those

signals and plotted them after simulation is done.

31. In **ADE L** window, the RESET_, CLK, CLK_2, and CLK_D signals will be listed in the Outputs to Plot and Save list.

32. In **ADE L** window, open ***Simulation -> Solver***, then select Analog solver to be used: **UltraSim**. We will use UltraSim in this simulation.
33. In ADE, open ***Simulation -> Options -> FastSPICE (Ultrasim)***, then select Simulation Mode: **Digital Fast (DF)**. Here you setup up the default sim_mode in ADE-L simulation, but if in hierarchical editor you specified a different sim_mode for some blocks, ADE-L will follow the property which setup up in hierarchical editor to run simulation of these blocks.





34. In **ADE L** window, open ***Session -> Save State***, then fill up the following field:

a. State Save Directory: **./artist_states**

b. Save As: **state1**

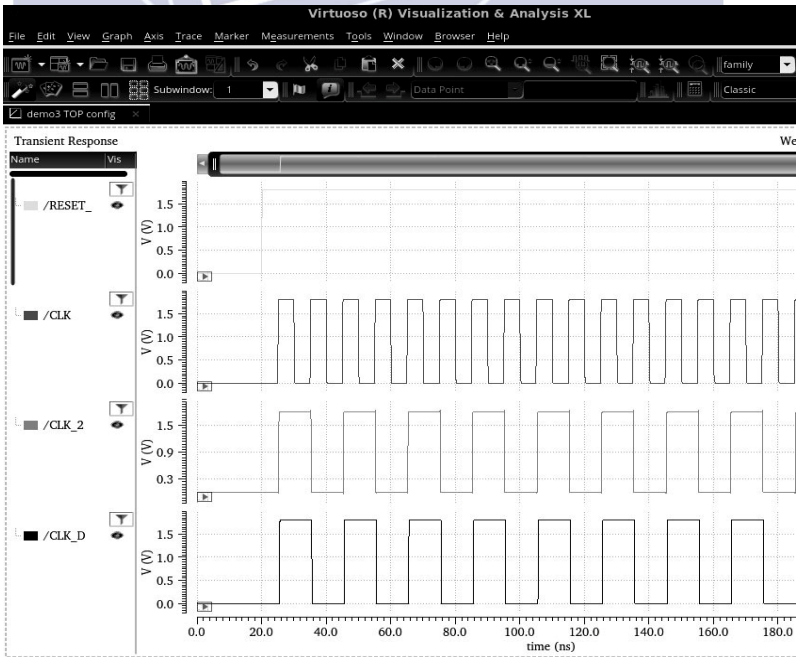
c. Click **OK** button

d. You can restore the setup when next time you re-start the ADE-L.

35. In **ADE L** window, open ***Simulation -> Netlist and Run***, then AMS simulator will start to simulation. The simulation log file is shown as follows.

```
Output System: Time usage: elapsed: 1.2  s (0h 0m 1s), CPU: 0 s
Output System: memory:                0 B   peak:      129.6138

**** AMSD: Mixed-Signal Activity Statistics ****
Number of A-to-D events:                      318
  Number of A-to-D events in IEs:             318
Number of D-to-A events:                       46
  Number of D-to-A events in IEs:              46
Number of VHDL-AMS Breaks:                      0

Time Usage:
  Total Time accumulated: elapsed: 5.4  s (0h 0m 5s), CPU: 2.9
Memory Usage:
  Total memory:                    2.4343 MB   peak:      129
Checking in licenses ... Done.
UltraSim completed successfully.
ncsim: Memory Usage - 38.6M program + 442.4M data = 481.0M total
ncsim: CPU Usage - 4.4s system + 6.6s user = 10.9s total (13.7s,
TOOL:       irun(64)    15.20-s086: Exiting on Oct 06, 2021 at 2
```

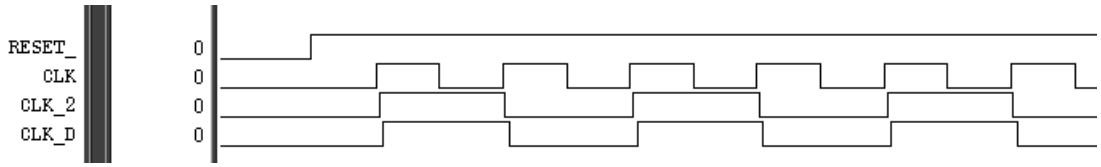
31. After AMS simulation, the plotted analog signals are shown in **Virtuoso Visualization & Analysis XL** window. In waveform viewer, select the panel combines all analog signals by clicking left mouse button, and then click on your right mouse button to split analog traces..



32. After AMS simulation, start Verdi to debug the output waveform:

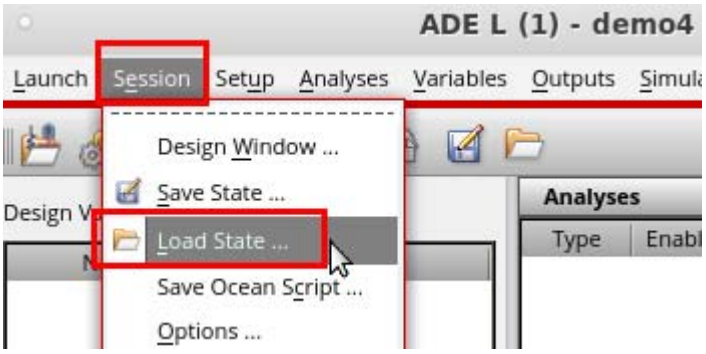
% nWave &

25. In nWave, open **demo3.vcd**, and restore the save signal file **demo3.rc**. Then you can see the simulation results in digital waveform

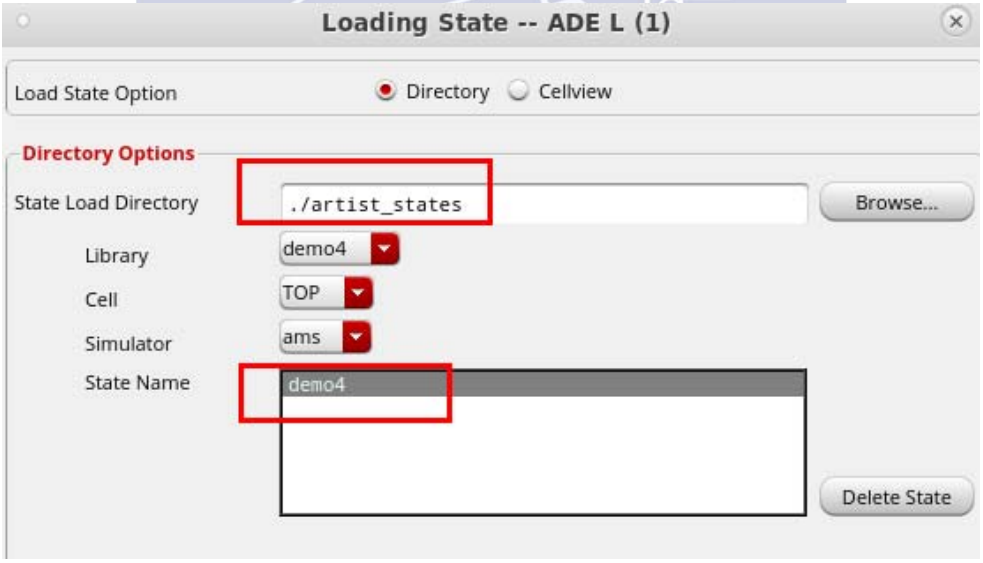


5. Run ADE-L Demo4: Auto Measurement

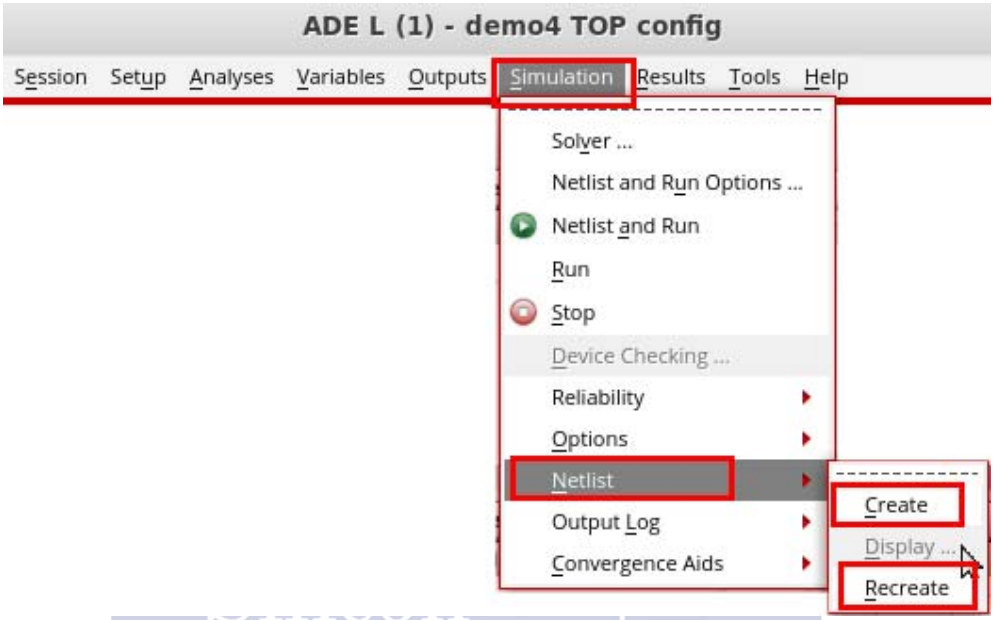
1. Change to directory: **Demo4**
2. Execute Virtuoso environment to perform AMS simulation of demo4
   % virtuoso &
   A CIW (Command Input Window) is opened, and it creates a log file (CDS.log) in your home directory.
3. The top-level design for this lab is Library: **demo4**, Cell: **TOP**, View: **schematic**.
4. This design is the same as you done in previous demo3. Thus we already have a **config** view on top level design.
5. In **Library Manger**, double click on **config** view of cell **TOP**
6. An **Open Configuration for Top Cell View** window will ask you that if you want to change the configuration of this design or not. Click **OK** button to open the **config** view. If you want to change the configuration of this design, you can select **yes** button, and modify the configuration in **hierarchy editor** again.
7. In **Virtuoso Schematic Editor** window menu, open ***Launch -> ADE L***. Then Analog Design Environment (ADE-L) will start.
8. In **ADE L** window, open ***Setup -> Simulator/Directory/Host*** . Then fill up the following field:
   a. Simulator: **ams**
   b. Project Directory: **./simulation**
   c. Click **OK** button.
9. In **ADE L** window, open ***Session -> Load State***. Then fill up the following field:



a. State Load Directory: **./artist_states**
b. Library: **demo4**
c. Cell: **TOP**
d. Simulator: **ams**
e. State Name: **demo4**
f. Click **OK** button.



10. In **ADE L** window, open ***Simulation -> Netlist -> Create***, then the whole design is compiled.
11. In **ADE L** window, open ***Simulation -> Netlist -> Recreate***, then the simulator input control file will be created in spectre format (**amsControlUltraSim.scs**).



12. Open the simulator input file, and include the content of **ams.inc** in the end of this file. Then save this file.

    % gedit amsControlUltraSim.scs &

```
// This is the Cadence AMS Designer(R) analog simulation control file.
// It specifies the options and analyses for the UltraSim analog solver.

simulator lang=spectre

global 0

simulatorOptions options temp=27 tnom=27 scale=1.0 scalem=1.0

// UltraSim Solver Options
usim_opt output_upper=0 ade=1 wf_spectre_syntax=1
usim_opt  sim_mode=df

tran tran stop=600n

finalTimeOP info what=oppoint where=rawfile

wave_out options rawfmt=sst2
```

Add here

13. In demo4, the sim_mode for cell: **CLKDIV** is specified in the input control file. You can also specify the sim_mode for different cell in **Virtuoso Hierarchy Editor** window.

```
// Other options
simulator lang=spice lookup=spectre
*-----------------------------------------------
* UltraSim Solver Options
*-----------------------------------------------
*ultrasim: .usim_opt  wf_format=fsdb
*ultrasim: .usim_opt  wf_tres=1p
*ultrasim: .usim_opt  vdd=1.8
*ultrasim: .usim_opt  vh=0.9
*ultrasim: .usim_opt  vl=0.9

*ultrasim: .usim_opt sim_mode=da TOP.CLKDIV
```

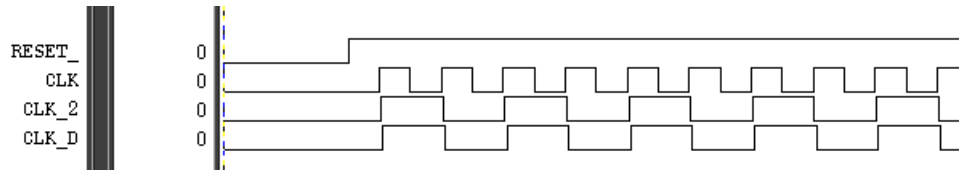
14. In **ADE L** window, open ***Simulation -> Run***, then AMS simulator will start simulation. Note, **YOU CAN'T USE "Netlist and Run" to start ADE-L simulation**, or you will overwrite the simulator input control file which you just modified (**amsControlUltraSim.scs**).
15. After AMS simulation, the simulation log file is shown as follows. First, you can find the user option which specified in **amsControlUltraSim.scs**. Also, in the end of the simulation log file, the activities between VERILOG and SPICE cells are shown, and then the AMS simulation is completed.

```
User Option Summary:
  wf_format = fsdb
  tnom = 27 scale = 1 scalem = 1
  output_upper = 0 ade = 1 wf_spectre_syntax = 1
  sim_mode = df
  wf_tres = 1e-12
  vdd = 1.8
  vh = 0.9
  vl = 0.9
  sim_mode = da  TOP.CLKDIV
Total Options statements: 9

Output System: Time usage: elapsed: 400.0 ms (0h 0m 0s), CPU: 0 s
Output System: memory:                0 B   peak:      132.8087 MB

**** AMSD: Mixed-Signal Activity Statistics ****
Number of A-to-D events:                    317
  Number of A-to-D events in IEs:           317
Number of D-to-A events:                     46
  Number of D-to-A events in IEs:            46
Number of VHDL-AMS Breaks:                    0

Time Usage:
  Total Time accumulated: elapsed: 5.3  s (0h 0m 5s), CPU: 3.4  s
Memory Usage:
  Total memory:                   7.0585 MB   peak:      132.8
Checking in licenses ... Done.
UltraSim completed successfully.
ncsim: Memory Usage - 38.6M program + 445.8M data = 484.5M total (
ncsim: CPU Usage - 4.9s system + 7.6s user = 12.5s total (15.2s, 8
TOOL:       irun(64)    15.20-s086: Exiting on Oct 07, 2021 at 08:
```

16. Start Verdi to debug the output waveform:

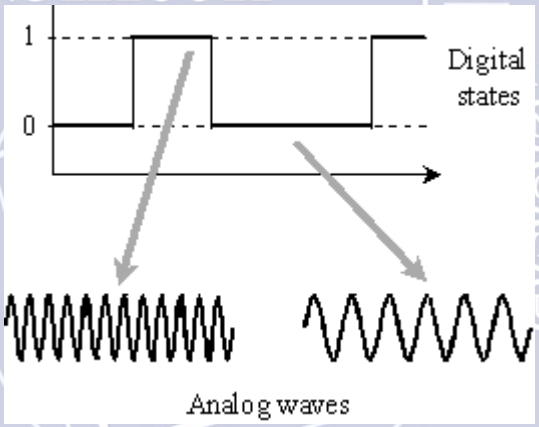
    % nWave &

17. In nWave, open **spiceModels.fsdb**, and restore the save signal file **demo4.rc**. Then you can see the simulation results in digital waveform.



18. Open the ADE-L measurement result file (**spiceModels.meas0**). In this file, you can see that the output clock period (**CLK_D**) measurement results.
    % gedit spiceModels.meas0 &
19. Close Virtuoso environment. (Exit virtuoso)

6. Design a Frequency Shift Keying (FSK) Modem



1. Frequency Shift Keying (FSK) is a method of transmitting digital signals. The two binary states, logic 0 (low) and 1 (high), are each represented by an analog waveform. Logic 0 is represented by a wave at a specific frequency: f1, and logic 1 is represented by a wave at different frequency: f2. A modem converts the binary data into analog waves for transmission over cables or wireless media.
2. In this exercise, only the transmitter part of FSK modem is designed.
3. Change to directory: **Exercise**
4. Open TOP level design of this circuit.
   % gedit *.v &
   In top-level of this circuit (TOP.v), a FSK modem (FSK_MODEM.v) and a MONITOR module (MONITOR.v) are instantiated. The MONITOR module is a test module to give reset inputs and data inputs for the FSK modem. And it also dumps the digital output waveform. The FSK modem converts digital input to frequency output.
5. Design a FSK modem which meets the following requirements:

a. Please use the DCO circuits which you designed in the **lab05b** to build-up this FSK modem.

b. The input ports of FSK_MODEM are RESET, TX_CLK and TX_DATA.

c. The output port of FSK_MODEM is FSK_OUT.

d. The sample output waveform of this lab is shown in the below figure.

e. When TX_DATA=1, FSK_OUT outputs the DCO highest frequency output, and when TX_DATA=0, FSK_OUT outputs the DCO lowest frequency output. You should use the positive edge of TX_CLK to sample the TX_DATA, and then converts it to FSK output (FSK_OUT).

f. You must perform AMS (ADE-L) simulation to simulate this FSK modem. The DCO is a SPICE circuit, and the other part of FSK modem is all-digital behavior Verilog code. In AMS (ADE-L) simulation, it only need to use sim_mode=DF in this lab.