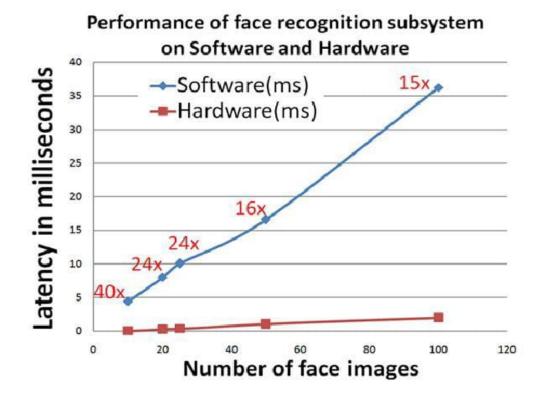
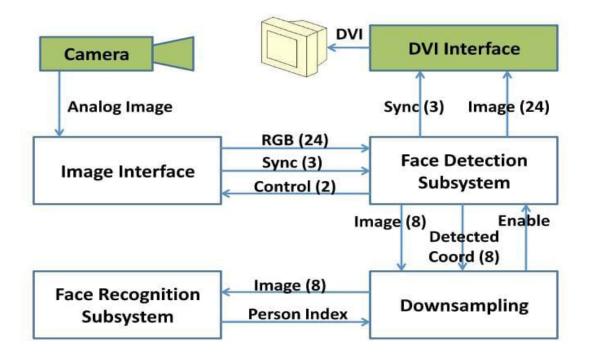
IMAGE RECOGNITION WITH IBM CLOUD VISUAL RECOGNITION INNOVATION

IMPLEMENTATION OF THE COMPLETE FACE RECOGNITION SYSTEM:

In this section, we present the downsampling module used to connect the detection and the recognition subsystems. Then we describe the complete face recognition system



Performance comparisons between software and hardware implementations of the face recognition subsystem.

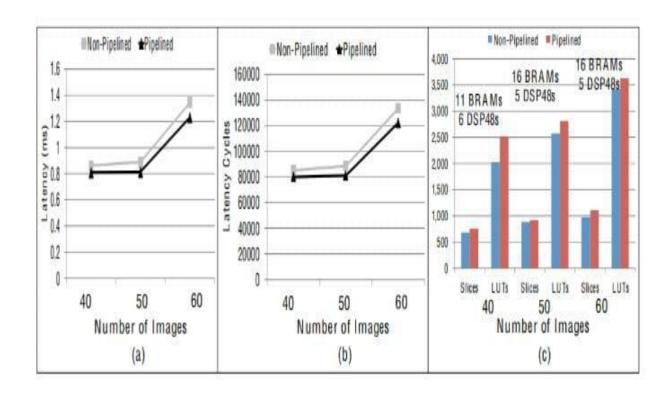


The architecture for the complete face recognition system consisting of the face detection and face recognition subsystems

Which is a combination of all of these subsystems. provides an overview of the architecture for the completeface recognition system. The downsampling module is notified when a face is detected by the face detection subsystem. After being notified, the downsampling module reads the face image data using the coordinates, width and height given by the face detection subsystem. According to the size of the detected face image data, the downsampling module reduces the detected faceto 20×20 and sends these 400 pixel values to the face recognition subsystem. The downsampling module resizes each detected face so that they are suitable as input into the face recognition subsystem.

We introduce a factor which is used to calculate how many pixels we should skip in order to downsample a x×x image into a 20 × 20 image. The factor depends on the size of detected face. For instance, if the size of the detected face is 60 × 60, then the factor would be 3. We can find the factor using f actor = detected f ace size/20. Finally, when the detected face is appropriately downsampled, the downsampling module checks if the face recognition subsystem is available, it reads 20 × 20 image and returns the index of a person which belongs to the detected face. According to the returned index of a person, we draw a box around the detected face with predefined color. Each individual's face in the set is represented by an index and each index is associated with a color.

The implementation was simulated/verified with ModelSim, and then implemented on a Virtex-5 FPGA. Table I shows the device utilization of the complete face recognition system on a Virtex-5 FPGA board. According to the experimental results, the complete face recognition system runs at 45 frames per second on VGA data.



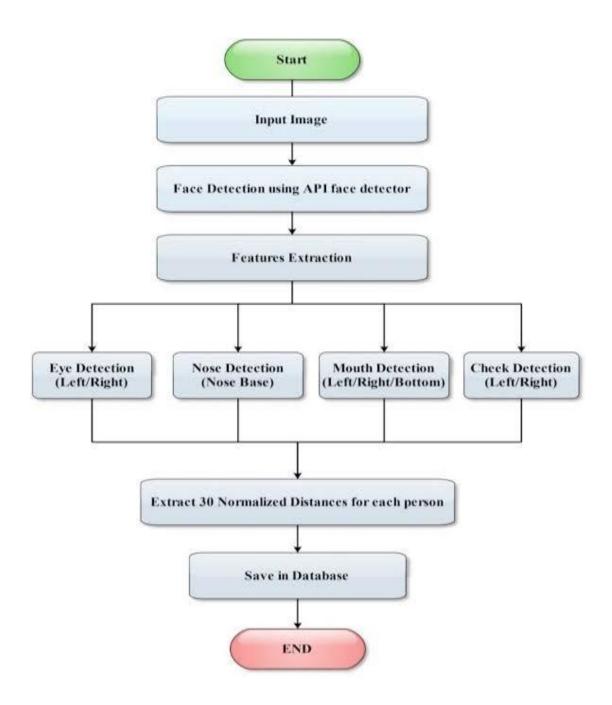
Part (a) shows the latency of our face recognition subsystem implementation results on an FPGA in milliseconds using both pipelined and non-pipelined implementations. Part (b) shows the latency cycles for pipelined and non-pipelined implementations. Part (c)show the device utilization summary for the number of slices, LUTs, block RAMs (BRAMs) and DSP48s for both pipelined and non-pipelined implementations.

DESIGN FOR IMAGE RECOGNITION:

The module consists of a face recognition system that uses KNN algorithm to find the closest probability to face acquired from the live feed. This system breaks the live feed into frames and each frame is applied to face detection process. The face detection process is used to identify a person by comparing the acquired face to the directory. The faces of the acquaintance stored in the directory is broken down to points and the points cumulatively provides the value to that person. By machine learning algorithm this data is trained to the system.

For the same person many images are feed to the machine as a training set by thoroughly studying each angle of the image and deriving a value for the face we

can uniquely identify a particular person with a maximum probability of correctness . The data obtained is transformed into audio file that is the final output of the proposed system presented to the visually impaired person . The heed by the visually impaired person through a microphone or a speaker.





The above mentioned survey results have some limitations like cost and network coverage. The cost of installing and maintaining the network is very high comparatively. Not only the network maintenance but also the coverage of the methodology is limited. So our project overcomes all the limitations of the existing systems and increases the overall performance comparatively.