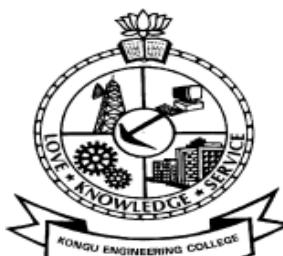


# KONGU ENGINEERING COLLEGE

(Autonomous Institution Affiliated to Anna University, Chennai)

PERUNDURAI ERODE – 638 060

TAMILNADU INDIA



Estd : 1984

## REGULATIONS, CURRICULUM & SYLLABI – 2024

(CHOICE BASED CREDIT SYSTEM AND  
OUTCOME BASED EDUCATION)

(For the students admitted from the academic year 2024 - 2025 )

### MASTER OF ENGINEERING DEGREE IN VLSI DESIGN

### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



**M.E. VLSI DESIGN CURRICULUM – R2024**  
**(For the candidates admitted in the academic year 2024-25 onwards)**

SEMESTER – I														
Course Code	Course Title	Hours / Semester						Credit	Maximum Marks			Category	Type	
		CI		LI	TW	SL	TH		CA	ESE	Total			
		L	T	P										
<b>Theory/Theory with Practical</b>														
24AMT12	Applied Mathematics for Electronics Engineers	45	15	0	60	0	120	4	40	60	100	FC	A	
24GET11	Introduction to Research	30	15	0	45	0	90	3	40	60	100	FC	C	
24VLT11	Advanced Digital System Design	45	15	0	60	0	120	4	40	60	100	PC	A	
24VLT12	VLSI Design Techniques	45	0	0	45	0	90	3	40	60	100	PC	C	
24VLT13	HDL for IC Design	45	0	0	45	0	90	3	40	60	100	PC	S	
24VLT14	Device Modeling	45	0	0	45	0	90	3	40	60	100	PC	C	
<b>Practical / Employability Enhancement</b>														
24VLL11	VLSI Design Laboratory	0	0	0	30	0	30	1	60	40	100	PC		
24VLL12	HDL for IC Design Laboratory	0	0	0	30	0	30	1	60	40	100	PC		
<b>Total Credits to be earned</b>									<b>22</b>					

CI – Classroom Instructions, LI – Laboratory Instructions, TW – Term Work, SL – Self Learning, L – Lecture, T – Tutorial, P – Practical, C – Credit, TH – Total Hours, CA – Continuous Assessment, ESE – End Semester Examination

Type: A – Analytical, D – Design using Hardware, S – Simulation using Coding, C – Concept, OC – Online course, OT - others

	
Signature of the Chairman Board of Studies - <b>ECE</b>	

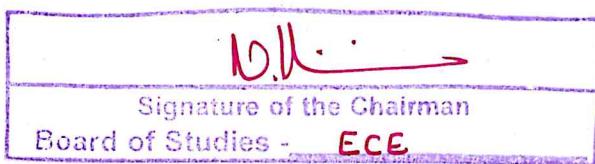


**M.E. VLSI DESIGN CURRICULUM – R2024**  
**(For the candidates admitted in the academic year 2024-25 onwards)**

SEMESTER – II														
Course Code	Course Title	Hours / Semester						Credit	Maximum Marks			Category	Type	
		CI		LI	TW	SL	TH		CA	ESE	Total			
		L	T	P										
<b>Theory/Theory with Practical</b>														
24VLT21	Analog Integrated Circuits	45	0	0	45	0	90	3	40	60	100	PC	C	
24VLT22	Application Specific Integrated Circuits	45	0	0	45	0	90	3	40	60	100	PC	C	
24VLT23	VLSI Signal Processing	45	15	0	60	0	120	4	40	60	100	PC	A	
	Professional Elective - I	45	0	0	45	0	90	3	40	60	100	PE	C	
	Professional Elective - II	45	0	0	45	0	90	3	40	60	100	PE	C	
	Professional Elective - III	45	0	0	45	0	90	3	40	60	100	PE	C	
<b>Practical / Employability Enhancement</b>														
24VLL21	Analog Integrated Circuits Laboratory	0	0	0	30	0	30	1	60	40	100	PC		
24VLL22	Application Specific Integrated Circuits Laboratory	0	0	0	30	0	30	1	60	40	100	PC		
<b>Total Credits to be earned</b>									<b>21</b>					

CI – Classroom Instructions, LI – Laboratory Instructions, TW – Term Work, SL – Self Learning, L – Lecture, T – Tutorial, P – Practical, C – Credit, TH – Total Hours, CA – Continuous Assessment, ESE – End Semester Examination

Type: A – Analytical, D – Design using Hardware, S – Simulation using Coding, C – Concept, OC – Online course, OT - others

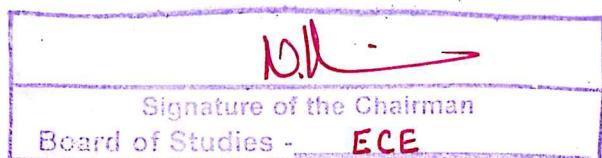


**M.E. VLSI DESIGN CURRICULUM – R2024**  
**(For the candidates admitted in the academic year 2024-25 onwards)**

SEMESTER – III														
Course Code	Course Title	Hours / Semester						Credit	Maximum Marks			Category	Type	
		CI		LI	TW	SL	TH		CA	ESE	Total			
		L	T	P										
<b>Theory/Theory with Practical</b>														
	Professional Elective - IV	45	0	0	45	0	90	3	40	60	100	PE		
	Professional Elective - V	45	0	0	45	0	90	3	40	60	100	PE		
	Professional Elective - VI	45	0	0	45	0	90	3	40	60	100	PE		
<b>Practical / Employability Enhancement</b>														
24VLP31	Project Work - I	0	0	240	0	0	240	8	50	50	100	EC		
<b>Total Credits to be earned</b>								<b>17</b>						

CI – Classroom Instructions, LI – Laboratory Instructions, TW – Term Work, SL – Self Learning, L – Lecture, T – Tutorial, P – Practical, C – Credit, TH – Total Hours, CA – Continuous Assessment, ESE – End Semester Examination

Type: A – Analytical, D – Design using Hardware, S – Simulation using Coding, C – Concept, OC – Online course, OT - others



**M.E. VLSI DESIGN CURRICULUM – R2024**  
**(For the candidates admitted in the academic year 2024-25 onwards)**

SEMESTER – IV															
Course Code	Course Title	Hours / Semester							Credit	Maximum Marks			Category	Type	
		CI		LI	TW	SL	TH	CA		ESE	Total				
		L	T	P											
<b>Practical / Employability Enhancement</b>															
24VLP41	Project Work - II	0	0	360	0	0	360	12	50	50	100	EC			
<b>Total Credits to be earned</b>									<b>12</b>						

CI – Classroom Instructions, LI – Laboratory Instructions, TW – Term Work, SL – Self Learning, L – Lecture, T – Tutorial, P – Practical, C – Credit, TH – Total Hours, CA – Continuous Assessment, ESE – End Semester Examination

Type: A – Analytical, D – Design using Hardware, S – Simulation using Coding, C – Concept, OC – Online course, OT - others

**Total Credits : 72**


Signature of the Chairman
Board of Studies - <b>ECE</b>



**M.E. VLSI DESIGN CURRICULUM – R2024**  
**(For the candidates admitted in the academic year 2024-25 onwards)**

LIST OF PROFESSIONAL ELECTIVE COURSES																					
S. No.	Course Code	Course Title	Hours / Week						Credit	Maximum Marks			Cate gory	Type							
			CI		LI	TW	SL	TH		CA	ESE	Total									
			L	T	P																
<b>SEMESTER - II</b>																					
<b>ELECTIVE – I</b>																					
1	24VLE01	Testing of VLSI Circuits	45	0	0	45	0	90	3	40	60	100	PE	C							
2	24VLE02	Semiconductor Memory Design	45	0	0	45	0	90	3	40	60	100	PE	C							
3	24VLE03	Quantum Computing	45	0	0	45	0	90	3	40	60	100	PE	C							
<b>ELECTIVE – II</b>																					
4	24VLE04	Low Power VLSI Design	45	0	0	45	0	90	3	40	60	100	PE	C							
5	24VLE05	Mixed Signal VLSI Design	45	0	0	45	0	90	3	40	60	100	PE	C							
6	24VLE06	RF Circuit Design	45	0	0	45	0	90	3	40	60	100	PE	C							
<b>ELECTIVE – III</b>																					
7	24VLE07	Computer Aided Design of VLSI Circuits	45	0	0	45	0	90	3	40	60	100	PE	C							
8	24VLE08	System on Chip	45	0	0	45	0	90	3	40	60	100	PE	C							
9	24VLE09	Hardware Software Co-Design	45	0	0	45	0	90	3	40	60	100	PE	C							

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Type: A – Analytical, D – Design using Hardware, S – Simulation using Coding, C – Concept, OC – Online course, OT - others

	
Signature of the Chairman	
Board of Studies -	ECE

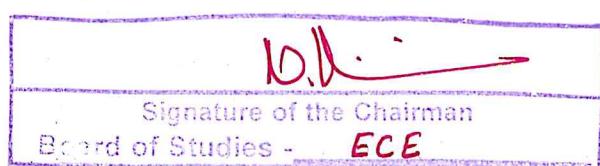


**M.E. VLSI DESIGN CURRICULUM – R2024**  
**(For the candidates admitted in the academic year 2024-25 onwards)**

S. No	Course Code	Course Title	Hours / Week					Credit	Maximum Marks			Category	Type							
			CI		LI	TW	SL	TH	CA	ESE	Total									
			L	T	P															
<b>SEMESTER – III</b>																				
<b>ELECTIVE – IV</b>																				
10	24VLE10	Network on Chip	45	0	0	45	0	90	3	40	60	100	PE	C						
11	24VLE11	Reconfigurable Architectures for VLSI	45	0	0	45	0	90	3	40	60	100	PE	C						
12	24VLE12	Hardware Security	45	0	0	45	0	90	3	40	60	100	PE	C						
<b>ELECTIVE – V</b>																				
13	24VLE13	Functional Verification Using HDL	45	0	0	45	0	90	3	40	60	100	PE	C						
14	24VLE14	VLSI for IOT Systems	45	0	0	15	30	90	3	40	60	100	PE	OC						
15	24VLE15	VLSI for Biomedical Applications	45	0	0	45	0	90	3	40	60	100	PE	C						
<b>ELECTIVE – VI</b>																				
16	24VLE16	VLSI Technology	45	0	0	45	0	90	3	40	60	100	PE	C						
17	24VLE17	Supervised Machine Learning Algorithms	45	0	0	45	0	90	3	40	60	100	PE	C						
18	24VLE18	Genetic Algorithms and Its Applications	45	0	0	45	0	90	3	40	60	100	PE	C						
19	24GET13	Innovation Entrepreneurship and Venture Development	45	0	0	45	0	90	3	40	60	100	PE	C						

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Type: A – Analytical, D – Design using Hardware, S – Simulation using Coding, C – Concept, OC – Online course, OT – others





24AMT12 – APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	1	PC	45	15	0	60	120	3	
Preamble	This course will demonstrate various analytical skills in applied mathematics and use extensive mathematical tools such as linear programming, matrix factorizations and queuing theory with the tactics of problem solving and logical thinking applicable in electronics engineering.									
Unit – I	<b>Advanced Matrix Theory:</b> Positive definite matrices – Cholesky decomposition – Generalized Eigenvectors – QR factorization – Generalized inverses – Singular value decomposition – Least squares solution.									
Unit – II	<b>Vector Spaces:</b> Vector Space – Subspaces – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.									
Unit – III	<b>Linear Programming:</b> Mathematical Formulation of LPP – Basic definitions – Solutions of LPP: Graphical method – Simplex method – Transportation Model – Mathematical Formulation – Initial Basic Feasible Solution: North west corner rule – Vogel's approximation method – Optimum solution by MODI method – Assignment Model – Mathematical Formulation – Hungarian algorithm.									
Unit – IV	<b>Non-Linear Programming:</b> Introduction – Mathematical formulation of Non-linear programming problems – Non-linear programming problem with equality constraints – Lagrange multipliers method – Non-linear programming problem with inequality constraint – Kuhn Tucker conditions.									
Unit – V	<b>Queuing Theory:</b> Introduction - Characteristics of a queueing system – Kendall's notation – Little's formula - Queueing model I ( Infinite capacity single server Poisson queue model) (M/M/1) : ( $\infty$ /FIFO) – Little's formulae – Queueing model II (Infinite capacity multiple server Poisson queue model (M/M/C): ( $\infty$ /FIFO) – Queueing model III (Finite capacity single server Poisson queue model) (M/M/1): (N/FIFO) – Queueing model IV (Finite capacity multiple server Poisson model) (M/M/C) : (N/ FIFO).									
<b>REFERENCES:</b>										
1.	Bronson, R., "Schaum's Outline Series of Matrix Operations", 2 <sup>nd</sup> Edition, Mc Graw-Hill Education, 2011.									
2.	Howard Anton, Anton Kaul, "Elementary Linear Algebra" 12 <sup>th</sup> Edition, John Wiley & Sons, 2019.									
3.	Kanti Swarup, Gupta, P.K and Man Mohan "Operations Research", 20 <sup>th</sup> Revised Edition, Sultan Chand and Sons., New Delhi, 2019.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	apply various methods in matrix theory in communication engineering problems.	Applying (K3)
CO2	understand the concept of vector spaces.	Understanding (K2)
CO3	formulate and solve various types of linear programming problems.	Applying (K3)
CO4	use non-linear programming concepts in real life situations.	Applying (K3)
CO5	identify the suitable queuing model to handle communication problems.	Applying (K3)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3					
CO2	3					
CO3	3			2	2	
CO4	3			3	3	
CO5	3			3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN - THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		30	70				100
CAT2		30	70				100
CAT3		25	75				100
ESE		30	70				100

\* ±3% may be varied (CAT 1,2 & 3 – 50 marks & ESE – 100 marks)


Signature of the Chairman
Board of Studies - <b>ECE</b>



**24GET11 - INTRODUCTION TO RESEARCH**

(Common to all ME / MTech Branches &amp; MCA )

<b>Programme &amp; Branch</b>	<b>All ME/MTech branches &amp; MCA</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>									
<b>Prerequisites</b>	<b>NIL</b>	<b>1 / 3<sup>#</sup></b>	<b>FC</b>	<b>30</b>	<b>15</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>									
<b>Preamble</b>	This course will familiarize the fundamental concepts/techniques adopted in research, problem formulation and patenting. also, will disseminate the process involved in collection, consolidation of published literature and rewriting them in a presentable form using latest tools.																	
<b>Unit - I Concept of Research:</b>																		
Meaning and Significance of Research: Skills, Habits and Attitudes for Research - Time Management - Status of Research in India. Why, How and What a Research is? - Types and Process of Research - Outcome of Research - Sources of Research Problem - Characteristics of a Good Research Problem - Errors in Selecting a Research Problem - Importance of Keywords - Literature Collection – Analysis - Citation Study - Gap Analysis - Problem Formulation Techniques.																		
<b>Unit - II</b>	<b>Research Methods and Journals:</b>																	
Interdisciplinary Research - Need for Experimental Investigations - Data Collection Methods - Appropriate Choice of Algorithms / Methodologies / Methods - Measurement and Result Analysis - Investigation of Solutions for Research Problem - Interpretation - Research Limitations. Journals in Science/Engineering - Indexing and Impact factor of Journals - Citations - h Index - i10 Index – Journal Policies - How to Read a Published Paper - Ethical issues Related to Publishing - Plagiarism and Self-Plagiarism.																		
<b>Unit - III</b>	<b>Paper Writing and Research Tools:</b>																	
Types of Research Papers - Original Article/Review Paper/Short Communication/Case Study - When and Where to Publish? - Journal Selection Methods. Layout of a Research Paper - Guidelines for Submitting the Research Paper - Review Process - Addressing Reviewer Comments. Use of tools / Techniques for Research - Hands on Training related to Reference Management Software -End Note, Software for Paper Formatting like LaTeX/MS Office. Introduction to Origin, SPSS, ANOVA etc., Software for detection of Plagiarism.																		
<b>Unit - IV</b>	<b>Effective Technical Thesis Writing/Presentation:</b>																	
How to Write a Report - Language and Style - Format of Project Report - Use of Quotations - Method of Transcription Special Elements: Title Page - Abstract - Table of Contents - Headings and Sub-Headings - Footnotes - Tables and Figures - Appendix - Bibliography etc. - Different Reference Formats. Presentation using PPTs.																		
<b>Unit - V</b>	<b>Nature of Intellectual Property:</b>																	
Patents - Designs - Trade and Copyright. Process of Patenting and Development: Technological research - innovation - patenting - development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents.																		
<b>REFERENCES:</b>																		
1.	DePoy, Elizabeth, and Laura N. Gitlin, "Introduction to Research-E-Book: Understanding and Applying Multiple Strategies", Elsevier Health Sciences, 2015.																	
2.	Walliman, Nicholas, "Research Methods: The basics", Routledge, 2017.																	
3.	Bettig Ronald V., "Copyrighting culture: The political economy of intellectual property", Routledge, 2018.																	

\*includes Term Work(TW) &amp; Online / Certification course hours

# Semester1: ME / MTech , Semester 3: MCA



COURSE OUTCOMES:			BT Mapped (Highest Level)
On completion of the course, the students will be able to			
CO1	list the various stages in research and categorize the quality of journals.		Analyzing (K4)
CO2	formulate a research problem from published literature/journal papers		Evaluating (K5)
CO3	write, present a journal paper/ project report in proper format		Creating (K6)
CO4	select suitable journal and submit a research paper.		Applying (K3)
CO5	compile a research report and the presentation		Applying (K3)

#### Mapping of COs with POs

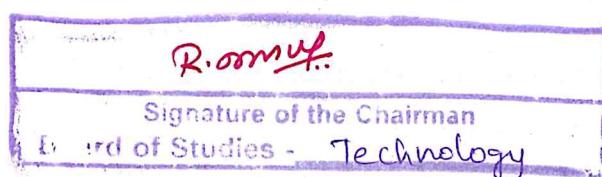
COs/POs	PO1	PO2	PO3	PO4	PO5
CO1	3	2	1		
CO2	3	2	3		
CO3	3	3	1		
CO4	3	2	1		
CO5	3	2	1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN - THEORY

Test / Blooms Category*	Remembering (K1) %	Understanding (K2) %	Applying(K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		30	40	30			100
CAT2		30	40	30			100
CAT3			30	40	30		100
ESE		30	40	30			100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)





24VLT11 - ADVANCED DIGITAL SYSTEM DESIGN										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	1	PC	45	15	0	60	120	3	
Preamble	To design synchronous, asynchronous digital circuits and implement using ASM chart and PLDs									
Unit- I	<b>Synchronous Sequential Circuit Design:</b> Analysis of Clocked Synchronous Sequential Networks (CSSN) – Modeling of CSSN – State table Reduction – Stable Assignment – Complete Design of CSSN.									
Unit- II	<b>Algorithmic State Machine (ASM):</b> ASM – ASM Chart – Synchronous Sequential Network Design Using ASM Charts – State Assignment – ASM Tables – ASM Realization - Asynchronous Inputs.									
Unit- III	<b>Asynchronous Circuit Design:</b> Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC- Static and Dynamic Hazards – Essential Hazards.									
Unit- IV	<b>Programming Logic Arrays:</b> PLA minimization – Essential Prime Cube theorem – PLA folding – foldable compatibility matrix - The Compact Algorithm. Practical PLA's – Data Synchronizers – Designing Vending Machine Controller.									
Unit- V	<b>Programmable Devices:</b> Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL - Realization State machine using PLD Language – FPGAs – Actel ACT.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	design clocked synchronous sequential circuits using state table reduction and assignment	Applying (K3)
CO2	realize functions using algorithmic state machines	Applying (K3)
CO3	design the asynchronous sequential circuit using flowtable reduction and find the hazards in circuits	Applying (K3)
CO4	simplify the Boolean function and implement using Programmable logic array, essential cube theorem and compact algorithm	Applying (K3)
CO5	design the synchronous sequential circuits using Programmable Logic Device, Programmable Array Logic and CPLD	Applying (K3)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2		3	3
CO2	3	3	2		2	3
CO3	3	3	2		3	3
CO4	3	3	2		3	3
CO5	3	3	2		3	3

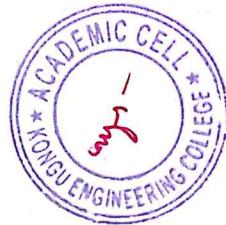
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN – THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		20	80				100
CAT2		20	80				100
CAT3		20	80				100
ESE		20	80				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


Signature of the Chairman
Board of Studies - <b>ECE</b>





24VLT12 - VLSI DESIGN TECHNIQUES																				
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit											
Prerequisites	NIL	1	PE	45	0	0	45	90	3											
Preamble	To understand the concepts of MOS Transistor characteristics, fabrication process and to design VLSI building blocks																			
Unit – I	<b>Overview of VLSI Design and MOS Transistor:</b>																			
VLSI Design Flow-Design Hierarchy-VLSI Design Styles. Fabrication Process Flow: Basic Steps-The CMOS n-well Process-Layout Design Rules. MOS Transistor: Structure and Operation of the MOS Transistor-MOSFET Current Voltage Characteristics-MOSFET Capacitances.																				
Unit – II	<b>MOS Inverters Characteristics:</b>																			
Static: Resistive Load Inverter-Inverters with MOSFET Load-CMOS Inverter. Switching: Delay Time Definitions-Calculation of Delay Times-Inverter Design with Delay constraints-Switching power Dissipation of CMOS Inverters-Power Delay Product, Energy Delay Product																				
Unit – III	<b>Combinational MOS and Dynamic Logic Circuits:</b>																			
MOS Logic Circuits with Pseudo-nMOS (pMOS) Loads-CMOS Logic Circuits-Complex Logic Circuits-CMOS Transmission Gates-Synchronous Dynamic Circuit Techniques-Dynamic CMOS Circuit Techniques-High performance CMOS Circuits.																				
Unit – IV	<b>Sequential MOS Logic Circuits:</b>																			
Behavior of Bistable Elements-The SR Latch Circuit-Clocked Latch and Flip-flop Circuits-CMOS D Latch and Edge triggered Flip-flop-Sense Amplifier based Flip-flops.																				
Unit – V	<b>VLSI Building Block Design:</b>																			
Arithmetic Building Block: Adders, Multipliers, Shifters, On chip Clock generation and Distribution-Memory Design (SRAM).																				
<b>REFERENCES:</b>																				
1.	Sung-Mo Kang, Yusuf Leblebici, Chulwoo Kim, "CMOS Digital Integrated Circuits Analysis and Design", Revised 4 <sup>th</sup> Edition, McGraw Hill Education (India) Edition 2018.																			
2.	Neil H.E. Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design", 3 <sup>rd</sup> Edition, Pearson Education ASIA, 2007.																			
3.	Jan M Rabaey, Anantha P Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: a Design Perspective", 2 <sup>nd</sup> Edition, Upper Saddle River, N.J., Pearson Education, 2003.																			

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	comprehend the principles of VLSI Design, MOS Transistor theory and its fabrication	Understanding(K2)
CO2	interpret the MOS inverter structures with various parameters	Understanding(K2)
CO3	make use of different logic styles for design of high performance CMOS circuits	Applying(K3)
CO4	comprehend the concepts of sequential MOS Logic circuits	Understanding(K2)
CO5	apply data path logic to design various building blocks	Applying(K3)

**Mapping of COs with POs**

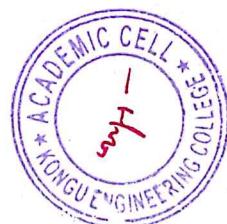
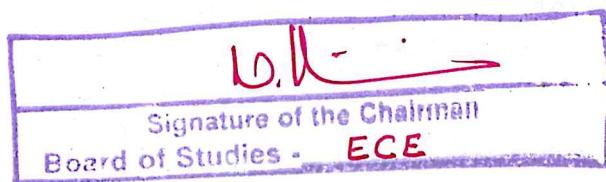
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3		3	3
CO2	3		3		3	3
CO3	3		3		3	3
CO4	3		3	3	3	3
CO5	3		3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN – THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100	-	-	-	-	100
CAT2		70	30	-	-	-	100
CAT3		65	35	-	-	-	100
ESE		70	30	-	-	-	100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)





<b>24VLT13 - HDL FOR IC DESIGN</b>										
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>	
<b>Prerequisites</b>	<b>NIL</b>	<b>1</b>	<b>PC</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>	
<b>Preamble</b>	To impart knowledge on designing and verification of Integrated Circuits using Verilog Hardware Description Language and System Verilog.									
<b>Unit – I</b>	<b>Introduction to Verilog:</b> Overview of digital design using Verilog HDL-Hierarchical Modeling concepts-Verilog Operators and Modules-Verilog Ports, Data types and Assignments-Gate level modelling-Switch level modelling-Modelling of CMOS gates and Boolean functions.									
<b>Unit – II</b>	<b>Dataflow and behavioral modelling:</b> Basics of dataflow modelling-Review of flip-flops-Verilog modeling of flip-flops-Basics of behavioral modelling-Verilog modeling of counters, sequence detector, FSMs and shift registers.									
<b>Unit – III</b>	<b>Verilog HDL Synthesis:</b> Synthesis Design Flow-Verification of the gate level net list-Modeling for logic synthesis-Example of sequential circuit synthesis - FIR filter implementation-IIR filter implementation									
<b>Unit – IV</b>	<b>Introduction to System Verilog:</b> Verification Process,- Basic Testbench Functionality - Directed Testing - Constrained-Random Stimulus, Functional Coverage, Testbench Components- Layered Testbench- Building a Layered Testbench- Simulation Environment Phases - Data types and procedural statements: Built-In Data Types- Fixed-Size Arrays- Dynamic Arrays- Queues- Associative Arrays- Array Methods- Choosing a Storage Type- Creating New Types with typedef- Creating User-Defined Structures- Type conversion- Enumerated Types- Task and Function Overview- Routine Arguments- Returning from a Routine.									
<b>Unit – V</b>	<b>Connecting the Test bench and Design:</b> Separating the Test bench and Design-The Interface Construct-Stimulus Timing-Interface Driving and Sampling-Connecting It All Together-Top-Level Scope-Program – Module Interactions-System Verilog Assertions-The Four-Port ATM Router.									
<b>REFERENCES:</b>										
1.	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2 <sup>nd</sup> Edition, Pearson Education New Delhi, 2018.									
2.	Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", 2 <sup>nd</sup> Edition, Springer, 2012.									
3.	<a href="https://ocw.mit.edu">https://ocw.mit.edu</a> – Massachusetts Institute of Technology Open Courseware.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:						BT Mapped (Highest Level)
On completion of the course, the students will be able to						
CO1	apply digital design concepts and write Verilog programs in gate level and transistor level modeling					Applying (K3)
CO2	write Verilog programs for the digital design using dataflow and behavioral modeling					Applying (K3)
CO3	synthesis the digital system for implementation in FPGA					Applying (K3)
CO4	understand the basic principles of verification process and System Verilog					Understanding(K2)
CO5	interface testbench and design environment					Applying (K3)

#### Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3

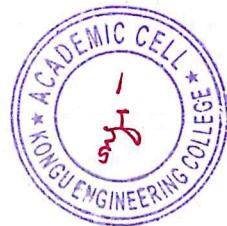
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		40	60				100
CAT2		35	65				100
CAT3		35	65				100
ESE		30	70				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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24VLT14-DEVICE MODELING									
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit
Prerequisites	NIL	1	PE	45	0	0	45	90	3
Preamble	To understand the solid state devices using mathematical concepts								
Unit – I	<b>Semiconductor Physics and Modeling of Passive Devices:</b> Quantum Mechanical Concepts- Carrier Concentration- Transport Equation- Mobility and Resistivity- Carrier diffusion- Carrier Generation and Recombination- Continuity equation- Tunneling and High field effects-Modeling of resistors-Modeling of Capacitors- Modeling of Inductors.								
Unit – II	<b>Diode and Bipolar Device Modeling :</b> Abrupt and linear graded PN junction- Ideal diode current equation- Static, Small signal and Large signal models of PN junction Diode-SPICE model for a Diode- Temperature and Area effects on Diode Model Parameters Transistor Action-Terminal currents -Switching- Static, Small signal and Large signal Eber-Moll models of BJT- temperature and area effects.								
Unit – III	<b>MOSFET Modeling and Parameter Measurements:</b> MOSFET Fundamentals – Basic Characteristics -Subthreshold region – Types of MOSFET – Threshold Voltage control – MOSFET Scaling - Short channel effects -Models for MOSFET- FinFET-CNTFET.								
Unit – IV	<b>Noise Models and BSIM4 MOSFET Model:</b> Noise Sources in MOSFET-Flicker Noise Modeling-Thermal Noise Modeling- BSIM4 MOSFET Model-Gate Dielectric Model- Enhanced Models for Effective DC and AC Channel Length and width-Threshold Voltage Model-I-V Model.								
Unit – V	<b>Other MOSFET Models:</b> EKV Model-Model Features-Long Channel Drain Current Model-Modeling Second order Effects of Drain Current-Effect of Charge Sharing-Modeling of Charge storage Effects-Non-quasi static Modeling-Noise Models-Temperature Effects-MOS Model 8-MOSAI Model.								
<b>REFERENCES:</b>									
1.	Massobrio Giuseppe and Antognetti Paolo, "Semiconductor Device Modeling with SPICE", 2 <sup>nd</sup> Edition, McGraw-Hill Inc, New York, 2010								
2.	Sze S. M., "Semiconductor Devices-Physics and Technology", 3 <sup>rd</sup> Edition, John Wiley and Sons, New York, 2010.								
3.	TrondYtterdal, Yuhua Cheng and Tor A.Fjeldly,"Device Modeling for Analog and RF CMOS Circuit Design" John Wiley & Sons Ltd ,2003.								

\*includes Term Work(TW) &amp; Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	realize the concepts of semiconductor physics				Understanding(K2)
CO2	understand various mathematical concepts to model semiconductor devices				Understanding(K2)
CO3	apply mathematical concepts to model MOSFET				Applying(K3)
CO4	infer the effects of noise in MOSFET using mathematical concepts.				Understanding(K2)
CO5	comprehend the secondary effects of semiconductor physics using mathematical expressions				Understanding(K2)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	3	2
CO2	3		3	2	3	2
CO3	3		3	2	3	2
CO4	3		3	2	3	2
CO5	3		3	2	3	2

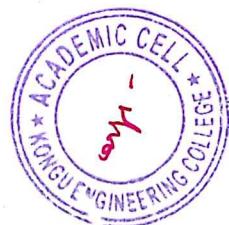
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN - THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		70	30				100
CAT3		100					100
ESE		80	20				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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24VLL11-VLSI DESIGN LABORATORY																			
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit										
Prerequisites	NIL	1	PC	0	0	30	0	30	1										
Preamble	To impart the knowledge of design and layout of digital circuits																		
LIST OF EXPERIMENTS / EXERCISES:																			
1.	Design and Analysis of CMOS Inverter																		
2.	Design and Analysis of Basic Logic Gates																		
3.	Design and Simulation of Combinational Circuits																		
4.	Design and Simulation of Sequential Circuits																		
5.	Design and Simulation of Memory Array																		
6.	Design and Simulation of Logic Designs using Pass Transistor and Transmission Gates																		
7.	Mini Project in CMOS Digital Circuits																		
REFERENCES/ MANUAL /SOFTWARE:																			
1.	Laboratory Manual																		
2.	Cadence- Virtuoso																		
COURSE OUTCOMES:																			
On completion of the course, the students will be able to										BT Mapped (Highest Level)									
CO1	design Digital systems at transistor level																		
CO2	obtain the layout of digital systems																		
CO3	analyze the characteristics of digital Circuits																		
Mapping of COs with POs																			
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6													
CO1	3	3	3	3	3	2													
CO2	3	3	3	3	3	2													
CO3	3	3	3	3	3	2													

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

\*includes Term Work(TW) & Online / Certification course hours

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24VLL12 - HDL FOR IC DESIGN LABORATORY																				
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit											
Prerequisites	NIL	1	PC	0	0	30	0	30	1											
Preamble	To impart the knowledge of design, verification and implementation of digital circuits using Verilog Hardware Description Language and System Verilog																			
LIST OF EXPERIMENTS / EXERCISES:																				
1.	Modeling of Combinational Digital Systems with Test benches																			
2.	Modeling of Sequential Digital Systems with Test benches																			
3.	Modeling of CMOS gates and Boolean functions																			
4.	Modeling of FSM and Memory design with Test benches																			
5.	Design and implementation of ALU, MAC using FPGA																			
6.	Mini project																			
REFERENCES/ MANUAL /SOFTWARE:																				
1.	Laboratory Manual																			
2.	Modelsim/EDA Tool																			
3.	Xilinx/EDA Tool																			
COURSE OUTCOMES:																				
On completion of the course, the students will be able to										BT Mapped (Highest Level)										
CO1	design and verification of digital systems using Verilog and system verilog									Applying (K3), Precision(S3)										
CO2	design and analysis of analog system using CMOS transistors									Applying (K3), Precision(S3)										
CO3	Implement system design in FPGA									Applying (K3), Precision(S3)										
Mapping of COs with POs																				
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6														
CO1	3	3	3	3	3	2														
CO2	3	3	3	3	3	2														
CO3	3	3	3	3	3	2														

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

\*includes Term Work(TW) & Online / Certification course hours

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24VLT21 - ANALOG INTEGRATED CIRCUITS																				
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit											
Prerequisites	NIL	2	PC	45	0	0	45	90	3											
Preamble	To focus on the concepts of MOSFETs and design of differential amplifiers, current mirrors, feedback amplifiers and oscillators																			
Unit – I	<b>Basic MOS Device Physics and Single Stage Amplifiers:</b>																			
Unit – II	<b>Differential Amplifiers and Current Mirrors:</b>																			
Differential Amplifiers: Single Ended and Differential Operation-Basic Differential Pair-Common-Mode Response- Differential Pair with MOS loads-Gilbert Cell. Passive and Active Current Mirrors: Basic Current Mirrors-Cascode Current Mirrors-Active Current Mirrors.																				
Unit – III	<b>Frequency Response of Amplifiers and Noise:</b>																			
Frequency Response of Amplifiers: General Considerations-Common Source Stage-Source Followers, Common Gate Stage-Cascode Stage-Differential Pair.Noise: Types of Noise-Representation of Noise in circuits-Noise in single stage amplifiers-Noise in Differential Pairs.																				
Unit – IV	<b>Feedback and Operational Amplifiers:</b>																			
Feedback Amplifiers: General Considerations-Feedback Topologies-Effect of Loading. Operational Amplifiers: General Considerations-One Stage Op Amps-Two Stage Op Amps-Gain Boosting-Common-Mode Feedback-Input Range limitations-Slew Rate-Power Supply Rejection.																				
Unit – V	<b>Oscillators and Phase Locked Loops:</b>																			
Oscillators: General Considerations-Ring Oscillators-LC Oscillators. Phase Locked Loops: Simple PLL-Delay Locked Loops-Applications.																				
<b>REFERENCES:</b>																				
1.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Edition 2002, McGraw-Hill Edition reprint 2017.																			
2.	Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5 <sup>th</sup> Edition, Wiley, New Delhi, 2013.																			
3.	David A. Johns, Martin K, "Analog Integrated Circuit Design", John Wiley & Sons, Inc., New York, 2013.																			

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	comprehend the concepts of MOS device physics and single stage amplifiers.				
CO2	design single stage amplifiers, differential amplifiers and current mirrors				
CO3	examine the frequency response of amplifiers and the effects of noise in amplifiers				
CO4	design feedback and operational amplifiers				
CO5	understand various oscillators and phase locked loops				

#### Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	3	3
CO2	3		3	2	3	3
CO3	3		3	2	3	3
CO4	3		3	2	3	3
CO5	3		3	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		80	20	-	-	-	100
CAT2		65	35	-	-	-	100
CAT3		65	35	-	-	-	100
ESE		65	35	-	-	-	100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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24VLT22 - APPLICATION SPECIFIC INTEGRATED CIRCUITS																				
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit											
Prerequisites	VLSI Design Techniques	2	PC	45	0	0	45	90	3											
Preamble	To know the different programmable ASICs, logic cells, I/O cells and interconnect and to learn how synthesis and physical design flow is carried out in an ASIC design.																			
Unit – I	<b>Introduction to ASICs, CMOS Logic and ASIC Library Design:</b>																			
Types of ASICs - Design flow - Combinational logic Cell – Sequential logic cell - Data path logic cell - Transistors as resistors - Transistor parasitic capacitance- Logical effort.																				
Unit – II	<b>Programmable ASICs, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells:</b>																			
Antifuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX - DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.																				
Unit – III	<b>Programmable ASIC Interconnect:</b>																			
Actel ACT -Xilinx LCA - Xilinx CPLD - Altera MAX 5000 and 7000 - Altera MAX8000 - Altera FLEX.																				
Unit – IV	<b>Logic Synthesis</b>																			
Design systems - Half gate ASIC –Schematic entry - Low level design language - PLA tools -EDIF- CF1 design representation-.Logic synthesis – Logic Simulation - Design and synthesis of various circuits.																				
Unit – V	<b>Physical Design</b>																			
ASIC Partitioning - floor planning- placement and routing – power and clocking strategies - DRC.																				
<b>REFERENCES:</b>																				
1.	Micheal John Sebastian Smith," Application - Specific Integrated Circuits", 12 <sup>th</sup> compression, Pearson,2013																			
2.	Steve Kilts, "Advanced FPGA Design: Architecture, Implementation, and Optimization" Wiley Inter-Science, 2016																			
3.	Roger Woods, John McAllister, Gaye Lightbody, Dr. Ying Yi, "FPGA-based Implementation of Signal Processing Systems", 2 <sup>nd</sup> Edition, Wiley, 2017.																			

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	understand ASIC Design flow and Design Libraries	Understanding(K2)
CO2	understand the ASIC programming technology and programmable ASIC I/O cells	Understanding(K2)
CO3	summarize the architecture of programmable ASIC interconnects	Understanding(K2)
CO4	Infer logic synthesis concept of digital circuits	Understanding(K2)
CO5	apply the algorithms used in partitioning, floorplanning, placement, routing, power and clock design for ASIC	Applying(K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3			
CO2	3		3			
CO3	3		3	2	3	
CO4	3		3	3	3	3
CO5	3		3	3	3	3

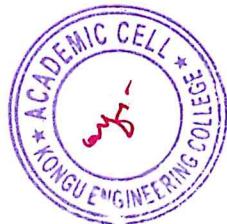
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		60	40				100
ESE		80	20				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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24VLT23 - VLSI SIGNAL PROCESSING										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	2	PC	45	15	0	45	90	4	
Preamble	To design an efficient signal processing architecture for VLSI implementation.									
<b>Unit – I</b>	<b>Introduction to DSP Systems:</b> Introduction To DSP Systems -Typical DSP algorithms; <b>Iteration Bound</b> — data flow graph representations, loop bound and iteration bound, Algorithms for computing iteration bound, Pipelining and parallel processing: Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.									
<b>Unit – II</b>	<b>Retiming &amp; Unfolding:</b> Retiming: Definitions and properties Retiming techniques; Solving systems of inequalities, Retiming Techniques. Unfolding: Algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application									
<b>Unit – III</b>	<b>Systolic Architecture Design &amp; Bit Level Arithmetic Architectures:</b> <b>Systolic Architecture Design:</b> Design methodology, FIR systolic arrays-B1,B2 and R1,R2 design <b>BitLevel Arithmetic Architectures:</b> Parallel Multipliers, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonical Signed Digit Arithmetic, Distributed Arithmetic									
<b>Unit – IV</b>	<b>Fast Convolution, Algorithmic strength reduction:</b> <b>Fast Convolution:</b> Fast convolution – Cook-Toom algorithm and Winograd Algorithm <b>Algorithmic strength reduction:</b> Algorithmic strength reduction in Filters-Parallel FIR Filters (two parallel and three parallel), Discrete Cosine Transform									
<b>Unit – V</b>	<b>Scaling, Round off Noise, Numerical Strength Reduction:</b> <b>Scaling, Round off Noise:</b> Scaling and Round off Noise- State variable Description of digital filters, Scaling and round off noise computation, Round off noise in pipelined I order IIR filters <b>Numerical Strength Reduction</b> -Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters									
<b>REFERENCES:</b>										
1.	Keshab K. Parhi, VLSI Digital Signal Processing Systems, Design and Implementation, Student Edition, John Wiley, Inter Science, New York, 2012									
2.	Mohammed Ismail, Terri Fiez, Analog VLSI Signal and Information Processing, McGraw-Hill, New York, 1984.									
3.	Magdy A. Bayoumi, Earl E. Swartzlander, VLSI Signal Processing Technology, Springer US Publishers. 2012									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	apply pipelining and parallel processing concepts for efficient low power architecture.	Applying(K3)
CO2	apply retiming and unfolding techniques for the design of VLSI architecture.	Applying(K3)
CO3	apply systolic and bit level architectures to improve the efficiency of VLSI circuits.	Applying(K3)
CO4	apply fast convolution algorithms for FIR and IIR filters	Applying(K3)
CO5	use of proper techniques for parallel processing design for scaling and roundoff noise computation	Applying(K3)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3		3
CO2	3	2	3	3		3
CO3	3	2	3	3		3
CO4	3	2	3	3		3
CO5	3	2	3	2		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN - THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		30	70			-	100
CAT2		30	70			-	100
CAT3		30	70			-	100
ESE		20	80			-	100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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24VLE01 - TESTING OF VLSI CIRCUITS										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	2	PE	45	0	0	45	90	3	
Preamble	To know the basics of VLSI test concepts, test generation, DFT architectures, Built in Self-Test, memory testing and test compression.									
Unit – I	<b>Fault modeling and simulation:</b> Importance of Testing- Challenges in VLSI Testing -Fault models- Logic simulation- Compiled code simulation-Event driven simulation- Fault simulation- Serial fault simulation- Parallel fault simulation- Deductive fault simulation- Concurrent fault simulation									
Unit – II	<b>Design For Testability:</b> Testability analysis -DFT basics- Scan cell designs- Scan architectures- Scan design rules- Scan design flow									
Unit – III	<b>Test Generation:</b> Random test generation- Designing a stuck-at model- ATPG for Combinational Circuits- Designing a sequential ATPG- Designing Simulation based ATPG-Hybrid deterministic and simulation based ATPG.									
Unit – IV	<b>Built In Self-Test:</b> BIST design rules- Test pattern generation- Output response analysis- Logic BIST architectures									
Unit – V	<b>Test compression and Memory Testing:</b> Test stimulus compression- Code based schemes - RAM functional fault models – Dynamic faults- Functional test patterns and algorithms-March tests-Word-oriented memory- Multi-port memory.									
<b>REFERENCES:</b>										
1.	Laung – Terngwang, Cheng – wen wu, Xidogingwen, "VLSI Testing Principles and Architectures: Design for Testability", Morgan Kaufmann Publisher, 2011.									
2.	Abramovici, M., Breuer, M.A and Friedman, A.D., "Digital Systems and Testable Design", Jaico Publishing House, 2014.									
3.	Bushnell, M.L and. Agrawal, V.D., "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers, 2002.									

\*includes Term Work(TW) & Online / Certification course hours





COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	distinguish between different fault models and types of simulation	Understanding (K2)
CO2	identify the design for testability techniques for combinational and sequential circuits	Understanding (K2)
CO3	apply various test generation methods for combinational and sequential circuits	Applying (K3)
CO4	compare the various Built In Self Test architectures	Understanding (K2)
CO5	understand the various fault models for memory, test generation algorithms for memories and test compression approaches	Understanding (K2)

**Mapping of COs with POs**

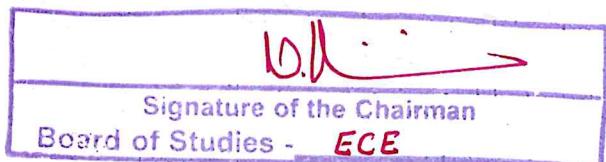
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	3	3
CO2	3		3	2	3	3
CO3	3		3	2	3	3
CO4	3		3	2	3	3
CO5	3		3	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN – THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		70	30				100
CAT3		100					100
ESE		85	15				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)





24VLE02-SEMICONDUCTOR MEMORY DESIGN										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	2	PE	45	0	0	45	90	3	
Preamble	To study the architectures of SRAM and DRAM and to understand the concepts of various non-volatile memories, fault modeling, memory testing and various packaging technologies									
Unit – I	<b>Random Access Memory Technologies:</b> SRAM cell structures-MOS SRAM architecture-MOS SRAM cell and Peripheral circuit operation- Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology- CMOS DRAMs- DRAMs cell theory and advanced cell structures- BiCMOS, DRAMs- Soft error failures in DRAMs									
Unit – II	<b>Nonvolatile Memories:</b> Masked Read-Only Memories (ROMs)- High Density ROMs- Programmable Read-Only Memories (PROMs)- Bipolar PROMs- CMOS PROMs- Erasable(UV) Programmable Read-Only Memories (EPROMs)- Floating-Gate PROM Cell- One-Time Programmable (OTP) EPROMS- Electrically Erasable PROMs (EEPROMs)- EEPROM technology and Architecture- Nonvolatile SRAM									
Unit – III	<b>Memory Fault Modeling And Testing:</b> RAM Fault Modeling, Electrical Testing, Peusdo Random Testing – Megabit DRAM Testing –Nonvolatile Memory Modeling and Testing – IDDQ Fault Modeling and Testing – Application Specific Memory Testing.									
Unit – IV	<b>Semiconductor Memory Reliability:</b> Generalability Issues – RAM Failure Modes and Mechanism – Nonvolatile Memory-Reliability Modeling and Failure Rate Prediction – Design for Reliability-Reliability Test Structures.									
Unit – V	<b>Packaging Technologies:</b> Ferroelectric Random Access Memories (FRAMs)- Gallium Arsenide (GaAs) FRAMs- Analog Memories- Magneto Resistive Random Access Memories (MRAMs)- Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and reliability issues-Memory cards- High density memory packaging future directions.									
<b>REFERENCES:</b>										
1.	Sharma, Ashok K., "Semiconductor Memories: Technology, Testing, and Reliability", Wiley-IEEE Press, New York, 2014.									
2.	Sharma, Ashok K., "Advanced Semiconductor Memories: Architectures, Designs And Application", Wiley-IEEE Press, 2014.									
3.	Sharma, Ashok K., "Semiconductor Memories", 2 Volume Set, Wiley, IEEE Press 2003.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	Comprehend the structures of random access memories				Understanding(K2)
CO2	Understand the need of non-volatile memories and their applications				Understanding(K2)
CO3	interpret the fault free memory systems by fault modeling techniques				Understanding(K2)
CO4	Demonstrate the memory architectures with reliability				Understanding(K2)
CO5	Identify the packages for memories				Understanding(K2)

#### Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		2	2		2
CO2	3		2	2		2
CO3	2		2	2		2
CO4	3		2	2		2
CO5	2		2	2		2

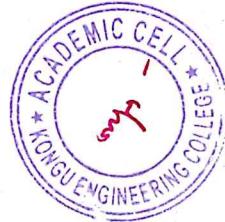
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		100					100
ESE		100					100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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<b>24VLE03-QUANTUM COMPUTING</b>										
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>	
<b>Prerequisites</b>	<b>NIL</b>	<b>2</b>	<b>PE</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>	
<b>Preamble</b>	To understand the concepts of quantum information theory, quantum algorithms and physical realization of systems									
<b>Unit – I</b>	<b>Introduction:</b> Global perspectives – Linear algebra-The postulates of quantum mechanics- Application: superdense coding-EPR and the Bellin equality									
<b>Unit – II</b>	<b>Quantum circuits:</b> Single qubit operations-Controlled operations–Measurement –Universalquantumgates-Quantumcircuitmodelofcomputation-Simulationofquantum systems									
<b>Unit – III</b>	<b>Quantum algorithms:</b> ThequantumFouriertransform-Phaseestimation–Orderfindingandfactoring- The quantum search algorithm									
<b>Unit – IV</b>	<b>Quantum Information:</b> Quantum information theory –Quantumerror-correction-Fault-tolerantquantumcomputation-Quantum cryptography.									
<b>Unit – V</b>	<b>Quantum computers(physical realization):</b> Guiding principles - Conditions for quantum computation - Optical photon quantum computer - Optical cavity quantum electrodynamics –Ion traps-Nuclear magnetic resonance-Other implementation schemes.									
<b>REFERENCES:</b>										
1.	Michael A. Nielsen & IsaacL.Chuang, "Quantum Computation and Quantum Information", Cambridge University Press,2013.									
2.	Eleanor G.Rieffel, Wolfgang H.Polak, "Quantum Computing: A Gentle Introduction", MITPress,2014.									
3.	Scott Aaronson, "Quantum Computing since Democritus", CambridgeUniversityPress,2013.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	describe the quantum mechanics using linear algebra	Understanding(K2)
CO2	interpret Qubits and design quantum gates	Understanding(K2)
CO3	demonstrate the quantum parallelism by using quantum algorithms	Understanding(K2)
CO4	Understand real-world quantum information processing	Understanding(K2)
CO5	infer the basic knowledge on physical realization of quantum computers	Understanding(K2)

**Mapping of COs with POs**

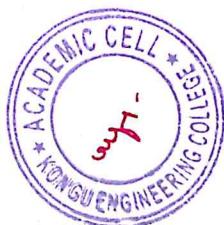
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2		2	2
CO2	3		2		2	2
CO3	3		2		2	2
CO4	3		2		2	2
CO5	3		2		2	2

**ASSESSMENT PATTERN – THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		100					100
ESE		100					100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

<i>N.L.</i>
Signature of the Chairman Board of Studies - <b>ECE</b>





24VLE04-LOW POWER VLSI DESIGN																				
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit											
Prerequisites	VLSI Design Techniques	2	PE	45	0	0	45	90	3											
Preamble	To design a low power digital circuits and analyze the various power optimization methods																			
<b>Unit – I</b>	<b>Sources of Power Dissipation and Power Optimization:</b>																			
Components of power dissipation in CMOS Circuits- Logic level power optimization- Problem formulation- Combinational circuits Technology independent optimization- Sequential circuits -Technology independent optimization- Technology-dependent optimization																				
<b>Unit – II</b>	<b>Circuit Level Techniques for Low Power Design:</b>																			
Circuit level low-power design- Logic style- Latches and Flip-flops- Transistor sizing and ordering- Drivers for large load- Power, and Delay in CMOS circuits- CMOS circuit design styles for adders- Power delay and area comparisons for 4-bit RCA, adders and multipliers																				
<b>Unit – III</b>	<b>Low Power System Design:</b>																			
Conventional arithmetic and low power design- Logarithmic Number System- Residue Number System- Reducing power consumption in memories- Static random access memories- Dynamic random access memories																				
<b>Unit – IV</b>	<b>Low Power Clock Design and Power Estimation:</b>																			
Low-Power Clock Design- Interconnect Delays- Classification of power estimation methodologies- Simulation based power estimation- Probabilistic methods.																				
<b>Unit – V</b>	<b>Software Design for Low Power:</b>																			
Sources of software power dissipation- Software power estimation- Software power optimization- Automated low power code generation- Co-design for low power.																				
<b>REFERENCES:</b>																				
1.	Dimitrios Soudris, Christian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002.																			
2.	Kaushik Roy and S.C. Prasad, "Low power CMOS VLSI circuit design", Wiley, 2018.																			
3.	Ajit Pal, "Low-Power VLSI Circuits and Systems", 1 <sup>st</sup> Edition, Springer 2015.																			

\*includes Term Work(TW) &amp; Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	enumerate the different sources of power dissipation in CMOS and various logic level power optimization techniques	Understanding (K2)
CO2	apply various power optimization techniques at circuit level.	Applying (K3)
CO3	design low power circuits at architecture level and memories	Applying (K3)
CO4	outline simulation and probabilistic method of power analysis and low power issues at low level design	Understanding (K2)
CO5	perform power estimation and optimization at programming level	Understanding (K2)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3	3	3
CO2	3		3	3	3	3
CO3	3		3	3	3	3
CO4	3		3	3	3	3
CO5	3		3	3	3	3

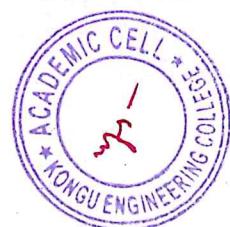
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN – THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		80	20				100
CAT2		50	50				100
CAT3		100					100
ESE		70	30				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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24VLE05-MIXED SIGNAL VLSI DESIGN										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	2	PE	45	0	0	45	90	3	
Preamble	To build the advanced CMOS VLSI Design with practical aspect of mixed signal VLSI blocks									
<b>Unit – I</b>	<b>Comparators and Switching circuits:</b> characterization of a comparator – two stage, open loop comparators-switched capacitor circuits – switched capacitor amplifiers-switched capacitor integrators.									
<b>Unit – II</b>	<b>Continuous Time Filters:</b> Introduction to continuous time filters: First and Second order filters - introduction to Gm - C filters - CMOS transconductors using Triode transistors- bipolar transconductors- BiCMOS transconductors – MOSFET C Filters - Tuning circuitry									
<b>Unit – III</b>	<b>Digital To Analog&amp; Analog To Digital Converters:</b> Ideal D/A Converter- ideal A/D converter- Types of DAC's: binary scaled converters – hybrid converters. Types of ADC's: successive approximation converters-pipelined A/D converters – flash converters-two step A/D converters- folding A/D converters.									
<b>Unit – IV</b>	<b>Over sampling converters:</b> Over sampling without noise shaping- oversampling with noise shaping – digital decimation filter-system architecture: system architecture of delta sigma A/D converters- system architecture of delta sigma D/A converters- higher order modulators.									
<b>Unit – V</b>	<b>Phase- locked loops:</b> Basic phase locked loop architecture- linearized small signal analysis- jitter and phase noise- electronic oscillators- jitter and phase noise in PLLs.									
<b>REFERENCES:</b>										
1.	Tony Chan Carusone, David Johns, Kenneth Martin, Analog Integrated Circuit Design, 2nd Edition, John Wiley and Sons, 2013									
2.	Rudy van de Plassche, Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd Edition, Springer, 2007.									
3.	Phillip Allen, Douglas Holberg, CMOS Analog Circuit Design, 2nd Edition, Oxford University Press, 2013.									

\*includes Term Work(TW) & Online / Certification course hours





COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	comprehend the concepts of switched capacitor circuits and comparators	Understanding (K2)
CO2	comprehend the concepts of continuous time filters and its performance	Understanding (K2)
CO3	illustrate Digital To Analog & Analog To Digital Converters	Understanding (K2)
CO4	comprehend sigma delta converters	Understanding (K2)
CO5	infer the working of PLL	Understanding (K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		2	3	2	3
CO2	2		2	3	2	3
CO3	3		3	3	2	3
CO4	3		3	3	2	3
CO5	3		3	3	2	3

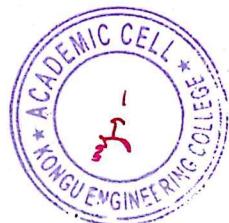
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		100					100
ESE		100					100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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<b>24VLE06-RF CIRCUIT DESIGN</b>																				
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>											
<b>Prerequisites</b>	<b>Analog IC Design</b>	<b>2</b>	<b>PE</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>											
<b>Preamble</b>	To infer the concepts of CMOS RF circuits and systems at microwave regime.																			
<b>Unit – I</b>	<b>CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES:</b> <span style="float: right;">9</span>																			
Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port noise theory, Noise figure, THD, IP2, IP3, sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne receiver, Heterodyne receiver, Image reject, Low IF receiver architectures direct up conversion transmitter, Two step up conversion transmitter																				
<b>Unit – II</b>	<b>IMPEDANCE MATCHING AND AMPLIFIERS:</b> <span style="float: right;">9</span>																			
S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.																				
<b>Unit – III</b>	<b>FEEDBACK SYSTEMS AND POWER AMPLIFIERS:</b> <span style="float: right;">9</span>																			
Stability of feedback systems: Gain and phase margin, Root- locus techniques, Time and Frequency domain considerations, Compensation, General model— Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations																				
<b>Unit – IV</b>	<b>MIXERS AND OSCILLATORS:</b> <span style="float: right;">9</span>																			
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.																				
<b>Unit – V</b>	<b>PLL AND FREQUENCY SYNTHESIZERS:</b> <span style="float: right;">9</span>																			
Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-frequency synthesizers, Direct Digital Frequency synthesizers																				
<b>REFERENCES:</b>																				
1.	T.Lee, "Design of CMOS RF Integrated Circuits", World Scientific Publishing Co Pvt. Ltd., 1 <sup>st</sup> edition 2010.																			
2.	B.Razavi, "RF Microelectronics", Pearson Education India; 2 <sup>nd</sup> edition, 2013.																			
3.	JanCrols, Michiel Steyaert, "CMOS Wireless Transceiver Design", Springer India, 2015.																			

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	differentiate the noises associated with CMOS technology and to comprehend the RF receiver operation				
CO2	infer the input and output impedance matching networks for amplifier design				
CO3	demonstrate the RF power amplifier design with the context of stability				
CO4	Interpret the design of RF mixers and oscillators for IC implementation				
CO5	summarize the PLL and synthesizer architectures and their performance				

#### Mapping of COs with POs

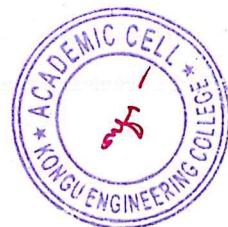
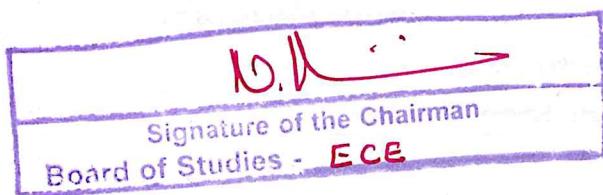
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	2	2	2
CO2	3		2	2	2	2
CO3	3		2	2	2	2
CO4	3		2	2	2	2
CO5	3		2	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		100					100
ESE		100					100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)





24VLE07-COMPUTER AIDED DESIGN OF VLSI CIRCUITS																						
Programme & Branch		ME & VLSI DESIGN		Sem.	Category	L	T	P	SL*	Total	Credit											
Prerequisites		ASIC Design		2	PE	45	0	0	45	90	3											
Preamble	To give an overview of the VLSI physical design and understand CAD algorithms used in VLSI physical design automation field																					
<b>Unit – I</b>	<b>Design Methodologies:</b>										<b>9</b>											
Introduction to VLSI design methodologies – Review of VLSI design automation tools –Algorithmic graph theory and Computational complexity –Tractable and intractable problems – general purpose methods for combinatorial optimization problems																						
<b>Unit – II</b>	<b>Partitioning, Placement and Floor planning :</b>										<b>9</b>											
Placement and partitioning –circuit representation – Placement algorithms –Genetic algorithm for standard-cell Placement(GASP) Partitioning- Partitioning algorithms-Floor planning concepts –shape functions and floor plan sizing –Floorplanning based on Simulated Annealing																						
<b>Unit – III</b>	<b>Routing and Compaction:</b>										<b>9</b>											
Routing – Types of local routing problems – area routing – channel routing – global routing –algorithms for global routing. Compaction- Layout Compaction –Design rules –problem formulation –algorithms for constraint graph compaction.																						
<b>Unit – IV</b>	<b>Logic Simulation:</b>										<b>9</b>											
Simulation –Gate-level modeling and simulation –Switch-level modeling and simulation. Introduction to Combinational Logic Synthesis–Binary Decision Diagrams –ROBDD- ROBDD principles, implementation, construction and manipulation.																						
<b>Unit – V</b>	<b>High level Synthesis :</b>										<b>9</b>											
Hardware models –Internal representation –Allocation assignment and scheduling –Simple scheduling algorithm –Assignment problem–High level transformations.																						
<b>REFERENCES:</b>																						
1.	Gerez, S.H., "Algorithms for VLSI Design Automation", John Wiley & Sons, New York, 2002																					
2.	Sherwani, N.A., "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, Boston, 2002																					
3.	Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill International Edition 1885																					

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	outline the concepts and properties associated with graph theory	Understanding(K2)
CO2	inference the concepts of physical design process such as partitioning, floorplanning and placement	Applying (K3)
CO3	comprehend the concepts of physical design process such as routing and compaction	Applying (K3)
CO4	utilize the concepts of simulation in VLSI physical design automation	Applying (K3)
CO5	understand the concepts of synthesis in VLSI physical design automation	Understanding(K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2		3	
CO2	3	3	3		3	3
CO3	3	3	3		3	3
CO4	3		3		3	3
CO5	3		3		3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		65	35				100
CAT2		30	70				100
CAT3		65	35				100
ESE		45	55				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

 Signature of the Chairman Board of Studies - <b>ECE</b>
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24VLE08-SYSTEM ON CHIP										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	3	PE	45	0	0	45	90	3	
Preamble	To infer the concepts of hardware and software on a chip and to discuss the applications and implementations of system on chip using different communication architectures									
Unit - I	<b>Introduction to the Systems Approach:</b> System Architecture: An Overview - Components of the System - Hardware and Software: Programmability Versus Performance - Processor Architectures - Memory and Addressing - System-Level Interconnection - An Approach for SOC Design - System Architecture and Complexity - Product Economics and Implications for SOC.									
Unit - II	<b>Chip Basics:</b> Cycle Time - Die Area and Cost - Ideal and Practical Scaling - Power - Area – Time – Power Trade - Offs in Processor Design - Reliability – Configurability									
Unit - III	<b>Processors:</b> Processor Selection for SOC - Basic Concepts in Processor Architecture - Basic Concepts in Processor Micro architecture - Basic Elements in Instruction Handling-Buffers: Minimizing Pipeline Delays - Branches: Reducing the Cost of Branches - Vector Processors and Vector Instruction Extensions - VLIW Processors - Superscalar Processors.									
Unit - IV	<b>Memory Design:</b> Overview of SOC memory - cache memory - Strategies for Line Replacement at Miss Time-Split I - and D - Caches and the Effect of Code Density - Multilevel Caches - Virtual-to-Real Translation-SOC Memory Systems - Board-based Memory Systems - Simple DRAM and Memory Array - Models of Simple Processor – Memory Interaction									
Unit - V	<b>Interconnect and customization:</b> Bus: Basic Architecture - SOC Standard Buses - Analytic Bus Models - NOC with Switch Interconnects - Layered Architecture and Network Interface Unit- Customizing Instruction Processors - Reconfigurable Technologies									
<b>REFERENCES:</b>										
1.	Michael J Flynn and Wayne Luk, "Computer system Design: System-on-Chip", Wiley-India, 2012.									
2.	Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2 <sup>nd</sup> Edition, Springer, 2012									
3.	Sudeep Pasricha, Nikil Dutt, "On Chip Communication Architectures: System on Chip Interconnect", Illustrated Edition, Morgan Kaufmann Publishers, 2008.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	comprehend the SOC design approaches				Understanding(K2)
CO2	understand the basic concepts of chip design				Understanding(K2)
CO3	summarize the different processor architectures for SOC				Understanding(K2)
CO4	design the memory for SOC				Applying (K3)
CO5	comprehend the interfacing techniques and customization				Understanding(K2)

#### Mapping of COs with POs

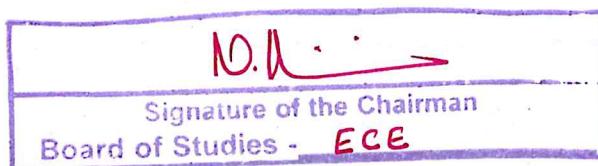
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	3		2
CO2	2		3	3		2
CO3	2		3	3		2
CO4	2		3	3		2
CO5	2		3	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		60	35				100
ESE		80	20				100

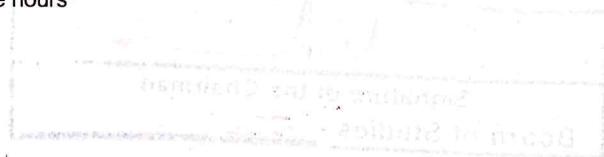
\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)





24VLE09-HARDWARE SOFTWARE CO-DESIGN										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	3	PE	45	0	0	45	90	3	
Preamble	To understand an integrated application development environment of hardware/software codesign in embedded system.									
Unit – I	<b>Design Consideration:</b> Platform - Based Design – System Modeling – Video Coding – Image Processing – Cryptography - Digital Communication									
Unit – II	<b>System Level Design:</b> Abstraction Levels–Algorithm Level Verification–Transaction Level Modeling–System Level Development Tools.									
Unit – III	<b>Embedded Processor Design</b> Specific Instruction-Set-Data Level Parallelism–Instruction Level Parallelism–Thread Level Parallelism									
Unit – IV	<b>Parallel Compiler:</b> Vectorization- Simdization–ILP Scheduling–Threading-Compiler Technique–Compiler Infrastructures									
Unit – V	<b>Real-Time Operating System for PLX:</b> PRRP Scheduler-Memory Management–Communication and Synchronization Primitives- Multimedia Applications in RTOS for PLX–Application Development Environment.									
<b>REFERENCES:</b>										
1.	Sao-jieChen ,Guang - Huei Lin, Pao -Ann Hsiung and Yu-Hen Hu, "Hardware Software Co-Design of a Multimedia SOC Platform" Illustrated Edition, Springer, 2008.									
2.	Patrick Schaumont, "A Practical Introduction to Hardware/Software Codesign", 2 <sup>nd</sup> Edition, Springer, 2010.									
3.	Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Publication, reprint 2007.									

\*includes Term Work(TW) & Online / Certification course hours





COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	acquire knowledge about system level modeling in image and video encoding				Understanding(K2)
CO2	perform algorithm level verification and work with system development tools				Understanding(K2)
CO3	distinguish between different levels of parallelism				Understanding(K2)
CO4	infer scheduling and compiler techniques				Understanding(K2)
CO5	apply the integrated application development environment for hardware/software codesign of embedded system				Applying(K3)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3			
CO2	3		3		3	3
CO3	3		3			
CO4	3		3			
CO5	3		3		3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN - THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		100					100
ESE		100					100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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**24VLL21- ANALOG INTEGRATED CIRCUITS LABORATORY**

Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit
Prerequisites	NIL	2	PC	0	0	30	0	30	1

Preamble To impart the knowledge of design, simulate and analysis of analog circuits

**LIST OF EXPERIMENTS / EXERCISES:**

1. Perform the Simulation of a Common Source Amplifier
2. Perform the Simulation of a Cascode Stage Amplifier
3. Perform the Simulation of a differential amplifier
4. Analysis of frequency response of voltage series and voltage shunt feedback topologies
5. Analysis of frequency response of current series and current shunt feedback topologies
6. Perform the Simulation of a Ring Oscillator
7. Miniproject

**REFERENCES/ MANUAL /SOFTWARE:**

1. Laboratory Manual
2. Cadence-Virtuoso

**COURSE OUTCOMES:**

On completion of the course, the students will be able to

**BT Mapped  
(Highest Level)**

CO1	design analog circuits at transistor level	Applying(K3), Precision(S3)
CO2	obtain the simulation of analog designs	Applying (K3), Precision (S3)
CO3	analyze the characteristics of analog Circuits	Analyzing (K4), Precision(S3)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

\*includes Term Work(TW) & Online / Certification course hours

<i>D.K.</i>
Signature of the Chairman
Board of Studies - <i>ECE</i>





**24VLL22 - APPLICATION SPECIFIC INTEGRATED CIRCUITS LABORATORY**

Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit
Prerequisites	VLSI Design Techniques	2	PC	0	0	30	0	30	1

Preamble To impart the knowledge of physical design of digital circuits

**LIST OF EXPERIMENTS / EXERCISES:**

1. Design, simulation and synthesis of Adders
2. Design, simulation and synthesis of multipliers
3. Design, simulation and synthesis of memory
  - For the following circuits,
  - a) Perform the functional verification
  - b) Synthesis the design
  - c) Generate the layout (Automatic)
  - d) Tabulate the area, power, delay
4. Universal Asynchronous Receiver Transmitter
5. Convolutional Neural Network Accelerator
6. Miniproject

**REFERENCES/ MANUAL /SOFTWARE:**

1. Laboratory Manual
2. Cadence

**COURSE OUTCOMES:**

**On completion of the course, the students will be able to**

		BT Mapped (Highest Level)
CO1	perform physical design of digital circuits	Applying(K3), Precision(S3)
CO2	analyze the performance of digital systems	Applying (K3), Precision (S3)
CO3	analyze the characteristics of digital Circuits	Analyzing (K4), Precision(S3)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

\*includes Term Work(TW) & Online / Certification course hours


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24VLE10- NETWORK ON CHIP										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	3	PE	45	0	0	45	90	3	
Preamble	To understand the different network architectures and concepts of Network On Chip									
Unit – I	<b>Uses of Interconnection Networks:</b> Processor-Memory Interconnect - I/O Interconnect - Packet Switching Fabric - Network Basics -Topology-Routing - Flow Control - Router Architecture - Performance of Interconnection - Case study with a simple interconnection network.									
Unit – II	<b>Topology Basics:</b> Channels and Nodes-Direct and Indirect Networks-Cuts and Bisects- Paths-Symmetry - Traffic Patterns - Performance - Throughput and Maximum Channel Load - Latency - Path Diversity - Case Study: Butterfly networks.									
Unit – III	<b>Non-Blocking Networks:</b> Non-Blocking vs. Non-Interfering Networks - Crossbar Networks –Close Networks - Bene's Networks - Sorting Networks. <b>Slicing and Dicing:</b> Concentrators and Distributors - Bit Slicing - Dimension Slicing - Channel Slicing - Slicing Multistage Networks.									
Unit – IV	<b>Routing Basics:</b> A Routing Example - Taxonomy of Routing Algorithms - The Routing Relation -Deterministic Routing - Oblivious Routing - Adaptive Routing.									
Unit – V	<b>Flow Control Basics:</b> <b>Flow Control Basics:</b> Resources and Allocation Units - Buffer less Flow Control - Circuit Switching -Buffered Flow Control. <b>Deadlock and Livelock:</b> Deadlock - Deadlock Avoidance - Adaptive Routing - Deadlock Recovery.									
<b>REFERENCES:</b>										
1.	William James Dally and Brian Towles, "Principles and Practices of Interconnection Networks", 1 <sup>st</sup> Edition, Morgan Kaufmann Publishers, 2004.									
2.	Santanu Kundu and Santanu Chattopadhyay, "Network-on-Chip: The Next Generation of System on-Chip Integration", CRC Press, 2014.									
3.	Giovanni De Micheli and Luca Benini, "Networks on Chips: Technology and Tools", 1 <sup>st</sup> Edition, Academic Press, 2006.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	summarize the interconnection networks	Understanding K2)
CO2	comprehend the basics of network topology	Understanding K2)
CO3	classify the different types of networks	Understanding(K2)
CO4	develop routing algorithms	Applying (K3)
CO5	explain the basics of flow control, deadlock and livelock	Understanding(K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	2	2	3
CO2	3		2	2	2	3
CO3	3		2	2	2	3
CO4	3		3	3	3	3
CO5	3		2	2	2	3

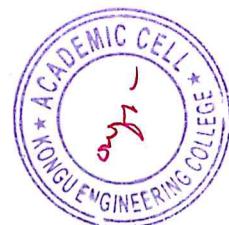
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		50	50				100
ESE		80	20				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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Board of Studies : <b>ECE</b>





<b>24VLE11-RECONFIGURABLE ARCHITECTURES FOR VLSI</b>										
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>	
<b>Prerequisites</b>	<b>VLSI Design Techniques</b>	<b>3</b>	<b>PE</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>	
<b>Preamble</b>	To comprehend and apply different reconfigurable architecture in FPGA.									
<b>Unit – I</b>	<b>Device architecture:</b> General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices– Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.									
<b>Unit – II</b>	<b>Reconfigurable computing architectures and systems:</b> Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Reconfiguration Management.									
<b>Unit – III</b>	<b>Programming reconfigurable systems:</b> Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing									
<b>Unit – IV</b>	<b>Mapping designs to reconfigurable platforms:</b> Technology Mapping – FPGA Placement – Datapath composition -Retiming, Repipelining, and C-slow Retiming – Configuration Bit stream Generation.									
<b>Unit – V</b>	<b>Application development:</b> Implementing Applications with FPGAs –Pattern Matching- Video Streaming -Adaptive cryptographic systems-Adaptive controller.									
<b>REFERENCES:</b>										
1.	Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation", Elsevier / Morgan Kaufmann, 2008.									
2.	Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005									
3.	Christophe Bobda, "Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications", Springer, 2010.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	comprehend the different computing models				Understanding(K2)
CO2	discuss the different reconfigurable computing architecture and systems				Understanding(K2)
CO3	develop program for reconfigurable systems				Applying(K3)
CO4	map the design into different platforms				Understanding(K2)
CO5	apply reconfigurable technique for developing applications				Applying(K3)

**Mapping of COs with POs**

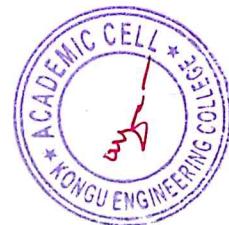
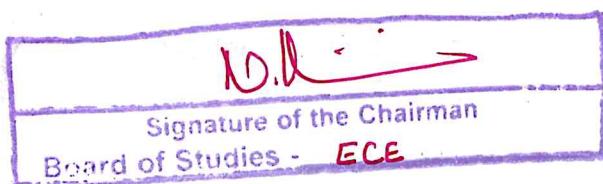
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3	2	2
CO2	3		3	3	2	2
CO3	3		3	3	2	2
CO4	3		3	3	2	2
CO5	3		3	3	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN - THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		65	35				100
CAT3		65	35				100
ESE		65	35				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)





<b>24VLE12-HARDWARE SECURITY</b>										
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>	
<b>Prerequisites</b>	<b>VLSI Design Techniques</b>	<b>3</b>	<b>PE</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>	
<b>Preamble</b>	To understand the basics of hardware security, hardware Trojan attacks in IPs and FPGAs, side-channel attacks and hardware Trojan prevention.									
<b>Unit – I</b>	<b>Introduction to Hardware Trojan and Hardware Trojan attacks:</b> Overview of Hardware Trojans- Trends, Tradeoffs and Threats of Trojans- Comparisons and Misconceptions with Trojan Attacks- Offensive Strategies- Defensive Strategies -Challenges of SoC Security- SoC Threat Model- SoC Security Assurance.									
<b>Unit – II</b>	<b>Hardware IP Trust and Hardware Trojan in ICs:</b> Trojan Characteristics – Inadequacies of existing testing and security features- Trojan classification – General Trojan Mitigation techniques- Trojan Mitigation at IP Level – Hardware Trojans in RF ICs - Hardware Trojans in Analog-Mixed Signal (AMS) ICs.									
<b>Unit – III</b>	<b>Side-Channel Attacks:</b> Taxonomy of Side-Channel Attacks – Power Analysis Attacks- Electromagnetic Side-Channel Attacks- Fault Injection Attacks- Timing Attacks									
<b>Unit – IV</b>	<b>Hardware Trojan Prevention:</b> Obfuscation- Role of Obfuscation in Hardware Trojan Prevention- Chip-Level Obfuscation- FPGA Obfuscation- Board Level Obfuscation- Evaluation Metrics for Hardware Obfuscation – Physical Unclonable Function									
<b>Unit – V</b>	<b>Hardware Trojan Attacks in FPGA and Protection Approaches:</b> Threat Models and Taxonomy- Trojans in FPGA Fabric- Trojans in FPGA Design- Trojan in Bit stream- Countermeasures against FPGA Trojans.									
<b>REFERENCES:</b>										
1.	SwarupBhunia, and M. Tehranipoor, "The Hardware Trojan War." Springer (2018).									
2.	SwarupBhunia, and Mark Tehranipoor, "Hardware security: a hands-on learning approach", Morgan Kaufmann, 2018.									
4.	RoelMaes, "Physically unclonable functions: Constructions, properties and applications" Springer Science & Business Media, 2013.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	outline the offensive and defensive strategies of hardware Trojan				Understanding (K2)
CO2	classify the Trojan and Mitigation techniques				Understanding (K2)
CO3	understand the various forms of side-channel attacks				Understanding (K2)
CO4	interpret the types of obfuscation techniques and physical unclonable function				Understanding (K2)
CO5	summarize the types of FPGA Trojans				Understanding (K2)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3		2	2
CO2	3		3		2	2
CO3	3		3		2	2
CO4	3		3		2	2
CO5	3		3		2	2

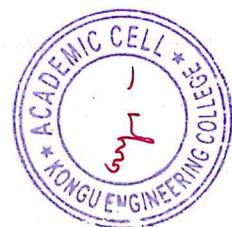
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN - THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		100					100
ESE		100					100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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24VLE13-FUNCTIONAL VERIFICATION USING HDL																				
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit											
Prerequisites	Verilog HDL	3	PE	45	0	0	45	90	3											
Preamble	To impart knowledge on System Verilog and demonstrate the design and verification using System Verilog constructs.																			
<b>Unit – I</b>	<b>Basic Object Oriented Programming:</b>																			
Introduction-OOP Terminology-Creating New Objects-Object De-allocation-Using Objects-Static Variables vs. Global Variables-Class Methods-Defining Methods Outside of the Class-Scoping Rules-Using One Class Inside Another-Understanding Dynamic Objects-Copying Objects-Building a Testbench.																				
<b>Unit – II</b>	<b>Randomization:</b>																			
Randomization in SystemVerilog-Constraint Details-Controlling Multiple Constraint Blocks-Valid Constraints-In-line Constraints-The pre-randomize and post-randomize Functions-Common Randomization Problems-Iterative and Array Constraints-Atomic Stimulus Generation vs. Scenario Generation-Random Control																				
<b>Unit – III</b>	<b>Threads and Inter-process Communication:</b>																			
Working with Threads-Disabling Threads-Inter-process Communication-Events-Semaphores-Mailboxes-Building a Testbench with Threads and IPC-Coverage Types-Functional Coverage Strategies-Data Sampling-Cross Coverage-Analyzing Coverage Data.																				
<b>Unit – IV</b>	<b>Advanced Interfaces:</b>																			
Virtual Interfaces with the ATM Router-Connecting to Multiple Design Configurations-Procedural Code in an Interface-Design Blocks-Testbench Blocks-Alternate Tests.																				
<b>Unit – V</b>	<b>Interfacing With C:</b>																			
Passing Simple Values- Connecting to a Simple C Routine- Connecting to C++- Simple Array Sharing- Open arrays- Sharing Composite Types- Pure and Context Imported Methods- Communicating from C to SystemVerilog- Connecting Other Languages.																				
<b>REFERENCES:</b>																				
1.	Chris Spear, "System Verilog for Verification: A Guide to Learning the Test bench Language Features", 2 <sup>nd</sup> Edition, Springer, 2012.																			
2.	Stuart Sutherland, Simon Davidman and Peter Flake , SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2nd Edition, , Springer																			
3.	Donald Thomas, "Logic Design and Verification Using SystemVerilog", Create Space Independent Publishing Platform, 2014																			

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	understand the basics of Object Oriented Programming concepts in System Verilog	Understanding(K2)
CO2	demonstrate the constrained random coverage driven verification in SV Environment	Applying(K3)
CO3	construct a complete verification with system verilog test bench	Applying(K3)
CO4	construct a verification platform with advanced interfaces	Applying(K3)
CO5	demonstrate communicating from C language to SystemVerilog	Applying(K3)

#### Mapping of COs with POs

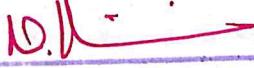
COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	3	3	2
CO2	2		3	3	3	2
CO3	2		3	3	3	2
CO4	3	3	3	3	3	2
CO5	3	3	3	3	3	3

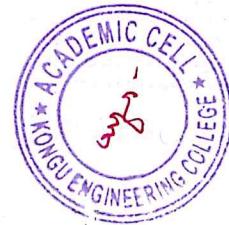
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		40	60				100
CAT2		20	80				100
CAT3		20	80				100
ESE		30	70				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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<b>24VLE14- VLSI FOR IOT SYSTEMS</b>										
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>	
<b>Prerequisites</b>	<b>VLSI Design Techniques</b>	<b>3</b>	<b>PE</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>	
<b>Preamble</b>	To impart knowledge on design methodologies and architectures for IoT systems on a chip.									
<b>Unit – I</b>	<b>Introduction:</b> The Internet of Things: Context and Overview- Requirements of IoT Nodes- Physical Constraints- Interaction with the External World - On-Board Capabilities of IoT Nodes- User Constraints -Present and Future Challenges in Chips for IoT Nodes: Energy Efficiency - The Wireless Power Issue and Communication - Computation Tradeoff- Opportunities to Achieve Highly Energy-Efficient Processing - Security Challenges in IoT Nodes.									
<b>Unit – II</b>	<b>IoT nodes:</b> Architecture of IoT Nodes - Requirements for IoT Nodes – Power – Cost – Interoperability – Security - Wireless Network Threats - Pairing, Registration, and Installation of IoT Nodes - Impact of Security on Power - Global System Power Optimization.									
<b>Unit – III</b>	<b>Low-Power Digital Architectures for the IOT:</b> Ultra-Low-Power Microcontroller Architectures - Power Management - IO Architecture - Data Processing - Near-Threshold MCU Architectures - From Single Core to Multi Core -Energy Benefits and Challenges for Parallel ULP Processors - Architecture of Memory Subsystem for Parallel ULP Processors.									
<b>Unit – IV</b>	<b>Design Methodologies for IoT Systems on a Chip:</b> Static Power Reduction - Power Gating- Power Gating and Well-Bias - Clamping and Isolation - State Retention with Power Gating - State Retention with Power Gating Optimizations - Active Power Reduction - Voltage Scaling - Clock Gating - Clock Distribution - Clock Tree Synthesis Methodology.									
<b>Unit – V</b>	<b>System Packaging and Assembly in IoT Nodes:</b> Packaging Technology - Current Commercial Packaging Technology for Internet of Things - Integration/Assembly of Multiple Chips (or) PCB Level Packaging - Second Level Packaging - Multiple Chip Integration (or) System in Package.									
<b>REFERENCES:</b>										
1.	Alloto."Enabling the Internet of Things- From Integrated Circuits to Integrated Systems", Springer Publications, 1 <sup>st</sup> Edition,2017.									
2.	Pieter Harpe, Kofi A. A Makinwa, Andrea Baschirotto, "Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design". Springer International Publishing AG,2017									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:						BT Mapped (Highest Level)
On completion of the course, the students will be able to						
CO1	summarize the concepts of IoT					
CO2	understand the components of IoT Nodes					
CO3	infer the low-power digital architectures for IoT					
CO4	develop the design methodologies for IoT systems on a chip					
CO5	understand the system packaging and assembly in IoT nodes					

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	2	2
CO2	3		3	2	2	2
CO3	3		3	2	2	2
CO4	3		3	2	2	2
CO5	3		3	2	2	2

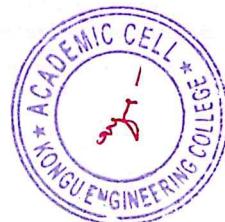
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN – THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		60	40				100
ESE		80	20				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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Board of Studies - <b>ECE</b>	





24VLE15-VLSI FOR BIOMEDICAL APPLICATIONS										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	Low Power VLSI Design	3	PE	45	0	0	45	90	3	
Preamble	To learn the various low power techniques for Biomedical systems									
<b>Unit – I</b>	<b>Low-Power Analog and Biomedical Circuits:</b>									
	Low power transimpedance amplifiers and photo receptors Low power transconductance amplifiers and scaling laws for power in analog circuits- Low-power filters and resonators- Low power current- mode circuits - Ultra-low-power and neuron-inspired analog-to-digital conversion for biomedical system.									
<b>Unit – II</b>	<b>Low-Power RF and Energy-Harvesting Circuits for Biomedical Systems:</b>									
	Wireless inductive power links for medical implants - Energy-harvesting RF antenna power links - Low-power RF telemetry in biomedical implants.									
<b>Unit – III</b>	<b>Biomedical Electronic Systems:</b>									
	Ultra-low-power implantable medical electronics- cochlear implants or bionic ears-an ultra-low power programmable analog bionic ear processor-low power electrode stimulation highly miniature electrode –stimulation –Brain machine interfaces for the blind-Brain machine interface for paralysis, speech, and other disorders. Ultra-low-power noninvasive medical electronics -Analog integrated circuit switched-capacitor model of the heart – the electrocardiogram- A micro power electrocardiogram amplifier -Low-power pulse oximetry.									
<b>Unit – IV</b>	<b>Principles for Ultra-Low-Power Analog and Digital Design:</b>									
	Digital design- Sizing and topologies for robust sub threshold operation-Types of power dissipation-energy efficiency-Optimization of energy efficiency-Varying the power-supply voltage and threshold voltage- Analog and mixed-signal design -Power consumption in analog and digital systems-low power hand- The optimum point for digitization in mixed-signal system Common themes in low-power analog and digital design-The Shannon limit for energy efficiency.									
<b>Unit – V</b>	<b>Bio-Inspired Systems:</b>									
	Neuromorphic electronics- Transmission-line theory- The cochlea: biology, motivations, theory, and RF-cochlea design- Cytomorphic electronics: cell-inspired electronics for systems and synthetic biology- Electronic analogies of chemical reactions- Log-domain current-mode models of chemical reactions and protein-protein networks- Analog circuit models of gene-protein dynamics- Logic-like operations in gene-protein circuits- Circuits-and-feedback techniques for systems and synthetic biology Hybrid analog-digital computation in cells and neurons.									
<b>REFERENCES:</b>										
1.	Rahul Sarpeshkar, "Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems" 1 <sup>st</sup> Edition, Cambridge University Press, 2011.									
2.	Kris Iniewski, "VLSI Circuit Design for Biomedical Applications", 1 <sup>st</sup> Edition, Artech House Publishers, 2008.									
3.	Khandpur RS, "Handbook of Biomedical Instrumentation", McGraw Hill, New Delhi, 2014.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:						BT Mapped (Highest Level)
On completion of the course, the students will be able to						
CO1	acquire the concepts of low power amplifier circuits					
CO2	comprehend RF CMOS circuits for Biomedical applications					
CO3	correlate the analogy of biological components with low power circuits					
CO4	design analog and mixed signal biomedical circuits					
CO5	interpret various bioinspired systems					

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			3	3	3	
CO4			2	3	2	
CO5	3	3	2	2	2	3

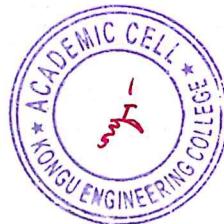
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100					100
CAT2		100					100
CAT3		60	40				100
ESE		80	20				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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Board of Studies - <b>ECE</b>





<b>24VLE16-VLSI TECHNOLOGY</b>										
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>	
<b>Prerequisites</b>	<b>NIL</b>	<b>3</b>	<b>PE</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>	
<b>Preamble</b>	To understand the basic concepts of CMOS fabrication process.									
<b>Unit – I</b>	<b>Crystal Growth and Epitaxy:</b> Silicon Crystal Growth from the Melt- Silicon Float-Zone Process- GaAs Crystal-Growth Techniques -Material Characterization- Epitaxial-Growth Techniques - Structures and Defects in Epitaxial Layers									
<b>Unit – II</b>	<b>Film Formation:</b> Thermal Oxidation- Chemical Vapor Deposition of Dielectrics - Chemical Vapor Deposition of Polysilicon- Atom Layer Deposition- Metallization									
<b>Unit – III</b>	<b>Lithography and Etching:</b> Optical Lithography- Next-Generation Lithographic Methods- Wet Chemical Etching- Dry Etching									
<b>Unit – IV</b>	<b>Impurity Doping:</b> Basic Diffusion Process- Extrinsic Diffusion- Diffusion-Related Processes- Range of Implanted Ions- Implant Damage and Annealing- Implantation-Related Processes									
<b>Unit – V</b>	<b>VLSI Process Integration:</b> Integrated Devices – Passive Components- Bipolar Technology- MOSFET Technology- MESFET Technology- Challenges for Nanoelectronics.									
<b>REFERENCES:</b>										
1.	Simon Sze, Ming-Kwei Lee "Semiconductor Devices Physics and Technology" 3 <sup>rd</sup> Edition, Wiley, 2012, for Units I, II, III, IV, V.									
2.	Sze S.M "VLSI Technology", 2 <sup>nd</sup> , McGraw-Hill New York, 2017.									
3.	Jim Plummer, Michael D. Deal, Peter B. Griffin, "Silicon VLSI Technology: Fundamentals Practice and Modeling", 1 <sup>st</sup> Edition, Prentice Hall India, New Delhi, 2000.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	summarize the approach for wafer preparation, epitaxy and oxidation	Understanding(K2)
CO2	distinguish the various methods for lithography and plasma etching	Understanding(K2)
CO3	illustrate the various deposition and diffusion process	Understanding(K2)
CO4	infer the process of ion implantation and metallization	Understanding(K2)
CO5	understand the various IC technology and package types	Understanding(K2)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		2			2
CO2	2		2			2
CO3	2		2			2
CO4	2		2			2
CO5	2		2			2

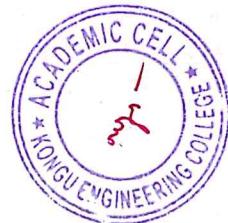
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100				-	100
CAT2		100				-	100
CAT3		100				-	100
ESE		100				-	100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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24VLE17- SUPERVISED MACHINE LEARNING ALGORITHMS										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	3	PE	45	0	0	45	90	3	
Preamble	To focus on supervised machine learning algorithms and to create simple, interpretable models to solve classification and regression problem									
Unit – I	<b>Discriminative Algorithms :</b> Cost function –LMS Algorithm – The normal Equations-Probability interpretation-locally weighted linear regression-logistic regression-generalized linear models-Application to prediction.									
Unit – II	<b>Generative Algorithms :</b> Generative Models: Gaussian Discriminant Analysis (GDA)-Naïve Bayes- Laplace smoothing-Marginal classifier: Support Vector Machine (SVM) as optimal Margin classifier-Application to Classification.									
Unit – III	<b>Multilayer Perceptrons:</b> Multilayer Perceptrons-Implementation of Multilayer Perceptrons-Forward Propagation, Backward Propagation and computer Graphs-Numerical stability and Initialization-Generalization in Deep Learning-Dropout-Case study: House Price Prediction.									
Unit – IV	<b>Convolutional Neural Networks (CNN) :</b> From fully Connected Layers to Convolutions –Convolution for Images-Padding and Stride-Multiple input and multiple output channel-Pooling-Case study: LeNet, Alexnet, VGGnet.									
Unit – V	<b>Recurrent Neural Network(RNN):</b> Working with sequences-Converting Raw Text into Sequence Data-Language model-Recurrent Neural Network-Back Propagation through time-Case study: GRU, LSTM.									
<b>REFERENCES:</b>										
1.	Christopher M. Bishop, "Pattern Recognition and Machine Learning", Springer-Verlag New York. reprint 2010									
2.	Aston Zhang, Zachary C. Lipton, Mu Li, and Alexander J. Smola,"Dive into Deep learning", ebook Published September 19, 2020 <a href="https://d2l.ai/index.html">https://d2l.ai/index.html</a>									
4.	UCI Machine Learning repository: <a href="http://archive.ics.uci.edu/ml/index.php">http://archive.ics.uci.edu/ml/index.php</a>									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:					BT Mapped (Highest Level)
On completion of the course, the students will be able to					
CO1	understand discriminative algorithms for classification and regression problems				Understanding(K2)
CO2	validate a generative model based algorithm for classification and regression problems				Applying (K3)
CO3	understand the designed ANN for a real time application using BPN				Understanding(K2)
CO4	develop a CNN model for image analysis				Applying(K3)
CO5	develop a RNN model for various types of sequence				Applying (K3)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				3	3
CO2	3		3		3	3
CO3	3		3		3	3
CO4	3		3		3	3
CO5	3		3		3	3

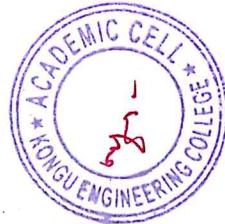
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN – THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		80	20				100
CAT2		80	20				100
CAT3		30	70				100
ESE		50	50				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)


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Board of Studies - <b>ECE</b>





<b>24VLE18-GENETIC ALGORITHMS AND ITS APPLICATIONS</b>										
<b>Programme &amp; Branch</b>	<b>ME &amp; VLSI DESIGN</b>	<b>Sem.</b>	<b>Category</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>SL*</b>	<b>Total</b>	<b>Credit</b>	
<b>Prerequisites</b>	<b>ASIC Design</b>	<b>3</b>	<b>PE</b>	<b>45</b>	<b>0</b>	<b>0</b>	<b>45</b>	<b>90</b>	<b>3</b>	
<b>Preamble</b>	To perform VLSI design optimization, layout generation and chip testing using genetic algorithm for developing efficient computer aided design tools									
<b>Unit – I</b>	<b>Introduction:</b> GA Terminology-The Simple GA-The Steady-State Algorithm-Genetic Operators- GA for VLSI Design, Layout and Test automation									
<b>Unit – II</b>	<b>Partitioning:</b> Problem Description-Circuit Partitioning by Genetic Algorithm-Hybrid Genetic Algorithm for Ratio-Cut Partitioning.									
<b>Unit – III</b>	<b>Standard Cell and Macro Cell Placement &amp; Routing:</b> Standard cell placement-GASP algorithm-Macro Cell Placement-unified algorithm-The Steiner Problem in a Graph-Macro Cell Global Routing.									
<b>Unit – IV</b>	<b>FPGA Technology Mapping and Automatic Test Generation:</b> Circuit Segmentation and FPGA Mapping-Circuit Segmentation for Pseudo-Exhaustive Testing-Test generation in a GA frame work-Deterministic/Genetic Test Generator Hybrids.									
<b>Unit – V</b>	<b>Power Estimation:</b> Application of GA to Peak power estimation –Estimation of Peak Single-Cycle and n-Cycle Powers-Peak Sustainable Power Estimation –Parallel Genetic Algorithms for Automatic Test Generation -problem encoding- fitness function-GA vs Conventional algorithm.									
<b>REFERENCES:</b>										
1.	Pinaki Mazumder, E.M Rudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall,2014.									
2.	Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley 2 <sup>nd</sup> edition, 2004.									
3.	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.									

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:		BT Mapped (Highest Level)
On completion of the course, the students will be able to		
CO1	comprehend the concepts of genetic algorithm and physical design of VLSI systems	Understanding(K2)
CO2	Interpret genetic algorithm for partitioning of VLSI systems	Understanding(K2)
CO3	outline the concepts of genetic algorithm for placement and routing	Understanding(K2)
CO4	infer the basics of automatic test pattern generation and FPGA mapping in VLSI systems	Understanding(K2)
CO5	understand the power estimation in VLSI Layout using Genetic Algorithm	Understanding(K2)

**Mapping of COs with POs**

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				2	2
CO2	3		3		3	2
CO3	3		3		3	2
CO4	3		3		3	2
CO5	3		3		3	2

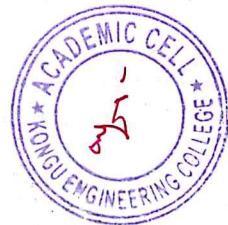
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

**ASSESSMENT PATTERN - THEORY**

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		100	-	-	-	-	100
CAT2		100	-	-	-	-	100
CAT3		100	-	-	-	-	100
ESE		100	-	-	-	-	100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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24GET13 - INNOVATION, ENTREPRENEURSHIP AND VENTURE DEVELOPMENT																	
(Common to ME/MTech and MCA Programmes)																	
Programme & Branch	All ME/MTech and MCA Programmes	Sem.	Category	L	T	P	SL*	Total	Credit								
Prerequisites	Nil	1/3	PE	45	0	0	45	90	3								
Preamble	This course will direct the students on how to employ their innovations towards a successful entrepreneurial venture development.																
Unit – I	<b>Innovation, Entrepreneurship and Design Thinking:</b>								9								
Creativity and Innovation – Types of innovation – challenges in innovation- steps in innovation management- Meaning and concept of entrepreneurship - Role of Entrepreneurship in Economic Development - Factors affecting Entrepreneurship – Entrepreneurship vs Intrapreneurship. Design Thinking and Entrepreneurship – Design Thinking Stages: Empathize – Define – Ideate – Prototype – Test. Design thinking tools: Analogies – Brainstorming – Mind mapping.																	
Unit – II	<b>Product Design:</b>								9								
Techniques and tools for concept generation, concept evaluation – Product architecture –Minimum Viable Product (MVP)- Product prototyping – tools and techniques– overview of processes and materials – evaluation tools and techniques for user-product interaction.																	
Unit – III	<b>Business Model Canvas (BMC) and Business Plan Preparation:</b>								9								
Lean Canvas and BMC - difference and building blocks- BMC: Patterns – Design – Strategy – Process–Business model failures: Reasons and remedies. Objectives of a Business Plan - Business Planning Process and Preparation.																	
Unit – IV	<b>IPR and Commercialization:</b>								9								
Need for Intellectual Property- Basic concepts - Different Types of IPs: Copy Rights, Trademarks, Patents, Geographical Indications, Trade Secrets and Industrial Design– Patent Licensing - Technology Commercialization – Innovation Marketing.																	
Unit – V	<b>Venture Planning and Means of Finance:</b>								9								
Startup Stages - Forms of Business Ownership - Sources of Finance – Idea Grant – Seed Fund – Angel & Venture Fund – Institutional Support to Entrepreneurs – Bank and Institutional Finance to Entrepreneurs.																	
<b>REFERENCES:</b>																	
1.	E. Gordon & K. Natarajan., "Entrepreneurship Development", 6 <sup>th</sup> Edition, Himalaya Publishing House, Mumbai, 2017.																
2.	Sangeeta Sharma, "Entrepreneurship Development", 1 <sup>st</sup> Edition, PHI Learning Pvt. Ltd., New Delhi, 2017.																
3.	Charantimath Poornima M., "Entrepreneurship Development and Small Business Enterprises", 3 <sup>rd</sup> Edition, Pearson Education, Noida, 2018.																
4.	Robert D. Hisrich, Michael P. Peters & Dean A. Shepherd, "Entrepreneurship", 10 <sup>th</sup> Edition, McGraw Hill, Noida, 2018.																

\*includes Term Work(TW) & Online / Certification course hours



COURSE OUTCOMES:											BT Mapped (Highest Level)	
On completion of the course, the students will be able to												
CO1	understand the relationship between innovation and entrepreneurship											Understanding (K2)
CO2	understand and employ design thinking process during product design and development											Analyzing (K4)
CO3	develop suitable business models as per the requirement of the customers											Analyzing (K4)
CO4	practice the procedures for protection of their ideas IPR											Applying (K3)
CO5	understand and plan for suitable type of venture and modes of finances											Applying (K3)

#### Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	2	1				3	2	1	3	2	1	1	
CO2	1	2			3	2	1					1	
CO3	3	1	3			1						1	
CO4	1	2				3						1	
CO5	1	2				3						1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

#### ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		80	20				100
CAT2		50	50				100
CAT3		80	20				100
ESE		70	30				100

\* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

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Board of Studies - Technology

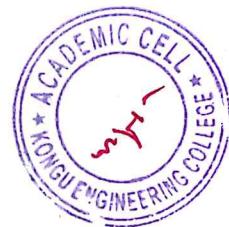
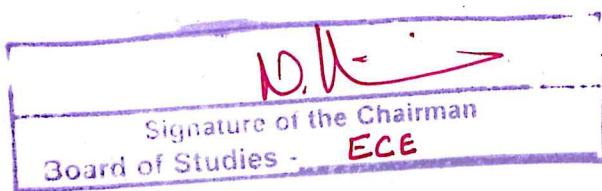




24VLP31 - PROJECT WORK - I												
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit			
Prerequisites	NIL	3	EC	0	0	240	0	240	8			
<b>COURSEOUTCOMES:</b> On completion of the course, the students will be able to									<b>BT Mapped (Highest Level)</b>			
CO1	formulate specific problem statements for ill-defined real life problems with reasonable assumptions and constraints.	Creating (K6), Precision (S3)										
CO2	perform literature review	Evaluating (K5), Precision (S3)										
CO3	conduct experiments, design and analysis, solution iterations and document the results.	Evaluating (K5), Precision (S3)										
CO4	perform error analysis and synthesize the results and arrive at scientific conclusions	Evaluating (K5), Precision (S3)										
CO5	paraphrase the results in the form of technical report and present the findings.	Creating (K6), Precision (S3)										
<b>Mapping of COs with POs</b>												
Cos/Pos	PO1	PO2	PO3	PO4	PO5	PO6						
CO1	3	2	3	3	2	3						
CO2	2	3	2	2	2	3						
CO3	3	2	3	3	3	3						
CO4	3	3	3	3	3	3						
CO5	2	3	2	2	3	3						

1-Slight,2-Moderate,3-Substantial, BT-Bloom's Taxonomy

\*includes Term Work(TW) & Online / Certification course hours





24VLP41 - PROJECT WORK - II										
Programme & Branch	ME & VLSI DESIGN	Sem.	Category	L	T	P	SL*	Total	Credit	
Prerequisites	NIL	4	EC	0	0	360	0	360	12	
<b>COURSE OUTCOMES:</b> On completion of the course, the students will be able to									<b>BT Mapped (Highest Level)</b>	
CO1	formulate specific problem statements for ill-defined real life problems with reasonable assumptions and constraints.									Creating (K6), Precision (S3)
CO2	perform literature review									Evaluating (K5), Precision (S3)
CO3	conduct experiments, design and analysis, solution iterations and document the results.									Evaluating (K5), Precision (S3)
CO4	perform error analysis and synthesize the results and arrive at scientific conclusions									Evaluating (K5), Precision (S3)
CO5	paraphrase the results in the form of technical report and present the findings.									Creating (K6), Precision (S3)
<b>Mapping of COs with POs</b>										
Cos/Pos	PO1	PO2	PO3	PO4	PO5	PO6				
CO1	3	2	3	3	2	3				
CO2	2	3	2	2	2	3				
CO3	3	2	3	3	3	3				
CO4	3	3	3	3	3	3				
CO5	2	3	2	2	3	3				

1-Slight, 2-Moderate, 3-Substantial, BT-Bloom's Taxonomy

\*includes Term Work(TW) & Online / Certification course hours

