KONGU ENGINEERING COLLEGE

(Autonomous Institution Affiliated to Anna University, Chennai)

PERUNDURAI ERODE – 638 060

TAMILNADU INDIA

REGULATIONS, CURRICULUM & SYLLABI – 2022

(CHOICE BASED CREDIT SYSTEM AND OUTCOME BASED EDUCATION)

(For the students admitted during 2022 - 2023 and onwards)

MASTER OF ENGINEERING DEGREE IN VLSI DESIGN

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638060

(An Autonomous Institution Affiliated to Anna University)

REGULATIONS 2022

CHOICE BASED CREDIT SYSTEM AND OUTCOME BASED EDUCATION

MASTER OF ENGINEERING (ME) / MASTER OF TECHNOLOGY (MTech) DEGREE PROGRAMMES

These regulations are applicable to all candidates admitted into ME/MTech Degree programmes from the academic year 2022 – 2023 onwards.

1. DEFINITIONS AND NOMENCLATURE

In these Regulations, unless otherwise specified:

i. "University" means ANNA UNIVERSITY, Chennai.

ii. "College" means KONGU ENGINEERING COLLEGE.

iii. "Programme" means Master of Engineering (ME) / Master of Technology (MTech) Degree programme

iv. "Branch" means specialization or discipline of ME/MTech Degree programme, like Construction Engineering and Management, Information Technology, etc.

v. "Course" means a Theory / Theory cum Practical / Practical course that is normally studied in a semester like Engineering Design Methodology, Machine Learning Techniques, etc.

vi. "Credit" means a numerical value allocated to each course to describe the candidate's workload required per week.

vii. "Grade" means the letter grade assigned to each course based on the marks range specified.

viii. "Grade point" means a numerical value (0 to 10) allocated based on the grade assigned to each course.

ix. "Principal" means Chairman, Academic Council of the College.

x. "Controller of Examinations" means authorized person who is responsible for all examination related activities of the College.

xi. "Head of the Department" means Head of the Department concerned of the College.

2. PROGRAMMES AND BRANCHES OF STUDY

The following programmes and branches of study approved by Anna University, Chennai and All India Council for Technical Education, New Delhi are offered by the College.

Programme	Branch
	Structural Engineering
	VLSI Design
	Embedded Systems
	Computer Science and Engineering
MTech	Information Technology
	Food Technology

3. ADMISSION REQUIREMENTS

Candidates seeking admission to the first semester of the ME/MTech Degree programme shall be required to have passed an appropriate qualifying Degree Examination of Anna University or any examination of any other University or authority accepted by the Anna University, Chennai as equivalent thereto, subject to amendments as may be made by the Anna University, Chennai from time to time. The candidates shall also be required to satisfy all other conditions of admission prescribed by the Anna University, Chennai and Directorate of Technical Education, Chennai from time to time.

4. STRUCTURE OF PROGRAMMES

4.1 Categorisation of Courses

The ME / MTechprogramme shall have a curriculum with syllabi comprising of theory, theory cum practical, practical courses in each semester and project work, internship,etc that have been approved by the respective Board of Studies and Academic Council of the College. All the programmes have well defined Programme Outcomes (PO) and Programme Educational Objectives (PEOs) as per Outcome Based Education (OBE). The content of each course is designed based on the Course Outcomes (CO). The courses shall be categorized as follows:

i. Foundation Courses (FC)

ii. Professional Core (PC) Courses

iii. Professional Elective (PE) Courses

iv. Open Elective (OE) Courses

v. Employability Enhancement Courses (EC) like Innovative Project, Internship cum Project work in Industry or elsewhere, Project Work

4.2 Credit Assignment

Each course is assigned certain number of credits as follows:

Contact period per week	Credits
1 Lecture / Tutorial Period	1
2 Practical Periods	1
2 Project Work Periods	1
40 Training /Internship Periods	1

The minimum number of credits to complete the ME/MTechprogramme is 72.

4.3 Employability Enhancement Courses

A candidate shall be offered with the employability enhancement courses like innovative project, internship cum project work and project work during the programme to gain/exhibit the knowledge/skills.

4.3.1 Innovative Project

A candidate shall earn two credits by successfully completing the project by using his/her innovations in second semester during his/her programme.

4.3.2 Internship cum Project Work

The curriculum enables a candidate to go for full time projects through internship during the third semester and can earn credits through it for his/her academics vide clause 7.6 and clause 7.12. Such candidate shall earn the minimum number of credits as mentioned in the third semester of the curriculum other than internship by either fast track mode or through approved courses in online mode or by self study mode. Such candidate can earn the number of credits for the internship same as that of Project Work in the third semester. Assessment procedure is to be followed as specified in the guidelines approved by the Academic Council.

4.3.4 Project Work

A candidate shall earn nine credits by successfully completing the project work in fourth semester during the programme inside the campus or in industries.

4.4 One / Two CreditCourses / Online Courses / Self Study Courses

The candidates may optionally undergo One / Two Credit Courses / Online Courses / Self Study Courses as elective courses.

4.4.1 One / Two Credit Courses: One / Two Credit Courses shall be offered by the college with the prior approval from respective Board of Studies. A candidate can earn a maximum of six credits through one / two credit courses during the entire duration of the programme.

4.4.2 **Online Courses:** Candidates may be permitted to earn credits for online courses, offered by NPTEL / SWAYAM / a University / Other Agencies, approved by respective Board of Studies.

4.4.3 **Self Study Courses:** The Department may offer an elective course as a self study course. The syllabus of the course shall be approved by the respective Board of Studies. However, mode of assessment for a self study course will be the same as that used for other courses. The candidates shall study such courses on their own under the guidance of member of the faculty. Self study course is limited to one per semester.

4.4.4 The elective courses in the final year may be exempted if a candidate earns the required credits vide clause 4.4.1, 4.4.2 and 4.4.3 by registering the required number of courses in advance (up to second semester).

4.4.5 A candidate can earn a maximum of 15 credits through all one /two credit courses, online courses and self study courses.

4.5 Flexibility to Add or Drop Courses

4.5.1 A candidate has to earn the total number of credits specified in the curriculum of the respective programme of study in order to be eligible to obtain the degree. However, if the candidate wishes, then the candidate is permitted to earn more than the total number of credits prescribed in the curriculum of the candidate's programme.

4.5.2 From the second to fourth semesters the candidates have the option of registering for additional elective courses or dropping of already registered additional elective courses within two weeks from the start of the semester. Add / Drop is only an option given to the candidates. Total number of credits of such courses during the entire programme of study cannot exceed eight.

4.6 Maximum number of credits the candidate can enroll in a particular semester cannot exceed 30 credits.

4.7 The blend of different courses shall be so designed that the candidate at the end of the programme would have been trained not only in his / her relevant professional field but also would have developed to become a socially conscious human being.

4.8 The medium of instruction, examinations and project report shall be English.

5. DURATION OF THE PROGRAMME

5.1 A candidate is normally expected to complete the ME / MTech Degree programme in 4 consecutive semesters (2 Years), but in any case not more than 8 semesters (4 Years).

5.2 Each semester shall consist of a minimum of 90 working days including continuous assessment test period. The Head of the Department shall ensure that every teacher imparts instruction as per the number of periods specified in the syllabus for the course being taught.

5.3 The total duration for completion of the programme reckoned from the commencement of the first semester to which the candidate was admitted shall not exceed the maximum duration specified in clause 5.1 irrespective of the period of break of study (vide clause 11) or prevention (vide clause 9) in order that the candidate may be eligible for the award of the degree (vide clause 16). Extension beyond the prescribed period shall not be permitted.

6. COURSE REGISTRATION FOR THE EXAMINATION

6.1 Registration for the end semester examination is mandatory for courses in the current semester as well as for the arrear courses failing which the candidate will not be permitted to move on to the higher semester. This will not be applicable for the courses which do not have an end semester examination.

6.2 The candidates who need to reappear for the courses which have only continuous assessment shall enroll for the same in the subsequent semester, when offered next, and repeat the course. In this case, the candidate shall attend the classes, satisfy the attendance requirements (vide clause 8), earn continuous assessment marks. This will be considered as an attempt for the purpose of classification.

6.3 If a candidate is prevented from writing end semester examination of a course due to lack of attendance, the candidate has to attend the classes, when offered next, and fulfill the attendance requirements as per clause 8 and earn continuous assessment marks. If the course, in which the candidate has a lack of attendance, is an elective, the candidate may register for the same or any other elective course in the subsequent semesters and that will be considered as an attempt for the purpose of classification.

7. ASSESSMENT AND EXAMINATION PROCEDURE FOR AWARDING MARKS

7.1 The ME/MTechprogrammes consist of Theory Courses, Theory cum Practical courses, Practical courses, Innovative Project, Internship cum Project work and Project Work. Performance in each course of study shall be evaluated based on (i) Continuous Assessments (CA) throughout the semester and (ii) End Semester Examination (ESE) at the end of the semester except for the courses which are evaluated based on continuous assessment only. Each course shall be evaluated for a maximum of 100 marks as shown below:

Sl. No.	Category of Course	Continuous Assessment Marks	End Semester Examination Marks
1.	Theory	40	60
2.	Theory cum Practical (The distribution of marks shall be	50	50
3.	Practical	60	40

4.	Project Work / Internship cum Project Work	50	50
5.	One / Two credit Course	The distribution of marks shall be decided based on the credit weightage assigned	---
6.	All other Courses		

7.2 Examiners for setting end semester examination question papers for theory courses, theory cum practical courses and practical courses and evaluating end semester examination answer scripts, project works, innovative project and internships shall be appointed by the Controller of Examinations after obtaining approval from the Principal.

7.3 Theory Courses

For all theory courses out of 100 marks, the continuous assessment shall be 40 marks and the end semester examination shall be for 60 marks. However, the end semester examinations shall be conducted for 100 marks and the marks obtained shall be reduced to 50. The continuous assessment tests shall be conducted as per the schedule laid down in the academic schedule. Three tests shall be conducted for 50 marks each and reduced to 30 marks each. The total of the continuous assessment marks and the end semester examination marks shall be rounded off to the nearest integer.

7.3.1 The assessment pattern for awarding continuous assessment marks shall be as follows:

Sl. No.	Type	Max. Marks	Remarks
1.	Test - I	12.5	---
	Test - II	12.5	
2.	Tutorial / Others (Tutorial/Problem Solving (or) Simulation (or) Simulation & Mini Project (or) Mini Project (or) Case Studies (or) Any other relevant to the course)	10	Type of assessment is to be chosen based on the nature of the course and to be approved by Principal
3.	Assignment / Paper Presentation in Conference / Seminar / Comprehension / Activity based learning / Class notes	05	To be assessed by the Course Teacher based on any one type.
	Total	40	Rounded off to the one decimal place

However, the assessment pattern for awarding the continuous assessment marks may be changed based on the nature of the course and is to be approved by the Principal.

7.3.2 A reassessment test or tutorial covering the respective test or tutorial portions may be conducted for those candidates who were absent with valid reasons

(Sports or any other reason approved by the Principal).

7.3.3 The end semester examination for theory courses shall be for duration of three hours and shall be conducted between November and January during odd semesters and between April and June during even semesters of every year.

7.4 Theory cum Practical Courses

For courses involving theory and practical components, the evaluation pattern as per the clause 7.1 shall be followed. Depending on the nature of the course, the end semester examination shall be conducted for theory and the practical components. The apportionment of continuous assessment and end semester examination marks shall be decided based on the credit weightage assigned to theory and practical components approved by Principal.

7.5 Practical Courses

For all practical courses out of 100 marks, the continuous assessment shall be for 50 marks and the end semester examination shall be for 50 marks. Every exercise / experiment shall be evaluated based on the candidate's performance during the practical class and the candidate's records shall be maintained.

7.5.1 The assessment pattern for awarding continuous assessment marks for each course shall be decided by the course coordinator based on rubrics of that particular course, and shall be based on rubrics for each experiment.

7.5.2 The end semester examination shall be conducted for a maximum of 100 marks for duration of 3 hours and reduced to 40 marks. The appointment of examiners and the schedule shall be decided by chairman of Board of Study of the relevant board.

7.6 Project Work

7.6.1 Project work shall becarried out individually. Candidates can opt for full time internship (vide clause 7.7) in lieu of project work in third semester. The project work is mandatory for all the candidates.

7.6.2 The Head of the Department shall constitute review committee for project work. There shall be two assessments by the review committee during the semester. The candidate shall make presentation on the progress made by him/her before the committee.

7.6.3 The continuous assessment and end semester examination marks for Project Work and the Viva-Voce Examination shall be distributed as below.

Continuous Assessment (Max. 50 Marks)						End Semester Examination (Max. 50 Marks)			
Review I (Max..10 Marks)		Review II (Max.. 20 Marks)		Review III (Max. 20 Marks)		Report Evaluation (Max. 20 Marks)	Viva - Voce (Max. 30 Marks)		
Rv. Com	Guide	Review Committee (excluding guide)	Guide	Review Committee (excluding guide)	Guide	Ext. Exr.	Guide	Exr.1	Exr.2
5	5	10	10	10	10	20	10	10	10

7.6.4 The Project Report prepared according to approved guidelines and duly signed by the Supervisor shall be submitted to Head of the Department. A candidate must submit the project report within the specified date as per the academic schedule of the semester. If the project report is not submitted within the specified date then the candidate is deemed to have failed in the Project Work and redo it in the subsequent semester. This applies to both Internship cum Project work and Project work.

7.6.5 If a candidate fails to secure 50% of the continuous assessment marks in the project work, he / she shall not be permitted to submit the report for that particular semester and shall have to redo it in the subsequent semester and satisfy attendance requirements.

7.6.6 Every candidate shall, based on his/her project work, publish a paper in a reputed journal or reputed conference in which full papers are published after usual review. A copy of the full paper accepted and proof for that shall be produced at the time of evaluation.

7.6.7 The project work shall be evaluated based on the project report submitted by the candidate in the respective semester and viva-voce examination by a committee consisting of two examiners and guide of the project work.

7.6.8 If a candidate fails to secure 50 % of the end semester examination marks in the project work, he / she shall be required to resubmit the project report within 30 days from the date of declaration of the results and a fresh viva-voce examination shall be conducted as per clause 7.6.7.

7.6.9 A copy of the approved project report after the successful completion of viva-voce examination shall be kept in the department library.

7.7 Internship cum Project Work

Each candidate shall submit a brief report about the internship undergone and a certificate issued from the organization concerned at the time of Viva-voce examination to the review committee. The evaluation method shall be same as that of the Project Work as per clause 7.6 excluding 7.6.6.

7.8 One / Two Credit Course

Two assessments shall be conducted during the value added course duration by the offering department concerned.

7.9 Online Course

The Board of Studies will provide methodology for the evaluation of the online courses. The Board can decide whether to evaluate the online courses through continuous assessment and end semester examination or through end semester examination only. In case of credits earned through online mode from NPTEL / SWAYAM / a University / Other Agencies approved by Chairman, Academic Council, the credits may be transferred and grades shall be assigned accordingly.

7.10 Self Study Course

The member of faculty approved by the Head of the Department shall be responsible for periodic monitoring and evaluation of the course. The course shall be evaluated through continuous assessment and end semester examination. The evaluation methodology shall be the same as that of a theory course.

7.11 Audit Course

A candidate may be permitted to register for specific course not listed in his/her programme curriculum and without undergoing the rigors of getting a 'good' grade, as an Audit course, subject to the following conditions.

The candidate can register only one Audit course in a semester starting from second semester subject to a maximum of two courses during the entire programme of study. Such courses shall be indicated as 'Audit' during the time of Registration itself. Only courses currently offered for credit to the candidates of other branches can be audited.

A course appearing in the curriculum of a candidate cannot be considered as an audit course. However, if a candidate has already met the Professional Elective and Open Elective credit requirements as stipulated in the curriculum, then, a Professional Elective or an Open Elective course listed in the curriculum and not taken by the candidate for credit can be considered as an audit course.

Candidates registering for an audit course shall meet all the assessment and examination requirements (vide clause 7.3) applicable for a credit candidate of that course. Only if the candidate obtains a performance grade, the course will be listed in the semester Grade Sheet and in the Consolidated Grade Sheet along with the grade SC (Successfully Completed). Performance grade will not be shown for the audit course.

Since an audit course has no grade points assigned, it will not be counted for the purpose of GPA and CGPA calculations.

8. REQUIREMENTS FOR COMPLETION OF A SEMESTER

8.1 A candidate who has fulfilled the following conditions shall be deemed to have satisfied the requirements for completion of a semester and permitted to appear for the examinations of that semester.

8.1.1 Ideally, every candidate is expected to attend all classes and secure 100 % attendance. However, a candidate shall secure not less than 80 % (after rounding off to the nearest integer) of the overall attendance taking into account the total number of working days in a semester.

8.1.2 A candidate who could not satisfy the attendance requirements as per clause 8.1.1 due to medical reasons (hospitalization / accident / specific illness) but has secured not less than 70 % in the current semester may be permitted to appear for the current semester examinations with the approval of the Principal on payment of a condonation fee as may be fixed by the authorities from time to time. The medical certificate needs to be submitted along with the leave application. A candidate can avail this provision only twice during the entire duration of the degree programme.

8.1.3 In addition to clause 8.1.1 or 8.1.2, a candidate shall secure not less than 60 % attendance in each course.

8.1.4 A candidate shall be deemed to have completed the requirements of study of any semester only if he/she has satisfied the attendance requirements (vide clause 8.1.1 to 8.1.3) and has registered for examination by paying the prescribed fee.

8.1.5 Candidate's progress is satisfactory.

8.1.6 Candidate's conduct is satisfactory and he/she was not involved in any indisciplined activities in the current semester.

8.2. The candidates who do not complete the semester as per clauses from 8.1.1 to 8.1.6 except 8.1.3 shall not be permitted to appear for the examinations at the end of the semester and not be permitted to go to the next semester. They have to repeat the incomplete semester in next academic year.

8.3 The candidates who satisfy the clause 8.1.1 or 8.1.2 but do not complete the course as per clause 8.1.3 shall not be permitted to appear for the end semester examination of that course alone. They have to repeat the incomplete course in the subsequent semester when it is offered next.

9. REQUIREMENTS FOR APPEARING FOR END SEMESTER EXAMINATION

9.1 A candidate shall normally be permitted to appear for end semester examination of the current semester if he/she has satisfied the semester completion requirements as per clause 8, and has registered for examination in all courses of that semester. Registration is mandatory for current semester examinations as well as for arrear examinations failing which the candidate shall not be permitted to move on to the higher semester.

9.2 When a candidate is deputed for a National / International Sports event during End Semester examination period, supplementary examination shall be conducted for such a candidate on return after participating in the event within a reasonable period of time. Such appearance shall be considered as first appearance.

9.3 A candidate who has already appeared for a course in a semester and passed the examination is not entitled to reappear in the same course for improvement of letter grades / marks.

10. PROVISION FOR WITHDRAWAL FROM EXAMINATIONS

10.1 A candidate may, for valid reasons, be granted permission to withdraw from appearing for the examination in any regular course or all regular courses registered in a particular semester. Application for withdrawal is permitted only once during the entire duration of the degree programme.

10.2 The withdrawal application shall be valid only if the candidate is otherwise eligible to write the examination (vide clause 9) and has applied to the Principal for permission prior to the last examination of that semester after duly recommended by the Head of the Department.

10.3 The withdrawal shall not be considered as an appearance for deciding the eligibility of a candidate for First Class with Distinction/First Class.

10.4 If a candidate withdraws a course or courses from writing end semester examinations, he/she shall register the same in the subsequent semester and write the end semester examinations. A final semester candidate who has withdrawn shall be permitted to appear for supplementary examination to be conducted within reasonable time as per clause 14.

10.5 The final semester candidate who has withdrawn from appearing for project viva-voce for genuine reasons shall be permitted to appear for supplementary viva-voce examination within reasonable time with proper application to Controller of Examinations and on payment of prescribed fee.

11. PROVISION FOR BREAK OF STUDY

11.1 A candidate is normally permitted to avail the authorised break of study under valid reasons (such as accident or hospitalization due to prolonged ill health or any other valid reasons) and to rejoin the programme in a later semester. He/She shall apply in advance to the Principal, through the Head of the Department, stating the reasons therefore, in any case, not later than the last date for registering for that semester examination. A candidate is permitted to avail the authorised break of study only once during the entire period of study for a maximum period of one year. However, in extraordinary situation the candidate may apply for additional break of study not exceeding another one year by paying prescribed fee for the break of study.

11.2 The candidates permitted to rejoin the programme after break of study / prevention due to lack of attendance shall be governed by the rules and regulations in force at the time of rejoining.

11.3 The candidates rejoining in new Regulations shall apply to the Principal in the prescribed format through Head of the Department at the beginning of the readmitted semester itself for prescribing additional/equivalent courses, if any, from any semester of the regulations in-force, so as to bridge the curriculum in-force and the old curriculum.

11.4 The total period of completion of the programme reckoned from the commencement of the semester to which the candidate was admitted shall not exceed the maximum period specified in clause 5 irrespective of the period of break of study in order to qualify for the award of the degree.

11.5 If any candidate is prevented for want of required attendance, the period of prevention shall not be considered as authorized break of study.

11.6 If a candidate has not reported to the college for a period of two consecutive semesters without any intimation, the name of the candidate shall be deleted permanently from the college enrollment. Such candidates are not entitled to seek readmission under any circumstances.

12. PASSING REQUIREMENTS

12.1 A candidate who secures not less than 50 % of total marks (continuous assessment and end semester examination put together) prescribed for the course with a minimum of 45 % of the marks prescribed for the end semester examination in all category of courses vide clause 7.1 except for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course in the examination.

12.2 A candidate who secures not less than 50 % in continuous assessment marks prescribed for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course. If a candidate secures less than 50% in the continuous assessment marks, he / she shall have to re-enroll for the same in the subsequent semester and satisfy the attendance requirements.

12.3 For a candidate who does not satisfy the clause 12.1, the continuous assessment marks secured by the candidate in the first attempt shall be retained and considered valid for subsequent attempts. However, from the fourth attempt onwards the marks scored in the end semester examinations alone shall be considered, in which case the candidate shall secure minimum 50 % marks in the end semester examinations to satisfy the passing requirements, but the grade awarded shall be only the lowest passing grade irrespective of the marks secured.

13. REVALUATION OF ANSWER SCRIPTS

A candidate shall apply for a photocopy of his / her semester examination answer script within a reasonable time from the declaration of results, on payment of a prescribed fee by submitting the proper application to the Controller of Examinations. The answer script shall be pursued and justified jointly by a faculty member who has handled the course and the course coordinator and recommended for revaluation. Based on the recommendation, the candidate can register for revaluation through proper application to the Controller of Examinations. The Controller of Examinations will arrange for revaluation and the results will be intimated to the candidate concerned. Revaluation is permitted only for Theory courses and Theory cum Practical courses where end semester examination is involved.

14. SUPPLEMENTARY EXAMINATION

If a candidate fails to clear all courses in the final semester after the announcement of final end semester examination results, he/she shall be allowed to take up supplementary examinations to be conducted within a reasonable time for the courses of final semester alone, so that he/she gets a chance to complete the programme.

15. AWARD OF LETTER GRADES

For all the passed candidates, the relative grading principle is applied to assign the letter grades.

Marks / Examination Status	Letter Grade	Grade Point
Based on the relative grading	O (Outstanding)	10
	A+ (Excellent)	9
	A (Very Good)	8
	B+ (Good)	7
	B (Average)	6
	C (Satisfactory)	5
Less than 50	U (Reappearance)	0
Successfully Completed	SC	0
Withdrawal	W	-
Absent	AB	-
Shortage of Attendance in a course	SA	-

The Grade Point Average (GPA) is calculated using the formula:

$$\text{GPA} = \frac{\sum[(\text{course credits})\times(\text{grade points})] \text{ for all courses in the specific semester}}{\sum(\text{course credits}) \text{for all courses in the specific semester}}$$

The Cumulative Grade Point Average (CGPA) is calculated from first semester (third semester for lateral entry candidates) to final semester using the formula

$$\text{CGPA} = \frac{\sum[(\text{course credits})\times(\text{grade points})] \text{ for all courses in all the semesters so far}}{\sum(\text{course credits}) \text{for all courses in all the semesters so far}}$$

The GPA and CGPA are computed only for the candidates with a pass in all the courses.

The GPA and CGPA indicate the academic performance of a candidate at the end of a semester and at the end of successive semesters respectively.

A grade sheet for each semester shall be issued containing Grade obtained in each course, GPA and CGPA.

A duplicate copy, if required can be obtained on payment of a prescribed fee and satisfying other procedure requirements.

Withholding of Grades: The grades of a candidate may be withheld if he/she has not cleared his/her dues or if there is a disciplinary case pending against him/her or for any other reason.

16. ELIGIBILITY FOR THE AWARD OF DEGREE

A candidate shall be declared to be eligible for the award of the ME / MTech Degree provided the candidate has

i. Successfully completed all the courses under the different categories, as specified in the regulations.

ii. Successfully gained the required number of total credits as specified in the curriculum corresponding to the candidate's programme within the stipulated time (vide clause 5).

iii. Successfully passed any additional courses prescribed by the respective Board of Studies whenever readmitted under regulations other than R-2020 (vide clause 11.3)

iv. No disciplinary action pending against him / her.

17. CLASSIFICATION OF THE DEGREE AWARDED

17.1 First Class with Distinction:

17.1.1 A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semestersin the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.
- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 8.50

(OR)

17.1.2 Acandidate who joins from other institutions on transfer or a candidate who gets readmitted and has to move from one regulation to another regulation and who qualifies for the award of the degree (vide clause 16) and satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semesters in the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.
- Submission of equivalent course list approved by the respective Board of studies.
- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 9.00

17.2 First Class:

A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class:

- Should have passed the examination in all the courses of all four semesters within six consecutive semesters excluding authorized break of study (vide clause 11) after the commencement of his / her study.
- Withdrawal from the examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 6.50

17.3 Second Class:

All other candidates (not covered in clauses 17.1 and 17.2) who qualify for the award of the degree (vide clause 16) shall be declared to have passed the examination in Second Class.

17.4 A candidate who is absent for end semester examination in a course / project work after having registered for the same shall be considered to have appeared for that examination for the purpose of classification.

18. MALPRACTICES IN TESTS AND EXAMINATIONS

If a candidate indulges in malpractice in any of the tests or end semester examinations, he/she shall be liable for punitive action as per the examination rules prescribed by the college from time to time.

19. AMENDMENTS

Notwithstanding anything contained in this manual, the Kongu Engineering College through the Academic council of the Kongu Engineering College, reserves the right to modify/amend without notice, the Regulations, Curricula, Syllabi, Scheme of Examinations, procedures, requirements, and rules pertaining to its ME / MTechprogramme.

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M.E VLSI DESIGNCURRICULUM – R2022
(For the students admitted from the academic year 2022-23 onwards)

SEMESTER – I									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Theory/Theory with Practical									
22AMT12	Applied Mathematics for Electronics Engineers	3	1	0	4	40	60	100	FC
22GET11	Introduction to Research	2	1	0	3	40	60	100	FC
22VLT11	Advanced Digital System Design	3	1	0	4	40	60	100	PC
22VLT12	VLSI Design Techniques	3	0	0	3	40	60	100	PC
22VLT13	HDL for IC Design	3	0	0	3	40	60	100	PC
22VLT14	Device Modeling	3	0	0	3	40	60	100	PC
Practical / Employability Enhancement									
22VLL11	VLSI Design Laboratory	0	0	2	1	60	40	100	PC
22VLL12	HDL for IC Design Laboratory	0	0	2	1	60	40	100	PC
Total Credits to be earned					**22**				

SEMESTER – II									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Theory/Theory with Practical									
22VLT21	Analog Integrated Circuits	3	0	0	3	40	60	100	PC
22VLT22	Application Specific Integrated Circuits	3	0	0	3	40	60	100	PC
22VLT23	VLSI Signal Processing	3	1	0	4	40	60	100	PC
	Professional Elective – I	3	0	0	3	40	60	100	PE
	Professional Elective – II	3	0	0	3	40	60	100	PE
	Professional Elective - III	3	0	0	3	40	60	100	PE
Practical / Employability Enhancement									
22VLL21	Analog Integrated Circuits Laboratory	0	0	2	1	60	40	100	PC
22VLL22	Application Specific Integrated Circuits Laboratory	0	0	2	1	60	40	100	PC
Total Credits to be earned					**21**				

M.E VLSI DESIGNCURRICULUM – R2022
(For the students admitted from the academic year 2022-23 onwards)

SEMESTER – III									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Theory/Theory with Practical									
	Professional Elective - IV	3	0	0	3	40	60	100	PE
	Professional Elective - V	3	0	0	3	40	60	100	PE
	Professional Elective - VI	3	0	0	3	40	60	100	PE
Practical / Employability Enhancement									
22VLP31	Project Work - I	0	0	16	8	50	50	100	EC
Total Credits to be earned					**17**				

SEMESTER – IV									
Course Code	**Course Title**	**Hours / Week**			**Credit**	**Maximum Marks**			**Category**
		L	**T**	**P**		**CA**	**ESE**	**Total**	
Practical / Employability Enhancement									
22VLP41	Project Work - II	0	0	24	12	50	50	100	EC
Total Credits to be earned					**12**				

Total Credits : 72

PROFESSIONAL ELECTIVES (PEs)						
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**
Semester - II						
Elective – I						
1.	22VLE01	Testing of VLSI Circuits	3	0	0	3
2.	22VLE02	Semiconductor Memory Design	3	0	0	3
3.	22VLE03	Quantum Computing	3	0	0	3
Elective – II						
4.	22VLE04	Low Power VLSI Design	3	0	0	3
5.	22VLE05	Mixed Signal VLSI Design	3	0	0	3
6.	22VLE06	RF Circuit Design	3	0	0	3
Elective - III						
7.	22VLE07	Computer Aided Design of VLSI Circuits	3	0	0	3
8.	22VLE08	VLSI Technology	3	0	0	3
9.	22VLE09	Hardware Software Co-Design	3	0	0	3
Semester - III						
Elective – IV						
10.	22VLE10	System on Chip	3	0	0	3
11.	22VLE11	Reconfigurable Architectures for VLSI	3	0	0	3
12.	22VLE12	Hardware Security	3	0	0	3
Elective - V						
13.	22VLE13	Functional Verification Using HDL	3	0	0	3
14.	22VLE14	VLSI for IOT Systems	3	0	0	3
15.	22VLE15	VLSI for Biomedical Applications	3	0	0	3
Elective – VI						
16.	22VLE16	Network on Chip	3	0	0	3
17.	22VLE17	Supervised Machine Learning Algorithms	3	0	0	3
18.	22VLE18	Genetic Algorithm and Its Applications	3	0	0	3
19.	22GET13	Innovation, Entrepreneurship and Venture Development	3	0	0	3

22AMT12 - APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS							
(Common to VLSI Design and Embedded Systems branches)							
Programme& Branch	**M.E & VLSI Design& Embedded Systems**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**FC**	**3**	**1**	**0**	**4**
Preamble	This course will demonstrate various analytical skills in applied mathematics and use extensive mathematical tools such as linear programming, matrix factorizations and queuing theory with the tactics of problem solving and logical thinking applicable in electronics engineering.						
Unit – I	**Advanced Matrix Theory**:						**9+3**
Positive definite matrices – Cholesky decomposition – Generalized Eigenvectors – QR factorization – Generalized inverses – Singular value decomposition –Least squares solution.							
Unit – II	**Vector Spaces:**						**9+3**
Vector Space – Subspaces – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.							
Unit – III	**Linear Programming:**						**9+3**
Mathematical Formulation of LPP – Basic definitions – Solutions of LPP: Graphical method – Simplex method – Transportation Model – Mathematical Formulation – Initial Basic Feasible Solution: North west corner rule – Vogel's approximation method – Optimum solution by MODI method – Assignment Model – Mathematical Formulation – Hungarian algorithm.							
Unit – IV	**Non-Linear Programming**:						**9+3**
Formulation of non-linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables.							
Unit – V	**Queuing Theory:**						**9+3**
Markovian queues – Single and Multi-server Models – Little's formula – Non- Markovian Queues – PollaczekKhintchine Formula.							
Lecture:45, Tutorial:15, Total:60							

REFERENCES:

1.	Bronson, R., "Schaum's Outline Series of Matrix Operations", 2nd Edition, McGraw-Hill Education, 2011.
2.	Howard Anton, Anton Kaul, "Elementary Linear Algebra" 12th Edition, John Wiley & Sons, 2019.
3.	KantiSwarup, Gupta, P.K and Man Mohan "Operations Research", 20th Revised Edition, Sultan Chand and Sons., New Delhi, 2019.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	apply various methods in matrix theory in communication engineering problems.	Applying (K3)
CO2	apply the concepts of linear algebra to solve practical problems.	Applying (K3)
CO3	formulate mathematical models for linear programming problems and solve the transportation and assignment problems.	Applying (K3)
CO4	use non-linear programming concepts in real life situations.	Applying (K3)
CO5	identify the suitable queuing model to handle communication problems.	Applying (K3)

Mapping of COs with POs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3					
CO2	3					
CO3	3			2	2	
CO4	3			3	3	
CO5	3			3		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	30	60	-	-	-	100
CAT2	10	20	70	-	-	-	100
CAT3	10	20	70	-	-	-	100
ESE	10	30	60	-	-	-	100

* ±3% may be varied (CAT 1,2 & 3 – 50 marks & ESE – 100 marks)

22GET11 - INTRODUCTION TO RESEARCH							
(Common to all ME / MTech Branches & MCA)							
Programme& Branch	**All ME/MTech branches & MCA**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**NIL**	**1 / 2**	**FC**	**2**	**1**	**0**	**3**

Preamble	This course will familiarize the fundamental concepts/techniques adopted in research, problem formulation and patenting. Also will disseminate the process involved in collection, consolidation of published literature and rewriting them in a presentable form using latest tools.	
Unit - I	**Concept of Research:**	**6+3**
Meaning and Significance of Research: Skills, Habits and Attitudes for Research - Time Management - Status of Research in India. Why, How and What a Research is? - Types and Process of Research - Outcome of Research - Sources of Research Problem - Characteristics of a Good Research Problem - Errors in Selecting a Research Problem - Importance of Keywords - Literature Collection – Analysis - Citation Study - Gap Analysis - Problem Formulation Techniques.		
Unit - II	**Research Methods and Journals:**	**6+3**
Interdisciplinary Research - Need for Experimental Investigations - Data Collection Methods - Appropriate Choice of Algorithms / Methodologies / Methods - Measurement and Result Analysis - Investigation of Solutions for Research Problem - Interpretation - Research Limitations. Journals in Science/Engineering - Indexing and Impact factor of Journals - Citations - h Index - i10 Index - Journal Policies - How to Read a Published Paper - Ethical issues Related to Publishing - Plagiarism and Self-Plagiarism.		
Unit - III	**Paper Writing and Research Tools:**	**6+3**
Types of Research Papers - Original Article/Review Paper/Short Communication/Case Study - When and Where to Publish? - Journal Selection Methods. Layout of a Research Paper - Guidelines for Submitting the Research Paper - Review Process - Addressing Reviewer Comments. Use of tools / Techniques for Research - Hands on Training related to Reference Management Software - EndNote, Software for Paper Formatting like LaTeX/MS Office. Introduction to Origin, SPSS, ANOVA etc., Software for detection of Plagiarism.		
Unit - IV	**Effective Technical Thesis Writing/Presentation:**	**6+3**
How to Write a Report - Language and Style - Format of Project Report - Use of Quotations - Method of Transcription Special Elements: Title Page - Abstract - Table of Contents - Headings and Sub-Headings - Footnotes - Tables and Figures - Appendix - Bibliography etc. - Different Reference Formats. Presentation using PPTs.		
Unit - V	**Nature of Intellectual Property:**	**6+3**
Patents - Designs - Trade and Copyright. Process of Patenting and Development: Technological research - innovation - patenting - development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents.		
		Lecture: 30, Tutorial:15, Total:45

REFERENCES:

1.	DePoy, Elizabeth, and Laura N. Gitlin, “Introduction to Research-E-Book: Understanding and Applying Multiple Strategies”, Elsevier Health Sciences, 2015.
2.	Walliman, Nicholas, “Research Methods: The basics”, Routledge, 2017.
3.	Bettig Ronald V., “Copyrighting culture: The political economy of intellectual property”, Routledge, 2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	list the various stages in research and categorize the quality of journals.	Analyzing (K4)
CO2	formulate a research problem from published literature/journal papers	Evaluating (K5)
CO3	write, present a journal paper/ project report in proper format	Creating (K6)
CO4	select suitable journal and submit a research paper.	Applying (K3)
CO5	compile a research report and the presentation	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5
CO1	3	2	1		
CO2	3	2	3		
CO3	3	3	1		
CO4	3	2	1		
CO5	3	2	1		

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying(K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		30	40	30			100
CAT2		30	40	30			100
CAT3			30	40	30		100
ESE		30	40	30			100

* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)

22VLT11- ADVANCED DIGITAL SYSTEM DESIGN							
(Common to VLSI Design and Embedded Systems branches)							
Programme & Branch	**ME - VLSI DESIGN & Embedded Systems**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**3**	**1**	**0**	**4**

Preamble	To design synchronous, asynchronous digital circuits and implement using ASM chart and PLDs	
Unit- I	**Synchronous Sequential Circuit Design:**	9+3
Analysis of Clocked Synchronous Sequential Networks (CSSN) – Modeling of CSSN – State table Reduction – Stable Assignment – Complete Design of CSSN.		
Unit- II	**Algorithmic State Machine (ASM):**	9+3
ASM **–** ASM Chart – Synchronous Sequential Network Design Using ASM Charts – State Assignment –ASM Tables – ASM Realization - Asynchronous Inputs.		
Unit- III	**Asynchronous Circuit Design:**	9+3
Analysis of Asynchronous Sequential Circuit (ASC) - Flow Table Reduction - Racesin ASC – State Assignment Problem and the Transition Table – Design of ASC- Static and Dynamic Hazards – Essential Hazards.		
Unit- IV	**Programming Logic Arrays:**	9+3
PLA minimization – Essential Prime Cube theorem – PLA folding – foldable compatibility matrix - The Compact Algorithm. Practical PLA's – Data Synchronizers – Designing Vending Machine Controller.		
Unit- V	**Programmable Devices:**	9+3
Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL - Realization State machine using PLD Language – FPGAs – ActelACT.		
		Lecture:45, Tutorial:15, Total:60

REFERENCES:

1.	Givone Donald G,"Digital Principles and Design" 1st Edition , McGraw Hill India, reprint 2017.
2.	Yarbrough, JohnM.,"Digital Logic Applications and Design",Cengage Learning India,1st Edition, reprint 2009
3.	BiswasNripendraN,"Logic Design Theory", Prentice Hall of India, New Delhi, reprint 2006.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	design clocked synchronous sequential circuits using state table reduction and assignment	Applying (K3)
CO2	realize functions using algorithmic state machines	Applying (K3)
CO3	design the asynchronous sequential circuit using flowtable reduction and find the hazards in circuits	Applying (K3)
CO4	simplify the Boolean function and implement using Programmable logic array, essential cube theorem and compact algorithm	Applying (K3)
CO5	design the synchronous sequential circuits using Programmable Logic Device, Programmable Array Logic and CPLD	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	3	2		3	3
CO2	3	3	2		2	3
CO3	3	3	2		3	3
CO4	3	3	2		3	3
CO5	3	3	2		3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	5	15	80				100
CAT2	5	15	80				100
CAT3	5	15	80				100
ESE	5	15	80				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLT12 - VLSI DESIGN TECHNIQUES							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**3**	**0**	**0**	**3**
Preamble	To understand the concepts of MOS Transistor characteristics, fabrication process and to design VLSI building blocks						
Unit – I	**Overview of VLSI Design and MOS Transistor:**						**9**
VLSI Design Flow-Design Hierarchy-VLSI Design Styles. Fabrication Process Flow: Basic Steps-The CMOS n-well Process-Layout Design Rules. MOS Transistor: Structure and Operation of the MOS Transistor-MOSFET Current Voltage Characteristics-MOSFET Capacitances.							
Unit – II	**MOS Inverters Characteristics:**						**9**
Static: Resistive Load Inverter-Inverters with MOSFET Load-CMOS Inverter. Switching: Delay Time Definitions-Calculation of Delay Times-Inverter Design with Delay constraints-Switching power Dissipation of CMOS Inverters-Power Delay Product, Energy Delay Product							
Unit – III	**Combinational MOS and Dynamic Logic Circuits:**						**9**
MOS Logic Circuits with Pseudo-nMOS(pMOS) Loads-CMOS Logic Circuits-Complex Logic Circuits-CMOS Transmission Gates-Synchronous Dynamic Circuit Techniques-Dynamic CMOS Circuit Techniques-High performance CMOS Circuits.							
Unit – IV	**Sequential MOS Logic Circuits:**						**9**
Behavior of Bistable Elements-The SR Latch Circuit-Clocked Latch and Flip-flop Circuits-CMOS D Latch and Edge triggered Flip-flop-Sense Amplifier based Flip-flops.							
Unit – V	**VLSI Building Block Design:**						**9**
Arithmetic Building Block: Adders, Multipliers, Shifters, On chip Clock generation and Distribution-Memory Design (SRAM).							
							Total:45

REFERENCES:

1. Sung-Mo Kang, Yusuf Leblebici, ChulwooKim, “CMOS Digital Integrated Circuits Analysis and Design”, Revised 4thEdition, McGraw Hill Education (India) Edition 2019.
2. Neil H.E. Weste, Kamran Eshraghian,” Principles of CMOS VLSI Design”, 3rd Edition, Pearson Education ASIA, 2007.
3. Jan M Rabaey, Anantha P Chandrakasan, BorivojeNikolic, “Digital Integrated Circuits: a Design Perspective”, 2nd Edition, Upper Saddle River, N.J., Pearson Education, 2003.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	comprehend the principles of VLSI Design, MOS Transistor theory and it's fabrication	Understanding(K2)
CO2	interpret the MOS inverter structures with various parameters	Understanding(K2)
CO3	make use of different logic styles for design of high performance CMOS circuits	Applying(K3)
CO4	comprehend the concepts of sequential MOS Logic circuits	Understanding(K2)
CO5	apply data path logic to design various building blocks	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		3		3	3
CO2	3		3		3	3
CO3	3		3		3	3
CO4	3		3	3	3	3
CO5	3		3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	90	-	-	-	-	100
CAT2	10	60	30	-	-	-	100
CAT3	10	55	35	-	-	-	100
ESE	10	60	30	-	-	-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLT13 - HDL FOR IC DESIGN							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**3**	**0**	**0**	**3**
Preamble	To impart knowledge on designing and verification of Integrated Circuits using Verilog Hardware Description Language and System Verilog.						
Unit – I	**Introduction to Verilog:**						**9**
Overview of digital design using Verilog HDL-Hierarchical Modeling concepts-Verilog Operators and Modules-Verilog Ports, Data types and Assignments-Gate level modelling-Switch level modelling-Modelling of CMOS gates and Boolean functions.							
Unit – II	**Dataflow and behavioral modelling:**						**9**
Basics of dataflow modelling-Review of flip-flops-Verilog modeling of flip-flops-Basics of behavioral modelling-Verilog modeling of counters, sequence detector,FSMs and shift registers.							
Unit – III	**Verilog HDL Synthesis:**						**9**
Synthesis Design Flow-Verification of the gate level net list-Modeling for logic synthesis-Example of sequential circuit synthesis - FIR filter implementation-IIR filter implementation							
Unit – IV	**Introduction to System Verilog:**						**9**
Verification Process,- Basic Testbench Functionality - Directed Testing - Constrained-Random Stimulus, Functional Coverage, Testbench Components- Layered Testbench- Building a Layered Testbench- Simulation Environment Phases - Data types and procedural statements: Built-In Data Types- Fixed-Size Arrays- Dynamic Arrays- Queues- Associative Arrays- Array Methods- Choosing a Storage Type- Creating New Types with typedef- Creating User-Defined Structures- Type conversion- Enumerated Types- Task and Function Overview- Routine Arguments- Returning from a Routine.							
Unit – V	**Connecting the Test bench and Design:**						**9**
Separating the Test bench and Design-The Interface Construct-Stimulus Timing-Interface Driving and Sampling-Connecting It All Together-Top-Level Scope-Program – Module Interactions-System Verilog Assertions-The Four-Port ATM Router.							
							Total:45

REFERENCES:

1.	Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2nd Edition, Pearson Education New Delhi, 2019.
2.	Chris Spear, “System Verilog for Verification: A Guide to Learning the Test bench Language Features”, 2nd Edition, Springer, 2012.
3.	https://ocw.mit.edu – Massachusetts Institute of Technology Open Courseware.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	apply digital design concepts and write Verilog programs in gate level and transistor level modeling	Applying (K3)
CO2	write Verilog programs for the digital design using dataflow and behavioral modeling	Applying (K3)
CO3	synthesis the digital system for implementation in FPGA	Applying (K3)
CO4	understand the basic principles of verification process and System Verilog	Understanding(K2)
CO5	interface testbench and design environment	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3
CO4	3	3	3	3	3	3
CO5	3	3	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	30	60				100
CAT2	10	25	65				100
CAT3	10	25	65				100
ESE	10	25	65				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLT14 - DEVICE MODELING							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**3**	**0**	**0**	**3**
Preamble	To understand the solid state devices using mathematical concepts						
Unit – I	**Semiconductor Physics and Modeling of Passive Devices:**						**9**
Quantum Mechanical Concepts- Carrier Concentration- Transport Equation- Mobility and Resistivity- Carrier diffusion-Carrier Generation and Recombination- Continuity equation- Tunneling and High field effects-Modeling of resistors-Modeling of Capacitors-Modeling of Inductors.							
Unit – II	**Diode and Bipolar Device Modeling :**						**9**
Abrupt and linear graded PN junction- Ideal diode current equation- Static, Small signal and Large signal models of PN junction Diode-SPICE model for a Diode- Temperature and Area effects on Diode Model Parameters Transistor Action-Terminal currents -Switching- Static, Small signal and Large signal Eber-Moll models of BJT- temperature and area effects.							
Unit – III	**MOSFET Modeling and Parameter Measurements:**						**9**
MOSFET Fundamentals – Basic Characteristics -Subthreshold region – Types of MOSFET – Threshold Voltage control – MOSFET Scaling - Short channel effects -Models for MOSFET- FinFET-CNTFET.							
Unit – IV	**Noise Models and BSIM4 MOSFET Model:**						**9**
Noise Sources in MOSFET-Flicker Noise Modeling-Thermal Noise Modeling- BSIM4 MOSFET Model-Gate Dielectric Model-Enhanced Models for Effective DC and AC Channel Length and width-Threshold Voltage Model-I-V Model.							
Unit – V	**Other MOSFET Models:**						**9**
EKV Model-Model Features-Long Channel Drain Current Model-Modeling Second order Effects of Drain Current-Effect of Charge Sharing-Modeling of Charge storage Effects-Non-quasi static Modeling-Noise Models-Temperature Effects-MOS Model 9-MOSAI Model.							
							Total:45

REFERENCES:

1.	Massobrio Giuseppe and Antognetti Paolo, “Semiconductor Device Modeling with SPICE”, 2nd Edition, McGraw-Hill Inc, New York, 2010
2.	Sze S. M., “Semiconductor Devices-Physics and Technology”, 3rd Edition, John Wiley and Sons, New York, 2010.
3.	TrondYtterdal,Yuhua Cheng and Tor A.Fjeldly,”Device Modeling for Analog and RF CMOS Circuit Design”John Wiley &Sons Ltd ,2003.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	realize the concepts of semiconductor physics	Understanding(K2)
CO2	understand various mathematical concepts to model semiconductor devices	Understanding(K2)
CO3	apply mathematical concepts to model MOSFET	Applying(K3)
CO4	infer the effects of noise in MOSFET using mathematical concepts.	Understanding(K2)
CO5	comprehend the secondary effects of semiconductor physics using mathematical expressions	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		3	2	3	2
CO2	3		3	2	3	2
CO3	3		3	2	3	2
CO4	3		3	2	3	2
CO5	3		3	2	3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	90					100
CAT2	10	60	30				100
CAT3	10	90					100
ESE	10	70	20				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLL11 - VLSI DESIGN LABORATORY							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**0**	**0**	**2**	**1**

Preamble	**To impart the knowledge of design and layout of digital circuits**

LIST OF EXPERIMENTS / EXERCISES:	
1.	Design and Analysis of CMOS Inverter
2.	Design and Analysis of Basic Logic Gates
3.	Design and Simulation of Combinational Circuits
4.	Design and Simulation of Sequential Circuits
5.	Design and Simulation of Memory Array
6.	Design and Simulation of Logic Designs using Pass Transistor and Transmission Gates
7.	Mini Project in CMOS Digital Circuits
	Total:30

REFERENCES/ MANUAL /SOFTWARE:	
1.	Laboratory Manual
2.	Cadence- Virtuoso

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	design Digital systems at transistor level	Applying (K3),Precision(S3)
CO2	obtain the layout of digital systems	Applying (K3),Precision(S3)
CO3	analyze the characteristics of digital Circuits	Applying (K3),Precision(S3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	**3**	**2**
CO2	3	3	3	3	**3**	**2**
CO3	3	3	3	3	**3**	**2**

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22VLL12 - HDL FOR IC DESIGN LABORATORY							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**1**	**PC**	**0**	**0**	**2**	**1**

Preamble	**To impart the knowledge of design, verification and implementation of digital circuits using Verilog Hardware Description Language and System Verilog**

LIST OF EXPERIMENTS / EXERCISES:

1.	Modeling of Combinational Digital Systems with Test benches
2.	Modeling of Sequential Digital Systems with Test benches
3.	Modeling of CMOS gates and Boolean functions
4.	Modeling of FSM and Memory design with Test benches
5.	Design and implementation of ALU, MAC using FPGA
6.	Mini project

Total:30

REFERENCES/ MANUAL /SOFTWARE:

1.	Laboratory Manual
2.	Modelsim/EDA Tool
3.	Xilinx/EDA Tool

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	design and verification of digital systems using Verilog and system verilog	Applying (K3),Precision(S3)
CO2	design and analysis of analog system using CMOS transistors	Applying (K3),Precision(S3)
CO3	Implement system design in FPGA	Applying (K3),Precision(S3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	**3**	**2**
CO2	3	3	3	3	**3**	**2**
CO3	3	3	3	3	**3**	**2**

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22VLT21 - ANALOG INTEGRATED CIRCUITS							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**3**	**0**	**0**	**3**

Preamble	To focus on the concepts of MOSFETs and design of differential amplifiers, current mirrors, feedback amplifiers and oscillators	
Unit – I	**Basic MOS Device Physics and Single Stage Amplifiers:**	**9**
Basic MOS Device Physics: General Considerations-MOS I/V Characteristics-Second Order effects-MOS Device models. Single Stage Amplifiers: Basic Concepts-Common Source Stage-Source Follower-Common Gate Stage-Cascode Stage.		
Unit – II	**Differential Amplifiers and Current Mirrors:**	**9**
Differential Amplifiers: Single Ended and Differential Operation-Basic Differential Pair-Common-Mode Response- Differential Pair with MOS loads-Gilbert Cell. Passive and Active Current Mirrors: Basic Current Mirrors-Cascode Current Mirrors-Active Current Mirrors.		
Unit – III	**Frequency Response of Amplifiers and Noise:**	**9**
Frequency Response of Amplifiers: General Considerations-Common Source Stage-Source Followers, Common Gate Stage-Cascode Stage-Differential Pair.Noise: Types of Noise-Representation of Noise in circuits-Noise in single stage amplifiers-Noise in Differential Pairs.		
Unit – IV	**Feedback and Operational Amplifiers:**	**9**
Feedback Amplifiers: General Considerations-Feedback Topologies-Effect of Loading. Operational Amplifiers: General Considerations-One Stage Op Amps-Two Stage Op Amps-Gain Boosting-Common–Mode Feedback-Input Range limitations-Slew Rate-Power Supply Rejection.		
Unit – V	**Oscillators and Phase Locked Loops:**	**9**
Oscillators: General Considerations-Ring Oscillators-LC Oscillators. Phase Locked Loops: Simple PLL-Delay Locked Loops-Applications.		
		Total:45

REFERENCES:

1.	BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, Edition 2002, McGraw--Hill Edition reprint 2017.
2.	Paul R.Gray, Paul J. Hurst , Stephen H. Lewis, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, 5th Edition, Wiley, New Delhi, 2013.
3.	David A. Johns, Martin K, “Analog Integrated Circuit Design”, John Wiley& Sons, Inc., New York, 2013.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	comprehend the concepts of MOS device physics and single stage amplifiers.	Understanding(K2)
CO2	design single stage amplifiers, differential amplifiers and current mirrors	Applying (K3)
CO3	examine the frequency response of amplifiers and the effects of noise in amplifiers	Understanding(K2)
CO4	design feedback and operational amplifiers	Applying (K3)
CO5	understand various oscillators and phase locked loops	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	3	3
CO2	3		3	2	3	3
CO3	3		3	2	3	3
CO4	3		3	2	3	3
CO5	3		3	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	70	20	-	-	-	100
CAT2	10	55	35	-	-	-	100
CAT3	10	55	35	-	-	-	100
ESE	10	55	35	-	-	-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLT22 - APPLICATION SPECIFIC INTEGRATED CIRCUITS							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**2**	**PC**	**3**	**0**	**0**	**3**

Preamble	To know the different programmable ASICs, logic cells, I/O cells and interconnect and to learn how synthesis and physical design flow is carried out in an ASIC design.	
Unit – I	**Introduction to ASICs, CMOS Logic and ASIC Library Design:**	**9**
Types of ASICs - Design flow - Combinational logic Cell – Sequential logic cell - Data path logic cell - Transistors as resistors - Transistor parasitic capacitance- Logical effort.		
Unit – II	**Programmable ASICs, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells:**	**9**
Antifuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX - DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.		
Unit – III	**Programmable ASIC Interconnect:**	**9**
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX9000 - Altera FLEX.		
Unit – IV	**Logic Synthesis**	**9**
Design systems - Half gate ASIC –Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation-.Logic synthesis – Logic Simulation - Design and synthesis of various circuits.		
Unit – V	**Physical Design**	**9**
ASIC Partitioning - floor planning- placement and routing – power and clocking strategies - DRC.		
		Total:45

REFERENCES:

1.	Micheal John Sebastian Smith," Application - Specific Integrated Circuits", 12thcompression, Pearson,2013
2.	Steve Kilts, "Advanced FPGA Design: Architecture, Implementation, and Optimization" Wiley Inter-Science, 2016
3.	Roger Woods, John McAllister, Gaye Lightbody, Dr. Ying Yi, "FPGA-based Implementation of Signal Processing Systems", 2ndEdition, Wiley, 2017.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	understand ASIC Design flow and Design Libraries	Understanding(K2)
CO2	understand the ASIC programming technology and programmable ASIC I/O cells	Understanding(K2)
CO3	summarize the architecture of programmable ASIC interconnects	Understanding(K2)
CO4	Infer logic synthesis concept of digital circuits	Understanding(K2)
CO5	apply the algorithms used in partitioning, floorplanning, placement, routing, power and clock design for ASIC	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		3			
CO2	3		3			
CO3	3		3	2	3	
CO4	3		3	3	3	3
CO5	3		3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	90					100
CAT2	10	90					100
CAT3	10	50	40				100
ESE	10	70	20				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLT23 – VLSI SIGNAL PROCESSING							
Programme & Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**3**	**1**	**0**	**4**
Preamble	To design an efficient signal processing architecture for VLSI implementation.						
Unit – I	**Introduction to DSP Systems:**						**9+3**
Introduction To DSP Systems -Typical DSP algorithms; **Iteration Bound** — data flow graph representations, loop bound and iteration bound, Algorithms for computing iteration bound, Iteration Bound of Multirate Data Flow Graphs, Pipelining and parallel processing: Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.							
Unit – II	**Retiming & Unfolding:**						**9+3**
Retiming : Definitions and properties Retiming techniques; Solving systems of inequalities, Retiming Techniques. Unfolding: Algorithm for Unfolding, properties of unfolding, Critical path Unfolding and Retiming applications of Unfolding- sample period reduction and parallel processing application							
Unit – III	**Systolic Architecture Design & Bit Level Arithmetic Architectures:**						**9+3**
Systolic Architecture Design: Design methodology, FIR systolic arrays. BitLevel Arithmetic Architectures: Parallel Multipliers, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic							
Unit – IV	**FastConvolution ,Algorithmic strength reduction & Pipelined and Parallel Recursive filters Adaptive Filters**						**9+3**
Fast Convolution: Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm. Algorithmic strength reduction: Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT. Pipelined and Parallel Recursive filters Adaptive Filters:–Pipelining in first- order IIR filters, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters							
Unit – V	**Scaling, Roundoff Noise, Lattice Structure & Numerical Strength Reduction**						**9+3**
Scaling, Roundoff Noise: Scaling and Round off Noise- State variable Description of digital filters, Scaling and round off noise computation, Round off noise in pipelined I order IIR filters. Lattice Structure: Introduction, Schur algorithm, Digital basic Lattice Filters, Derivation of One-Multiplier Lattice Filter, Derivation of Normalized Lattice filter. Numerical Strength Reduction-Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.							
Lecture :45,Tutorial :15,Total:60							
REFERENCES:							
1.	Keshab K. Parhi, VLSI Digital Signal Processing Systems, Design and Implementation, Student Edition, John Wiley, Inter Science, New York, 2012						
2.	Mohammed Ismail, Terri Fiez, Analog VLSI Signal and Information Processing, McGraw-Hill, New York, 1994.						
3.	Magdy A. Bayoumi, Earl E. Swartzlander, VLSI Signal Processing Technology, Springer US Publishers. 2012						

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	apply pipelining and parallel processing concepts for efficient low power architecture.	Applying(K3)
CO2	apply retiming and unfolding techniques for the design of VLSI architecture.	Applying(K3)
CO3	apply systolic and bit level architectures to improve the efficiency of VLSI circuits.	Applying(K3)
CO4	apply fast convolution algorithms for FIR and IIR filters	Applying(K3)
CO5	use of proper techniques for parallel processing design for scaling and roundoff noise computation	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	3	3		3
CO2	3	2	3	3		3
CO3	3	2	3	3		3
CO4	3	2	3	3		3
CO5	3	2	3	2		3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	20	70			-	100
CAT2	10	20	70			-	100
CAT3	10	20	70			-	100
ESE	5	15	80			-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLL21 - ANALOG INTEGRATED CIRCUITS LABORATORY							
Programme & Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PC**	**0**	**0**	**2**	**1**

Preamble	To impart the knowledge of design, simulate and analysis of analog circuits

LIST OF EXPERIMENTS / EXERCISES:

1.	Perform the Simulation of a Common Source Amplifier
2.	Perform the Simulation of a Cascode Stage Amplifier
3.	Perform the Simulation of a differential amplifier
4.	Analysis of frequency response of voltage series and voltage shunt feedback topologies
5.	Analysis of frequency response of current series and current shunt feedback topologies
6.	Perform the Simulation of a Ring Oscillator
7.	Miniproject

Total:30

REFERENCES/ MANUAL /SOFTWARE:

1.	Laboratory Manual
2.	Cadence-Virtuoso

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	design analog circuits at transistor level	Applying(K3), Precision(S3)
CO2	obtain the simulation of analog designs	Applying (K3), Precision (S3)
CO3	analyze the characteristics of analog Circuits	Analyzing (K4), Precision(S3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22VLL22 - APPLICATION SPECIFIC INTEGRATED CIRCUITS LABORATORY							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**2**	**PC**	**0**	**0**	**2**	**1**

Preamble	To impart the knowledge of physical design of digital circuits

LIST OF EXPERIMENTS / EXERCISES:

1.	Design, simulation and synthesis of Adders
2.	Design, simulation and synthesis of multipliers
3.	Design, simulation and synthesis of memory
	For the following circuits, a) Perform the functional verification b) Synthesis the design c) Generate the layout (Automatic) d) Tabulate the area, power, delay
4.	Universal Asynchronous Receiver Transmitter
5.	Convolutional Neural Network Accelerator
6.	Miniproject

Total:30

REFERENCES/ MANUAL /SOFTWARE:

1.	Laboratory Manual
2.	Cadence

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	perform physical design of digital circuits	Applying(K3), Precision(S3)
CO2	analyze the performance of digital systems	Applying (K3), Precision (S3)
CO3	analyze the characteristics of digital Circuits	Analyzing (K4), Precision(S3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	3	3
CO2	3	3	3	3	3	3
CO3	3	3	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22VLP31 - PROJECT WORK - I							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**EC**	**0**	**0**	**16**	**8**

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	formulate a problem statement for the problem given by the industry.	Applying (K3)
CO2	summarize the literature review	Understanding (K2)
CO3	develop a methodology for the identified problem	Applying (K3
CO4	carry out the experimental work and analyse the performance as per the specified methodology in VLSI domain.	Analyzing (K4)
CO5	prepare and present the project report	Applying (K3)

Mapping of Cos with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	2	3
CO2	2	3	2	2	2	3
CO3	3	2	3	3	3	3
CO4	3	3	3	3	3	3
CO5	2	3	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22VLP41 - PROJECT WORK - II							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**4**	**EC**	**0**	**0**	**16**	**8**

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	formulate a problem statement for the problem given by the industry.	Applying (K3)
CO2	summarize the literature review	Understanding (K2)
CO3	develop a methodology for the identified problem	Applying (K3
CO4	carry out the experimental work and analyse the performance as per the specified methodology in VLSI domain.	Analyzing (K4)
CO5	prepare and present the project report	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	3	3	2	3
CO2	2	3	2	2	2	3
CO3	3	2	3	3	3	3
CO4	3	3	3	3	3	3
CO5	2	3	2	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

22VLE01 - TESTING OF VLSI CIRCUITS (Common to VLSI Design and Embedded Systems branches)							
Programme& Branch	**ME - VLSI DESIGN & ME - EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To know the basics of VLSI test concepts, test generation, DFT architectures, Built in SelfTest, memory testing and test compression.						
Unit – I	**Fault modeling and simulation:**						**9**
Importance of Testing- Challenges in VLSI Testing -Fault models- Logic simulation- Compiled code simulation-Event driven simulation- Fault simulation- Serial fault simulation- Parallel fault simulation- Deductive fault simulation- Concurrent fault simulation							
Unit – II	**Design For Testability:**						**9**
Testability analysis –DFT basics- Scan cell designs- Scan architectures- Scan design rules- Scan design flow							
Unit – III	**Test Generation:**						**9**
Random test generation- Designing a stuck-at model- ATPG for Combinational Circuits- Designing a sequential ATPG- Designing Simulation based ATPG-Hybrid deterministic and simulation based ATPG.							
Unit – IV	**Built In Self-Test:**						**9**
BIST design rules- Test pattern generation- Output response analysis- Logic BIST architectures							
Unit – V	**Test compression and Memory Testing:**						**9**
Test stimulus compression- Code based schemes - RAM functional fault models – Dynamic faults- Functional test patterns and algorithms-March tests-Word-oriented memory- Multi-port memory.							
							Total:45

REFERENCES:

1. Laung – Terngwang, Cheng – wen wu, Xidogingwen, “VLSI Testing Principles and Architectures: Design for Testability”, Morgan Kaufmann Publisher, 2011.
2. Abramovici, M., Breuer, M.A and Friedman, A.D., “Digital Systems and Testable Design”, Jaico Publishing House, 2014.
3. Bushnell, M.L and. Agrawal, V.D., “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	distinguish between different fault models and types of simulation	Understanding (K2)
CO2	identify the design for testability techniques for combinational and sequential circuits	Understanding (K2)
CO3	apply various test generation methods for combinational and sequential circuits	Applying (K3)
CO4	compare the various Built In Self-Test architectures	Understanding (K2)
CO5	understand the various fault models for memory, test generation algorithms for memories and test compression approaches	Understanding (K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	3	3
CO2	3		3	2	3	3
CO3	3		3	2	3	3
CO4	3		3	2	3	3
CO5	3		3	2	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	55	30				100
CAT3	15	85					100
ESE	5	80	15				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE02 - SEMICONDUCTOR MEMORY DESIGN							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To study the architectures of SRAM and DRAM and to understand the concepts of various non-volatile memories, fault modeling, memory testing and various packaging technologies						
Unit – I	**Random Access Memory Technologies:**						**9**
SRAM cell structures-MOS SRAM architecture-MOS SRAM cell and Peripheral circuit operation- Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology- CMOS DRAMs- DRAMs cell theory and advanced cell structures- BiCMOS, DRAMs- Soft error failures in DRAMs							
Unit – II	**Nonvolatile Memories:**						**9**
Masked Read-Only Memories (ROMs)- High Density ROMs- Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOSPROMs- Erasable(UV) Programmable Road-Only Memories (EPROMs)- Floating-Gate PROM Cell- One-Time Programmable (OTP)EPROMS- Electrically Erasable PROMs (EEPROMs)- EEPROM technology and Architecture- Nonvolatile SRAM							
Unit – III	**Memory Fault Modeling And Testing:**						**9**
RAM Fault Modeling, Electrical Testing, Peusdo Random Testing – Megabit DRAM Testing –Nonvolatile Memory Modeling and Testing – IDDQ Fault Modeling and Testing – Application Specific Memory Testing.							
Unit – IV	**Semiconductor Memory Reliability:**						**9**
Generalability Issues – RAM Failure Modes and Mechanism – Nonvolatile Memory-Reliability Modeling and Failure Rate Prediction – Design for Reliability-Reliability Test Structures.							
Unit – V	**Packaging Technologies:**						**9**
Ferroelectric Random Access Memories (FRAMs)- Gallium Arsenide (GaAs) FRAMs- Analog Memories- Magnetoresistive Random Access Memories (MRAMs)- Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and reliability issues-Memory cards- High density memory packaging future directions.							
							Total:45

REFERENCES:

1. Sharma, Ashok K.,“SemiconductorMemories:Technology,Testing,andReliability”,Wiley-IEEE Press, NewYork, 2014.
2. Sharma, Ashok K., “Advanced Semiconductor Memories: Architectures, Designs And Application”, Wiley-IEEE Press, 2014.
3. Sharma, Ashok K., “Semiconductor Memories”, 2 Volume Set, Wiley, IEEE Press 2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	Comprehend the structures of random access memories	Understanding(K2)
CO2	Understand the need of non-volatile memories and their applications	Understanding(K2)
CO3	interpret the fault free memory systems by fault modeling techniques	Understanding(K2)
CO4	Demonstrate the memory architectures with reliability	Understanding(K2)
CO5	Identify the packages for memories	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		2	2		2
CO2	3		2	2		2
CO3	2		2	2		2
CO4	3		2	2		2
CO5	2		2	2		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	85					100
CAT3	15	85					100
ESE	10	90					100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE03 - QUANTUM COMPUTING							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To understand the concepts of quantum information theory, quantum algorithms and physical realization of systems						
Unit – I	**Introduction:**						**9**
Global perspectives – Linear algebra-The postulates of quantum mechanics- Application :super dense coding-EPR and the Bellin equality							
Unit – II	**Quantum circuits:**						**9**
Single qubit operations-Controlled operations–Measurement –Universal quantum gates-Quantum circuit model of computation-Simulation of quantum systems							
Unit – III	**Quantum algorithms:**						**9**
The quantum Fourier transform-Phase estimation–Order finding and factoring- The quantum search algorithm							
Unit – IV	**Quantum Information:**						**9**
Quantum information theory –Quantum error-correction-Fault-tolerant quantum computation-Quantum cryptography.							
Unit – V	**Quantum computers(physical realization):**						**9**
Guiding principles - Conditions for quantum computation - Optical photon quantum computer - Optical cavity quantum electrodynamics –Ion traps-Nuclear magnetic resonance-Other implementation schemes.							
							Total:45
REFERENCES:							
1.	Michael A. Nielsen & Isaac L. Chuang, “Quantum Computation and Quantum Information”,Cambridge University Press, 2013.						
2.	Eleanor G. Rieffel, Wolfgang H. Polak, “Quantum Computing: A Gentle Introduction”, MIT Press, 2014.						
3.	Scott Aaronson, “Quantum Computing since Democritus”, Cambridge University Press, 2013.						

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	Describe the quantum mechanics using linear algebra	Understanding(K2)
CO2	interpret Qubits and design quantum gates	Understanding(K2)
CO3	demonstrate the quantum parallelism by using quantum algorithms	Understanding(K2)
CO4	Understand real-world quantum information processing	Understanding(K2)
CO5	infer the basic knowledge on physical realization of quantum computers	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2		2	2
CO2	3		2		2	2
CO3	3		2		2	2
CO4	3		2		2	2
CO5	3		2		2	2

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	85					100
CAT3	15	85					100
ESE	10	90					100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE04 - LOW POWER VLSI DESIGN
(Common to VLSI Design and Embedded Systems branches)

Programme& Branch	ME - VLSI DESIGN & ME - EMBEDDED SYSTEMS	Sem.	Category	L	T	P	Credit
Prerequisites	**VLSI Design Techniques**	**2**	**PE**	**3**	**0**	**0**	**3**

Preamble	To design a low power digital circuits and analyze the various power optimization methods	
Unit – I	**Sources of Power Dissipation and Power Optimization:**	**9**
Components of power dissipation in CMOS Circuits- Logic level power optimization- Problem formulation- Combinational circuits Technology independent optimization- Sequential circuits -Technology independent optimization- Technology-dependent optimization		
Unit – II	**Circuit Level Techniques for Low Power Design:**	**9**
Circuit level low-power design- Logic style- Latches and Flip-flops- Transistor sizing and ordering- Drivers for large load- Power, and Delay in CMOS circuits- CMOS circuit design styles for adders- Power delay and area comparisons for 4-bit RCA, adders and multipliers		
Unit – III	**Low Power System Design:**	**9**
Conventional arithmetic and low power design- Logarithmic Number System- Residue Number System- Reducing power consumption in memories- Static random access memories- Dynamic random access memories		
Unit – IV	**Low Power Clock Design and Power Estimation:**	**9**
Low-Power Clock Design- Interconnect Delays- Classification of power estimation methodologies- Simulation based power estimation- Probabilistic methods.		
Unit – V	**Software Design for Low Power:**	**9**
Sources of software power dissipation- Software power estimation- Software power optimization- Automated low power code generation- Co-design for low power.		
		Total:45

REFERENCES:

1.	Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002.
2.	Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2018.
3.	Ajit Pal, “Low-Power VLSI Circuits and Systems”, 1st Edition, Springer 2015.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	enumerate the different sources of power dissipation in CMOS and various logic level power optimization techniques	Understanding (K2)
CO2	apply various power optimization techniques at circuit level.	Applying (K3)
CO3	design low power circuits at architecture level and memories	Applying (K3)
CO4	outline simulation and probabilistic method of power analysis and low power issues at low level design	Understanding (K2)
CO5	perform power estimation and optimization at programming level	Understanding (K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		3	3	3	3
CO2	3		3	3	3	3
CO3	3		3	3	3	3
CO4	3		3	3	3	3
CO5	3		3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	65	20				100
CAT2	15	35	50				100
CAT3	15	85					100
ESE	10	60	30				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE05 - MIXED SIGNAL VLSI DESIGN							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To build the advanced CMOS VLSI Design with practical aspect of mixed signal VLSI blocks						
Unit – I	**Comparators and Switching circuits:**						**9**
Characterization of a comparator – two stage, open loop comparators-switched capacitor circuits – switched capacitor amplifiers-switched capacitor integrators.							
Unit – II	**Continuous Time Filters:**						**9**
Introduction to continuous time filters: First and Second order filters - introduction to Gm - C filters - CMOS transconductors using Triode transistors- bipolar transconductors- BiCMOS transconductors – MOSFET C Filters - Tuning circuitry							
Unit – III	**Digital To Analog& Analog To Digital Converters:**						**9**
Ideal D/A Converter- ideal A/D converter- Types of DAC's: binary scaled converters – hybrid converters. Types of ADC's: successive approximation converters-pipelined A/D converters – flash converters-two step A/D converters- folding A/D converters.							
Unit – IV	**Over sampling converters:**						**9**
Over sampling without noise shaping- oversampling with noise shaping – digital decimation filter-system architecture: system architecture of delta sigma A/D converters- system architecture of delta sigma D/A converters- higher order modulators.							
Unit – V	**Phase- locked loops:**						**9**
Basic phase locked loop architecture- linearized small signal analysis- jitter and phase noise- electronic oscillators- jitter and phase noise in PLLs.							
							Total:45
REFERENCES:							
1.	Tony Chan Carusone, David Johns, Kenneth Martin, Analog Integrated Circuit Design, 2nd Edition, John Wiley and Sons, 2013						
2.	Rudy van de Plassche, Integrated Analog-to-Digital and Digital-to-Analog Converters, 2nd Edition, Springer, 2007.						
3.	Phillip Allen, Douglas Holberg, CMOS Analog Circuit Design, 2nd Edition, Oxford University Press, 2013.						

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped** **(Highest Level)**
CO1	comprehend the concepts of switched capacitor circuits and comparators	Understanding (K2)
CO2	comprehend the concepts of continuous time filters and its performance	Understanding (K2)
CO3	illustrate Digital To Analog & Analog To Digital Converters	Understanding (K2)
CO4	comprehend sigma delta converters	Understanding (K2)
CO5	infer the working of PLL	Understanding (K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		2	3	2	3
CO2	2		2	3	2	3
CO3	3		3	3	2	3
CO4	3		3	3	2	3
CO5	3		3	3	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	85					100
CAT2	15	85					100
CAT3	15	85					100
ESE	10	90					100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE06 - RF CIRCUIT DESIGN							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Analog IC Design**	**2**	**PE**	**3**	**0**	**0**	**3**

Preamble	To infer the concepts of CMOS RF circuits and systems at microwave regime.	
Unit – I	**CMOS PHYSICS,TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES:**	**9**
Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port noise theory, Noise figure, THD, IP2, IP3, sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne receiver, Heterodyne receiver, Image reject, Low IF receiver architectures direct up conversion transmitter, Two step up conversion transmitter		
Unit – II	**IMPEDANCE MATCHING AND AMPLIFIERS:**	**9**
S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.		
Unit – III	**FEEDBACK SYSTEMS AND POWER AMPLIFIERS:**	**9**
Stability of feedback systems: Gain and phase margin, Root- locus techniques, Time and Frequency domain considerations, Compensation, General model— Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations		
Unit – IV	**MIXERS AND OSCILLATORS:**	**9**
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.		
Unit – V	**PLL AND FREQUENCY SYNTHESIZERS:**	**9**
Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-frequency synthesizers, Direct Digital Frequency synthesizers		
		Total:45

REFERENCES:

1.	T.Lee, “Design of CMOS RF Integrated Circuits”, World Scientific Publishing Co Pvt. Ltd.,1st edition 2010.
2.	B.Razavi,“RF Microelectronics”, Pearson Education India; 2nd edition, 2013.
3.	JanCrols, Michiel Steyaert,“CMOS Wireless Transceiver Design”,Springer India, 2015.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	differentiate the noises associated with CMOS technology and to comprehend the RF receiver operation	Understanding(K2)
CO2	infer the input and output impedance matching networks for amplifier design	Understanding(K2)
CO3	demonstrate the RF power amplifier design with the context of stability	Understanding(K2)
CO4	Interpret the design of RF mixers and oscillators for IC implementation	Understanding(K2)
CO5	summarize the PLL and synthesizer architectures and their performance	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		2	2	2	2
CO2	3		2	2	2	2
CO3	3		2	2	2	2
CO4	3		2	2	2	2
CO5	3		2	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	85					100
CAT2	15	85					100
CAT3	15	85					100
ESE	10	90					100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE07 - COMPUTER AIDED DESIGN OF VLSI CIRCUITS							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**ASIC Design**	**2**	**PE**	**3**	**0**	**0**	**3**

Preamble	To give an overview of the VLSI physical design and understand CAD algorithms used in VLSI physical design automation field	
Unit – I	**Design Methodologies:**	**9**
Introduction to VLSI design methodologies – Review of VLSI design automation tools –Algorithmic graph theory and Computational complexity –Tractable and intractable problems – general purpose methods for combinatorial optimization problems		
Unit – II	**Partitioning, Placement and Floor planning :**	**9**
Placement and partitioning –circuit representation – Placement algorithms –Genetic algorithm for standard-cell Placement(GASP) Partitioning- Partitioning algorithms-Floor planning concepts –shape functions and floor plan sizing –Floor planning based on Simulated Annealing		
Unit – III	**Routing and Compaction:**	**9**
Routing – Types of local routing problems – area routing – channel routing – global routing –algorithms for global routing. Compaction- Layout Compaction –Design rules –problem formulation –algorithms for constraint graph compaction.		
Unit – IV	**Logic Simulation**:	**9**
Simulation –Gate-level modeling and simulation –Switch-level modeling and simulation. Introduction to Combinational Logic Synthesis–Binary Decision Diagrams –ROBDD- ROBDD principles, implementation, construction and manipulation.		
Unit – V	**High level Synthesis** :	**9**
Hardware models –Internal representation –Allocation assignment and scheduling –Simple scheduling algorithm –Assignment problem–High level transformations.		
		Total:45

REFERENCES:

1.	Gerez, S.H., “Algorithms for VLSI Design Automation”, John Wiley & Sons, New York, 2002
2.	Sherwani, N.A., “Algorithms for VLSI Physical Design Automation”, Kluwar Academic Publishers, Boston, 2002
3.	Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill International Edition 1995

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	outline the concepts and properties associated with graph theory	Understanding(K2)
CO2	inference the concepts of physical design process such as partitioning, floor planning and placement	Applying (K3)
CO3	comprehend the concepts of physical design process such as routing and compaction	Applying (K3)
CO4	utilize the concepts of simulation in VLSI physical design automation	Applying (K3)
CO5	understand the concepts of synthesis in VLSI physical design automation	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		2		3	
CO2	3	3	3		3	3
CO3	3	3	3		3	3
CO4	3		3		3	3
CO5	3		3		3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	50	35	-	-	-	100
CAT2	10	20	70	-	-	-	100
CAT3	15	50	35	-	-	-	100
ESE	10	35	55	-	-	-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE08 - VLSI TECHNOLOGY							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**

Preamble	To understand the basic concepts of CMOS fabrication process.	
Unit – I	**Crystal growth, Wafer preparation, Epitaxy and Oxidation:**	**9**
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Polysilicon, Oxidation induced Defects.		
Unit – II	**Lithography and Relative Plasma Etching:**	**9**
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, reactive Plasma Etching techniques and Equipment.		
Unit – III	**Deposition and Diffusion:**	**9**
Deposition process, Polysilicon, Silicon Dioxide- Silicon Nitride- plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques		
Unit – IV	**Ion implementation and Metallization:**	**9**
Range theory- Implantation equipment - Annealing-Shallow junctions – High energy implantation – Metallization Applications-Metallization choices- Physical vapor deposition – Patterning.		
Unit – V	**VLSI Process Integration and Packaging of VLSI Devices:**	**9**
NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology – Bipolar IC Technology – IC Fabrication. Package types– banking design consideration – VLSI assembly technology – Package fabrication technology		
		Total:45

REFERENCES:

1.	Sze S.M, "VLSI Technology", 2nd edition, McGraw-Hill New York, 2017.
2.	Amar Mukherjee," Introduction to NMOS and CMOS VLSI System Design", 1st Edition, Prentice Hall India, New Delhi, 2000.
3.	Jim Plummer, Michael D. Deal, Peter B. Griffin, "Silicon VLSI Technology: Fundamentals Practice and Modeling", 1stEdition, Prentice Hall India, New Delhi, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	summarize the approach for wafer preparation, epitaxy and oxidation	Understanding(K2)
CO2	distinguish the various methods for lithography and plasma etching	Understanding(K2)
CO3	illustrate the various deposition and diffusion process	Understanding(K2)
CO4	infer the process of ion implantation and metallization	Understanding(K2)
CO5	understand the various IC technology and package types	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		2			2
CO2	2		2			2
CO3	2		2			2
CO4	2		2			2
CO5	2		2			2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85				-	100
CAT2	15	85				-	100
CAT3	15	85				-	100
ESE	10	90				-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE09 - HARDWARE SOFTWARE CO-DESIGN							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**2**	**PE**	**3**	**0**	**0**	**3**
Preamble	To understand an integrated application development environment of hardware/software codesign in embedded system.						
Unit – I	**Design Consideration:**						**9**
Platform - Based Design – System Modeling – Video Coding – Image Processing – Cryptography - Digital Communication.							
Unit – II	**System Level Design:**						**9**
Abstraction Levels–Algorithm Level Verification–Transaction Level Modeling–System Level Development Tools.							
Unit – III	**Embedded Processor Design**						**9**
Specific Instruction-Set-Data Level Parallelism–Instruction Level Parallelism–Thread Level Parallelism							
Unit – IV	**Parallel Compiler:**						**9**
Vectorization-Simdization–ILPScheduling–Threading-CompilerTechnique–Compiler Infrastructures							
Unit – V	**Real-Time Operating System for PLX:**						**9**
PRRP Scheduler-Memory Management–Communication and Synchronization Primitives- Multimedia Applications in RTOS for PLX–Application Development Environment.							
							Total:45

REFERENCES:

1. Sao-jieChen ,Guang - Huei Lin, Pao -Ann Hsiung and Yu-Hen Hu, "Hardware Software Co-Design of a Multimedia SOC Platform" Illustrated Edition, Springer, 2009.
2. Patrick Schaumont, “A Practical Introduction to Hardware/Software Codesign”, 2nd Edition, Springer, 2010.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Publication, reprint 2007.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	acquire knowledge about system level modeling in image and video encoding	Understanding(K2)
CO2	perform algorithm level verification and work with system development tools	Understanding(K2)
CO3	distinguish between different levels of parallelism	Understanding(K2)
CO4	infer scheduling and compiler techniques	Understanding(K2)
CO5	apply the integrated application development environment for hardware/software codesign of embedded system	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	**3**		**3**			
CO2	**3**		**3**		**3**	**3**
CO3	**3**		**3**			
CO4	**3**		**3**			
CO5	**3**		**3**		**3**	**3**

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	85					100
CAT2	15	85					100
CAT3	15	50	35				100
ESE	10	90					100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE10 - SYSTEM ON CHIP							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To infer the concepts of hardware and software on a chip and to discuss the applications and implementations of system on chip using different communication architectures	
Unit – I	**Introduction to the Systems Approach:**	**9**
System Architecture: An Overview - Components of the System - Hardware and Software: Programmability Versus Performance - Processor Architectures - Memory and Addressing - System-Level Interconnection - An Approach for SOC Design - System Architecture and Complexity - Product Economics and Implications for SOC.		
Unit – II	**Chip Basics:**	**9**
Cycle Time - Die Area and Cost - Ideal and Practical Scaling - Power - Area – Time – Power Trade - Offs in Processor Design - Reliability – Configurability		
Unit – III	**Processors:**	**9**
Processor Selection for SOC - Basic Concepts in Processor Architecture - Basic Concepts in Processor Micro architecture - Basic Elements in Instruction Handling-Buffers: Minimizing Pipeline Delays - Branches: Reducing the Cost of Branches - Vector Processors and Vector Instruction Extensions - VLIW Processors - Superscalar Processors.		
Unit – IV	**Memory Design:**	**9**
Overview of SOC memory - cache memory - Strategies for Line Replacement at Miss Time-Split I - and D - Caches and the Effect of Code Density - Multilevel Caches - Virtual-to-Real Translation-SOC Memory Systems - Board-based Memory Systems - Simple DRAM and Memory Array - Models of Simple Processor – Memory Interaction		
Unit – V	**Interconnect and customization:**	**9**
Bus: Basic Architecture - SOC Standard Buses - Analytic Bus Models - NOC with Switch Interconnects - Layered Architecture and Network Interface Unit- Customizing Instruction Processors - Reconfigurable Technologies		
		Total:45

REFERENCES:

1.	Michael J Flynn and Wayne Luk, “Computer system Design: System-on-Chip”, Wiley-India, 2012.
2.	Patrick Schaumont, “A Practical Introduction to Hardware/Software Co-design”, 2nd Edition, Springer, 2012
3.	Sudeep Pasricha, NikilDutt, “On Chip Communication Architectures: System on Chip Interconnect”, Illustrated Edition, Morgan Kaufmann Publishers, 2008.

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	comprehend the SOC design approaches	Understanding(K2)
CO2	understand the basic concepts of chip design	Understanding(K2)
CO3	summarize the different processor architectures for SOC	Understanding(K2)
CO4	design the memory for SOC	Applying (K3)
CO5	comprehend the interfacing techniques and customization	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	3		2
CO2	2		3	3		2
CO3	2		3	3		2
CO4	2		3	3		2
CO5	2		3	3		2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	85					100
CAT2	15	85					100
CAT3	15	50	35				100
ESE	10	70	20				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE11 - RECONFIGURABLE ARCHITECTURES FOR VLSI							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To comprehend and apply different reconfigurable architecture in FPGA.	
Unit – I	**Device architecture:**	**9**
General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices– Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.		
Unit – II	**Reconfigurable computing architectures and systems:**	**9**
Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Reconfiguration Management.		
Unit – III	**Programming reconfigurable systems:**	**9**
Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing		
Unit – IV	**Mapping designs to reconfigurable platforms:**	**9**
Technology Mapping – FPGA Placement – Datapath composition -Retiming, Repipelining, and C-slow Retiming – Configuration Bit stream Generation.		
Unit – V	**Application development:**	**9**
Implementing Applications with FPGAs –Pattern Matching- Video Streaming -Adaptive cryptographic systems-Adaptive controller.		
		Total:45

REFERENCES:

1.	Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.
2.	Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005
3.	Christophe Bobda, “Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications”, Springer, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	comprehend the different computing models	Understanding(K2)
CO2	discuss the different reconfigurable computing architecture and systems	Understanding(K2)
CO3	develop program for reconfigurable systems	Applying(K3)
CO4	map the design into different platforms	Understanding(K2)
CO5	apply reconfigurable technique for developing applications	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3	2	2
CO2	3		3	3	2	2
CO3	3		3	3	2	2
CO4	3		3	3	2	2
CO5	3		3	3	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	50	35				100
CAT3	15	50	35				100
ESE	10	55	35				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE12 - HARDWARE SECURITY							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To understand the basics of hardware security, hardware Trojan attacks in IPs and FPGAs, side-channel attacks and hardware Trojan prevention.	
Unit – I	**Introduction to Hardware Trojan and Hardware Trojan attacks:**	**9**
Overview of Hardware Trojans- Trends, Tradeoffs and Threats of Trojans- Comparisons and Misconceptions with Trojan Attacks- Offensive Strategies- Defensive Strategies -Challenges of SoC Security- SoC Threat Model- SoC Security Assurance.		
Unit – II	**Hardware IP Trust and Hardware Trojan in ICs:**	**9**
Trojan Characteristics – Inadequacies of existing testing and security features- Trojan classification – General Trojan Mitigation techniques- Trojan Mitigation at IP Level – Hardware Trojans in RF ICs - Hardware Trojans in Analog-Mixed Signal (AMS) ICs.		
Unit – III	**Side-Channel Attacks:**	**9**
Taxonomy of Side-Channel Attacks – Power Analysis Attacks- Electromagnetic Side-Channel Attacks- Fault Injection Attacks- Timing Attacks		
Unit – IV	**Hardware Trojan Prevention:**	**9**
Obfuscation- Role of Obfuscation in Hardware Trojan Prevention- Chip-Level Obfuscation- FPGA Obfuscation- Board Level Obfuscation- Evaluation Metrics for Hardware Obfuscation – Physical Unclonable Function		
Unit – V	**Hardware Trojan Attacks in FPGA and Protection Approaches:**	**9**
Threat Models and Taxonomy- Trojans in FPGA Fabric- Trojans in FPGA Design- Trojan in Bit stream- Countermeasures against FPGA Trojans.		
		Total:45

REFERENCES:

1.	Swarup Bhunia, and M. Tehranipoor, "The Hardware Trojan War." Springer (2018).
2.	Swarup Bhunia, and Mark Tehranipoor, “Hardware security: a hands-on learning approach”, Morgan Kaufmann, 2018.
3.	RoelMaes, “Physically unclonable functions: Constructions, properties and applications” Springer Science & Business Media, 2013.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	outline the offensive and defensive strategies of hardware Trojan	Understanding (K2)
CO2	classify the Trojan and Mitigation techniques	Understanding (K2)
CO3	understand the various forms of side-channel attacks	Understanding (K2)
CO4	interpret the types of obfuscation techniques and physical unclonable function	Understanding (K2)
CO5	summarize the types of FPGA Trojans	Understanding (K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3		**2**	**2**
CO2	3		3		**2**	**2**
CO3	3		3		**2**	**2**
CO4	3		3		**2**	**2**
CO5	3		3		**2**	**2**

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	85					100
CAT3	15	85					100
ESE	10	90					100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE13 - FUNCTIONAL VERIFICATION USING HDL							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Verilog HDL**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To impart knowledge on System Verilog and demonstrate the design and verification using System Verilog constructs.	
Unit – I	**Basic Object Oriented Programming:**	**9**
Introduction-OOP Terminology-Creating New Objects-Object De-allocation-Using Objects-Static Variables vs. Global Variables-Class Methods-Defining Methods Outside of the Class-Scoping Rules-Using One Class Inside Another-Understanding Dynamic Objects-Copying Objects-Building a Testbench.		
Unit – II	**Randomization:**	**9**
Randomization in SystemVerilog-Constraint Details-Controlling Multiple Constraint Blocks-Valid Constraints-In-line Constraints-The pre-randomize and post-randomize Functions-Common Randomization Problems-Iterative and Array Constraints-Atomic Stimulus Generation vs. Scenario Generation-Random Control		
Unit – III	**Threads and Inter-process Communication:**	**9**
Working with Threads-Disabling Threads-Inter-process Communication-Events-Semaphores-Mailboxes-Building a Testbench with Threads and IPC-Coverage Types-Functional Coverage Strategies-Data Sampling-Cross Coverage-Analyzing Coverage Data.		
Unit – IV	**Advanced Interfaces:**	**9**
Virtual Interfaces with the ATM Router-Connecting to Multiple Design Configurations-Procedural Code in an Interface-Design Blocks-Testbench Blocks-Alternate Tests.		
Unit – V	**Interfacing With C:**	**9**
Passing Simple Values- Connecting to a Simple C Routine- Connecting to C++- Simple Array Sharing- Open arrays- Sharing Composite Types- Pure and Context Imported Methods- Communicating from C to SystemVerilog- Connecting Other Languages.		
		Total:45

REFERENCES:

1.	Chris Spear, “System Verilog for Verification: A Guide to Learning the Test bench Language Features”, 2nd Edition, Springer, 2012.
2.	Stuart Sutherland, Simon Davidman and Peter Flake , SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2nd Edition, , Springer
3.	Donald Thomas, “Logic Design and Verification Using SystemVerilog”, Create Space Independent Publishing Platform, 2014

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	understand the basics of Object Oriented Programming concepts in System Verilog	Understanding(K2)
CO2	demonstrate the constrained random coverage driven verification in SV Environment	Applying(K3)
CO3	construct a complete verification with system verilog test bench	Applying(K3)
CO4	construct a verification platform with advanced interfaces	Applying(K3)
CO5	demonstrate communicating from C language to SystemVerilog	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3	3	3	2
CO2	2		3	3	3	2
CO3	2		3	3	3	2
CO4	3	3	3	3	3	2
CO5	3	3	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	30	60				100
CAT2	10	10	80				100
CAT3	10	10	80				100
ESE	10	20	70				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE14 - VLSI FOR IOT SYSTEMS							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To impart knowledge on design methodologies and architectures for IoT systems on a chip.	
Unit – I	**Introduction:**	**9**
The Internet of Things: Context and Overview- Requirements of IoT Nodes- Physical Constraints- Interaction with the External World - On-Board Capabilities of IoT Nodes- User Constraints -Present and Future Challenges in Chips for IoT Nodes: Energy Efficiency - The Wireless Power Issue and Communication - Computation Tradeoff- Opportunities to Achieve Highly Energy-Efficient Processing - Security Challenges in IoT Nodes.		
Unit – II	**IoT nodes:**	**9**
Architecture of IoT Nodes - Requirements for IoT Nodes – Power – Cost – Interoperability – Security - Wireless Network Threats - Pairing, Registration, and Installation of IoT Nodes - Impact of Security on Power - Global System Power Optimization.		
Unit – III	**Low-Power Digital Architectures for the IOT:**	**9**
Ultra-Low-Power Microcontroller Architectures - Power Management - IO Architecture - Data Processing - Near-Threshold MCU Architectures - From Single Core to Multi Core -Energy Benefits and Challenges for Parallel ULP Processors - Architecture of Memory Subsystem for Parallel ULP Processors.		
Unit – IV	**Design Methodologies for IoT Systems on a Chip:**	**9**
Static Power Reduction - Power Gating- Power Gating and Well-Bias - Clamping and Isolation - State Retention with Power Gating - State Retention with Power Gating Optimizations - Active Power Reduction - Voltage Scaling - Clock Gating - Clock Distribution - Clock Tree Synthesis Methodology.		
Unit – V	**System Packaging and Assembly in IoT Nodes:**	**9**
Packaging Technology - Current Commercial Packaging Technology for Internet of Things - Integration/Assembly of Multiple Chips (or) PCB Level Packaging - Second Level Packaging - Multiple Chip Integration (or) System in Package.		
		Total:45

REFERENCES:

1.	Alloto."EnablingtheInternetofThings-FromIntegratedCircuitstoIntegratedSystems", Springer Publications,1st Edition,2017.
2.	Pieter Harpe, Kofi A. A Makinwa, Andrea Baschirotto, "Hybrid ADCs, Smart Sensors for the loT, and Sub-1V & Advanced NodeAnalogCircuit Design". Springer International Publishing AG,2017

COURSE OUTCOMES: **On completion of the course, the students will be able to**		**BT Mapped (Highest Level)**
CO1	summarize the concepts of IoT	Understanding (K2)
CO2	understand the components of IoT Nodes	Understanding (K2)
CO3	infer the low-power digital architectures for IoT	Understanding (K2)
CO4	develop the design methodologies for IoT systems on a chip	Applying (K3)
CO5	understand the system packaging and assembly in IoT nodes	Understanding (K2)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3		3	2	2	2
CO2	3		3	2	2	2
CO3	3		3	2	2	2
CO4	3		3	2	2	2
CO5	3		3	2	2	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	85					100
CAT2	15	85					100
CAT3	10	45	45				100
ESE	10	70	20				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE15 - VLSI FOR BIOMEDICAL APPLICATIONS							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Low Power VLSI Design**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	To learn the various low power techniques for Biomedical systems						
Unit – I	**Low-Power Analog and Biomedical Circuits:**						**9**
Low power transimpedance amplifiers and photo receptors Low power transconductance amplifiers and scaling laws for power in analog circuits- Low-power filters and resonators- Low power current- mode circuits - Ultra-low-power and neuron-inspired analog-to-digital conversion for biomedical system.							
Unit – II	**Low-Power RF and Energy-Harvesting Circuits for Biomedical Systems:**						**9**
Wireless inductive power links for medical implants - Energy-harvesting RF antenna power links - Low-power RF telemetry in biomedical limplants.							
Unit – III	**Biomedical Electronic Systems:**						**9**
Ultra-low-power implantable medical electronics- cochlear implants or bionic ears-an ultra low power programmable analog bionic ear processor-low power electrode stimulation highly miniature electrode –stimulation –Brain machine interfaces for the blind-Brain machine interface for paralysis, speech, and other disorders. Ultra-low-power noninvasive medical electronics -Analog integrated circuit switched-capacitor model of the heart – the electrocardiogram- A micro power electrocardiogram amplifier -Low-power pulse oximetry.							
Unit – IV	**Principles for Ultra-Low-Power Analog and Digital Design:**						**9**
Digital design- Sizing and topologies for robust sub threshold operation-Types of power dissipation-energy efficiency-Optimization of energy efficiency-Varying the power-supply voltage and threshold voltage- Analog and mixed-signal design -Power consumption in analog and digital systems-low power hand- The optimum point for digitization in mixed-signal system Common themes in low-power analog and digital design-The Shannon limit for energy efficiency.							
Unit – V	**Bio-Inspired Systems:**						**9**
Neuromorphic electronics- Transmission-line theory- The cochlea: biology, motivations, theory, and RF-cochlea design- Cytomorphic electronics: cell-inspired electronics for systems and synthetic biology- Electronic analogies of chemical reactions- Log-domain current-mode models of chemical reactions and protein-protein networks- Analog circuit models of gene-protein dynamics- Logic-like operations in gene-protein circuits- Circuits-and-feedback techniques for systems and synthetic biology Hybrid analog-digital computation in cells and neurons.							
							Total:45

REFERENCES:

1. Rahul Sarpeshkar, “Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems” 1st Edition, Cambridge University Press, 2011.
2. Kris Iniewski, “VLSI Circuit Design for Biomedical Applications”, 1stEdition, Artech House Publishers, 2008.
3. Khandpur RS, “Handbook of Biomedical Instrumentation”, McGraw Hill, New Delhi, 2014.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	acquire the concepts of low power amplifier circuits	Understanding(K2)
CO2	comprehend RF CMOS circuits for Biomedical applications	Understanding(K2)
CO3	correlate the analogy of biological components with low power circuits	Understanding(K2)
CO4	design analog and mixed signal biomedical circuits	Applying(K3)
CO5	interpret various bioinspired systems	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2	2	2	3
CO2	3	3	2	2	2	3
CO3			3	3	3	
CO4			2	3	2	
CO5	3	3	2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	85					100
CAT3	10	45	45				100
ESE	10	70	20				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE16 - NETWORK ON CHIP							
Programme & Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To understand the different network architectures and concepts of Network On Chip	
Unit – I	**Uses of Interconnection Networks:**	**9**
Processor-Memory Interconnect - I/O Interconnect - Packet Switching Fabric - Network Basics -Topology-Routing - Flow Control - Router Architecture - Performance of Interconnection - Case study with a simple interconnection network.		
Unit – II	**Topology Basics:**	**9**
Channels and Nodes-Direct and Indirect Networks-Cuts and Bisections- Paths-Symmetry - Traffic Patterns - Performance - Throughput and Maximum Channel Load - Latency - Path Diversity - Case Study: Butterfly networks.		
Unit – III	**Non-Blocking Networks:**	**9**
Non-Blocking vs. Non-Interfering Networks - Crossbar Networks –Close Networks - Beneˇs Networks - Sorting Networks. **Slicing and Dicing:** Concentrators and Distributors - Bit Slicing - Dimension Slicing - Channel Slicing - Slicing Multistage Networks.		
Unit – IV	**Routing Basics:**	**9**
A Routing Example - Taxonomy of Routing Algorithms - The Routing Relation -Deterministic Routing - Oblivious Routing - Adaptive Routing**.**		
Unit – V	**Flow Control Basics:**	**9**
Flow Control Basics: Resources and Allocation Units - Buffer less Flow Control - Circuit Switching -Buffered Flow Control. **Deadlock and Livelock:** Deadlock - Deadlock Avoidance - Adaptive Routing - Deadlock Recovery.		
		Total:45

REFERENCES:

1.	William James Dally and Brian Towles, “Principles and Practices of Interconnection Networks”, 1st Edition, Morgan Kaufmann Publishers, 2004.
2.	Santanu Kundu and Santanu Chattopadhyay, “Network-on-Chip: The Next Generation of System on-Chip Integration”, CRC Press, 2014.
3.	Giovanni De Micheli and Luca Benini, “Networks on Chips: Technology and Tools”, 1st Edition, Academic Press, 2006.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	summarize the interconnection networks	Understanding K2)
CO2	comprehend the basics of network topology	Understanding K2)
CO3	classify the different types of networks	Understanding(K2)
CO4	develop routing algorithms	Applying (K3)
CO5	explain the basics of flow control, deadlock and livelock	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	2	2	3
CO2	3		2	2	2	3
CO3	3		2	2	2	3
CO4	3		3	3	3	3
CO5	3		2	2	2	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85					100
CAT2	15	85					100
CAT3	10	45	45				100
ESE	10	70	20				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE17- SUPERVISED MACHINE LEARNING ALGORITHMS (Common to VLSI Design and Embedded Systems branches)							
Programme& Branch	**ME - VLSI DESIGN & ME - EMBEDDED SYSTEMS**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	To focus on supervised machine learning algorithms and to create simple, interpretable models to solve classification and regression problem						
Unit – I	**Discriminative Algorithms :**						**9**
Cost function –LMS Algorithm – The normal Equations-Probability interpretation-locally weighted linear regression-logistic regression-generalized linear models-Application to prediction.							
Unit – II	**Generative Algorithms :**						**9**
Generative Models: Gaussian Discriminant Analysis (GDA)-Naïve Bayes- Laplace smoothing-Marginal classifier: Support Vector Machine (SVM) as optimal Margin classifier-Application to Classification.							
Unit – III	**Multilayer Perceptrons:**						**9**
Multilayer Perceptrons-Implementation of Multilayer Perceptrons-Forward Propagation, Backward Propagation and computer Graphs-Numerical stability and Initialization-Generalization in Deep Learning-Dropout-Case study :House Price Prediction.							
Unit – IV	**Convolutional Neural Networks (CNN) :**						**9**
From fully Connected Layers to Convolutions –Convolution for Images-Padding and Stride-Multiple input and multiple output channel-Pooling-Case study: LeNet, Alexnet, VGGnet.							
Unit – V	**Recurrent Neural Network(RNN):**						**9**
Working with sequences-Converting Raw Text into Sequence Data-Language model-Recurrent Neural Network-Back Propagation through time-Case study: GRU,LSTM.							
							Total:45

REFERENCES:

1.	Christopher M. Bishop, “Pattern Recognition and Machine Learning”, Springer-Verlag New York. reprint 2010
2.	Aston Zhang, Zachary C. Lipton, Mu Li, and Alexander J. Smola,”Dive into Deep learning”, ebook Published September 18, 2020 https://d2l.ai/index.html
3.	UCI Machine Learning repository: http://archive.ics.uci.edu/ml/index.php

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	understand discriminative algorithms for classification and regression problems	Understanding(K2)
CO2	validate a generative model based algorithm for classification and regression problems	Applying (K3)
CO3	understand the designed ANN for a real time application using BPN	Understanding(K2)
CO4	develop a CNN model for image analysis	Applying(K3)
CO5	develop a RNN model for various types of sequence	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				3	3
CO2	3		3		3	3
CO3	3		3		3	3
CO4	3		3		3	3
CO5	3		3		3	3

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	65	20				100
CAT2	15	65	20				100
CAT3	10	20	70				100
ESE	5	45	50				100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22VLE18 - GENETIC ALGORITHMS AND ITS APPLICATIONS							
Programme& Branch	**ME & VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**ASIC Design**	**3**	**PE**	**3**	**0**	**0**	**3**

Preamble	To perform VLSI design optimization, layout generation and chip testing using genetic algorithm for developing efficient computer aided design tools	
Unit – I	**Introduction:**	**9**
GA Terminology-The Simple GA-The Steady-State Algorithm-Genetic Operators- GA for VLSI Design, Layout and Test automation		
Unit – II	**Partitioning:**	**9**
Problem Description-Circuit Partitioning by Genetic Algorithm-Hybrid Genetic Algorithm for Ratio-Cut Partitioning.		
Unit – III	**Standard Cell and Macro Cell Placement & Routing:**	**9**
Standard cell placement-GASP algorithm-Macro Cell Placement-unified algorithm-The Steiner Problem in a Graph-Macro Cell Global Routing.		
Unit – IV	**FPGA Technology Mapping and Automatic Test Generation**:	**9**
Circuit Segmentation and FPGA Mapping-Circuit Segmentation for Pseudo-Exhaustive Testing-Test generation in a GA frame work-Deterministic/Genetic Test Generator Hybrids.		
Unit – V	**Power Estimation**:	**9**
Application of GA to Peak power estimation –Estimation of Peak Single-Cycle and n-Cycle Powers-Peak Sustainable Power Estimation –Parallel Genetic Algorithms for Automatic Test Generation -problem encoding- fitness function-GA vs Conventional algorithm.		
		Total:45

REFERENCES:

1.	PinakiMazumder,E.MRudnick,"Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall,2014.
2.	Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley 2nd edition, 2004.
3.	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	comprehend the concepts of genetic algorithm and physical design of VLSI systems	Understanding(K2)
CO2	Interpret genetic algorithm for partitioning of VLSI systems	Understanding(K2)
CO3	outline the concepts of genetic algorithm for placement and routing	Understanding(K2)
CO4	infer the basics of automatic test pattern generation and FPGA mapping in VLSI systems	Understanding(K2)
CO5	understand the power estimation in VLSI Layout using Genetic Algorithm	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				2	2
CO2	3		3		3	2
CO3	3		3		3	2
CO4	3		3		3	2
CO5	3		3		3	2

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	85	-	-	-	-	100
CAT2	15	85	-	-	-	-	100
CAT3	15	85	-	-	-	-	100
ESE	10	90	-	-	-	-	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

22GET13 - INNOVATION, ENTREPRENEURSHIP AND VENTURE DEVELOPMENT							
(Common to ME/MTech and MCA Programmes)							
Programme & Branch	**All ME/MTech and MCA Programmes**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**3**	**PE**	**3**	**0**	**0**	**3**
Preamble	This course will direct the students on how to employ their innovations towards a successful entrepreneurial venture development.						
Unit – I	**Innovation and Entrepreneurship:**						**9**
Creativity and Innovation – Types of innovation – challenges in innovation- steps in innovation management- Meaning and concept of entrepreneurship - Role of Entrepreneurship in Economic Development - Factors affecting Entrepreneurship – Entrepreneurship vs Intrapreneurship.							
Unit – II	**Design Thinking and Product Design:**						**9**
Design Thinking and Entrepreneurship – Design Thinking Stages: Empathize – Define – Ideate – Prototype – Test. Design thinking tools: Analogies – Brainstorming – Mind mapping. Techniques and tools for concept generation, concept evaluation – Product architecture –Minimum Viable Product (MVP)- Product prototyping – tools and techniques– overview of processes and materials – evaluation tools and techniques for user-product interaction.							
Unit – III	**Business Model Canvas (BMC) and Business Plan Preparation:**						**9**
Lean Canvas and BMC - difference and building blocks- BMC: Patterns – Design – Strategy – Process–Business model failures: Reasons and remedies. Objectives of a Business Plan - Business Planning Process and Preparation.							
Unit – IV	**IPR and Commercialization:**						**9**
Need for Intellectual Property- Basic concepts - Different Types of IPs: Copy Rights, Trademarks, Patents, Geographical Indications, Trade Secrets and Industrial Design– Patent Licensing - Technology Commercialization – Innovation Marketing.							
Unit – V	**Venture Planning and Means of Finance:**						**9**
Startup Stages - Forms of Business Ownership - Sources of Finance – Idea Grant – Seed Fund – Angel & Venture Fund – Institutional Support to Entrepreneurs – Bank and Institutional Finance to Entrepreneurs.							
							Total:45

REFERENCES:

1.	Gordon E. & Natarajan K., "Entrepreneurship Development", 6th Edition, Himalaya Publishing House, Mumbai, 2017.
2.	Sangeeta Sharma, "Entrepreneurship Development", 1st Edition, PHI Learning Pvt. Ltd., New Delhi, 2017.
3.	Charantimath Poornima M., "Entrepreneurship Development and Small Business Enterprises", 3rd Edition, Pearson Education, Noida, 2018.
4.	Robert D. Hisrich, Michael P. Peters & Dean A. Shepherd, "Entrepreneurship", 10th Edition, McGraw Hill, Noida, 2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		BT Mapped (Highest Level)
CO1	understand the relationship between innovation and entrepreneurship	Understanding (K2)
CO2	understand and employ design thinking process during product design and development	Analyzing (K4)
CO3	develop suitable business models as per the requirement of the customers	Analyzing (K4)
CO4	practice the procedures for protection of their ideas IPR	Applying (K3)
CO5	understand and plan for suitable type of venture and modes of finances	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1				3	2	1	3	2		1	1	
CO2	1	2			3	2	1						1	
CO3	3	1	3			1							1	
CO4	1	2				3							1	
CO5	1	2				3							1	

1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy

ASSESSMENT PATTERN – THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	40	40	20				100
CAT2	30	40	30				100
CAT3	30	40	30				100
ESE	30	40	30				100

* ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)