Single Stage Static Level Shifter Design for Subthreshold to I/O Voltage Conversion

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ABSTRACT

A static subthreshold to I/O voltage level shifter is proposed. The proposed circuit employs a diode-connected pull-up transistor stack and a feedback structure to alleviate the drive strength requirement on the pull-down transistors. The proposed level shifter achieves less than 6 FO4 inverter delay under process and temperature variation when converting the input from 300mV to 2.5V. Compared to a conventional DCVS design, the new design consumes 8 times less power and is 10% faster under room temperature.

Categories and Subject Descriptors

B.6.1 [**Design Styles**]: Combinational logic

General Terms Design

Keywords subthreshold, level shifter

1. INTRODUCTION

Operating in the subthreshold region helps to greatly reduce power dissipation for applications that do not require high performance [2, 6]. Level conversion has always been an issue for systems that need to deal with two or more power domains. This problem is more severe in subthreshold circuits. Since the drive strength of the input devices are mostly limited to subthreshold operation and have a corresponding exponential dependency on voltage, several intermediate voltages are typically required to up-convert to I/O voltage levels. Generating intermediate voltages and the extra wiring requirements are undesirable side effects of multi-stage level conversion. In this paper we discuss the design issues associated with bridging the subthreshold core logic and I/O voltage in a single stage design, and propose a robust circuit that addresses these issues.

Differential cascode voltage switch (DCVS) is a commonly used circuit technique for voltage level conversion [5]. It has the advantage of low static power consumption and small propagation delay due to the cross-coupled latch structure. The drawback is that converting from ultra-low input voltages requires large transistors, which will be discussed in Section 2. Modified DCVS was proposed to alleviate the contention problem [8], however it still suffers the same sizing issue as the DCVS level shifter when the input is at subthreshold voltage. A dynamic level converter is a reliable way to achieve level conversion at low voltages [3, 1]. The disadvantage is that it is more power hungry compared to its static counterpart and requires extra clock routing and synchronization circuitry. Since power consumption is the critical performance metric in subthreshold systems, dynamic level conversion becomes undesirable. Single supply diode-voltage-limited buffer and half-latch level converters are other options used for dual supply systems [4]. While not specifically designed for subthreshold level conversion, these designs generally require the cascading of multiple stages.

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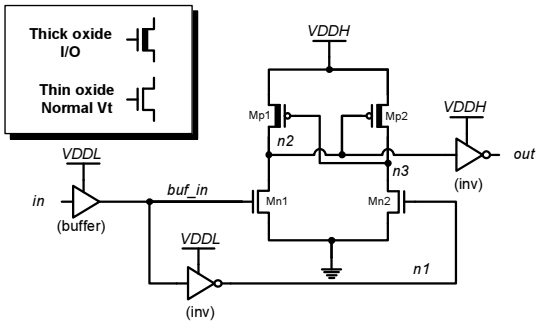

Figure 1: Conventional DCVS-type level shifter with cross-coupled pull-up transistors.

In this paper, we will first examine the sizing of conventional DCVS level shifters at very low voltages and demonstrate its susceptibility to process and temperature variations. We will then present a modified diode-voltage-limited level shifter that takes the advantage of the input level independent pull-up devices. We compare the proposed circuit to the conventional approach in terms of power consumption, area, and delay.

2. CONVENTIONAL APPROACH

Fig. 1 shows the circuit diagram of a DCVS-type level shifter. The circuit operates on the basis of contention between pull-up and pull-down devices. In order for the output to switch, the NMOS drive strength has to be sufficiently greater than the PMOS drive strength. When VDDL is at a subthreshold level and VDDH is the I/O voltage, the difference in drive strength for the pull-up and pull-down transistors can easily be greater than three orders of magnitude.

Fig. 2 shows the simulated gate delay of the DCVS level shifter converting a periodic input to the I/O voltage in 0.13μm CMOS. Transistors Mp1 and Mp2 are both sized at W/L of 5μm/0.36μm [1] to provide decent fall delay with respect to the rise delay while restricting the size of the pull-down transistors Mn1 and Mn2. When VDDL is 0.35V, the operating frequency is primarily limited by the fall delay if the width of Mn1 and Mn2 (represented by Wn) is greater

[1] 0.36μm is the minimum length of I/O device in this technology

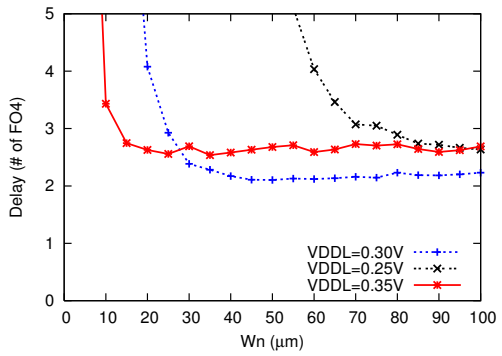

Figure 2: Simulation results showing the operating frequency with respect to pull-down transistor width Wn.

than 15μm. This also indicates that the results can be further optimized by up-sizing Mp1 and Mp2. However, at lower VDDL, the rise delay is not able to catch up with the fall delay until Mn1 and Mn2 is disproportionately large. Other than the area and corresponding leakage power arising from such large pull-down transistor sizes, operating at low temperatures leads to another problem for this type of circuit. The drive strength of Mp1/Mp2 are (at most) quadratically sensitive to Vt shift while the drain current of Mn1/Mn2 has an exponential dependency on Vt. As a result it is much more difficult to balance drive strengths at lower temperature by sizing up Wn. In typical cases, conventional level shifter is able to achieve less than 5 fanout-of-four inverter (FO4) delays at VDDL, which is sufficiently fast for most subthreshold applications. However, considering 3σ process variation, Wn needs to be up-sized at least two times larger than the nominal case to maintain functionality.

3. PROPOSED APPROACH

To overcome the dramatic difference in overdrive voltage for pull-up and pull-down transistors, diode-connected PMOS transistors are used to replace the pull-up transistors. The proposed circuit is shown in Fig. 3. The pull-down of internal nodes *intn* and *intp* is directly through normal Vt transistor Mn1 and zero Vt thick oxide transistor Mn2. The use of Mn2 was previously proposed to reduce the potential difference across the drain and source of Mn1 [7]. Therefore, the drive strength of Mn1 can be increased by avoiding the use of thick oxide devices. We apply this stack transistor technique to the conventional level shifter for fair comparisons in the results section. The purpose of Mp1 is to help eliminate part of the cross-bar current at the beginning of the transition, although it also introduces roughly 10% delay penalty due to the extra loading.

For pulling up the internal nodes, Md1 through MdN transistor stacks provide a variable resistance path to the supply. At the beginning of input switching, most of the VDDH voltage drop is across Md1-MdN. Assuming that each transistor in the stack is still biased above threshold voltage and neglecting second order effects, the effective resistance of the stack can be represented by

$$R_{eff} = \frac{V_{VDDH} \cdot L_p}{\mu \cdot C_{ox} \cdot W_p(\frac{V_{VDDH}}{\mathrm{N}} - V_t)^2} \qquad (1)$$

where N is the number of devices in the stack. A small N helps to achieve faster falling delay by initially providing a

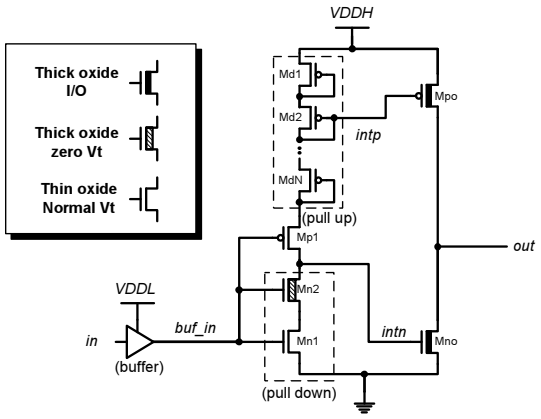

Figure 3: Proposed approach that uses input voltage independent diode-connected transistor stacks for pull-up devices.

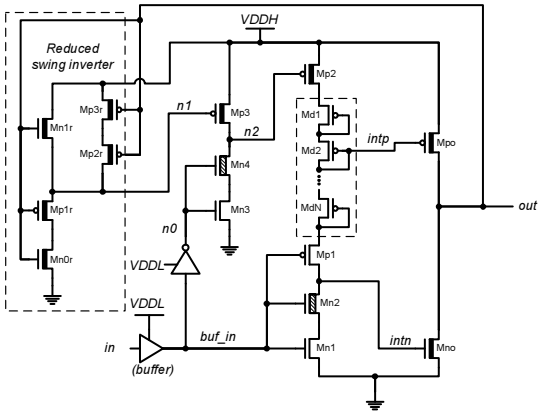

Figure 4: Proposed level shifter with feedback path for leakage reduction.

smaller R_{eff} and reducing the time it stays in subthreshold region before the state is switched. However, a smaller N also leads to larger leakage when the input is at state 1. Nodes *intn* and *intp* are used to drive output transistors Mno and Mpo, respectively. In this way, the 'good 0' property of *intn* and 'good 1' property of *intp* can both be used to reduce static power with little impact on the ON current of the output stage.

The circuit in Fig. 4 is proposed to solve the leakage problem introduced in the previous paragraph. The idea is to add a PMOS header Mp2 on top of the pull-up transistor stack. When both the input and the output is high, $n0$ is low and $n1$ is designed at 500mV below VDDH due to the reduced swing inverter. As a consequence, $n2$ will be pulled high, strongly turning off Mp2 to save leakage. When the input switches low, Mn3 needs to be strong enough with a gate voltage of VDDL to pull down $n2$. Otherwise, the pull-up transistor stack will not be able to charge *intn* and *intp*, causing functional failure. Assuming that node $n2$ can be pulled down very quickly after *in* goes low, the rise delay is dictated by the size of transistors Md1 through MdN. In this way, we can choose circuit parameters (including the number of transistors in the stack N, and transistor widths) to match the fall delay with the rise delay without sacrificing leakage power or vice versa.

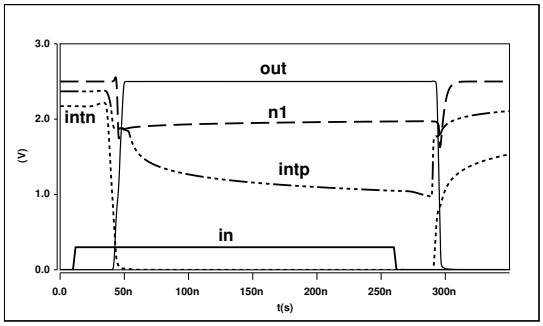

Figure 5: Waveforms demonstrating the operation of our proposed circuit.

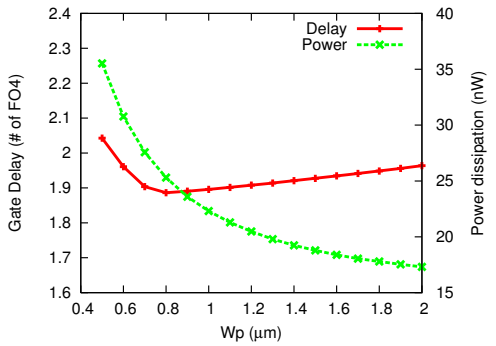

Figure 6: Sizing of diode-connected stacked PMOS (Wp) versus gate delay and power dissipation.

The use of the reduced swing inverter helps to match the gate overdrive voltage to the subthreshold voltage input that is being converted. All devices are thick oxide I/O devices in this circuit. When *out* is low, Mp2r and Mp3r can easily pull $n1$ to VDDH. When *out* goes high, it behaves like a reduced swing driver, which is used to save switching energy for interconnect [9]. Instead of pulling all the way to 0, $n1$ will remain slightly higher than (VDDH-Vtn) in this situation. The inverted output is designed at 2V for 0.3V to 2.5V voltage conversion. It provides a fast response time for leakage reduction and still makes Mp3 weak enough compared to Mn3 when there is logic contention at $n2$.

The simulated waveforms of our proposed circuit are shown in Fig. 5 where N is 5. As *in* transitions from high to low, $n1$ is pulled up to VDDH to ensure the diode transistors stack is able to sink current from VDDH. Therefore, both *intp* and *intn* rise to within 10% of their corresponding steady state voltage in a few hundred ns (FO4 delay at 0.3V in this technology is 18ns). Node *intp* has to be able to quickly turn on the output pull-up transistor Mpo. In this design, the internal node between Md2 and Md3 is chosen as *intp*. The tradeoff in the selection of this node is the leakage power since *intp* will never reach VDDH. When *in* goes high again, $n1$ drops from VDDH to turn off Mp2 in order to save leakage power in this state. Nodes *intp* and *intn* decrease as well, allowing *out* to go high.

The guidelines for transistor sizing in the proposed level shifter can be summarized as follows:

- Use minimal transistor dimensions for Mp1 to minimize the intrinsic loading on node *intn*.
- Determine the size of Mp2 based on leakage current constraints when the input is at state 1.
- Size Mn1 to meet the target leakage current at state 0 and the rise delay requirements.
- Choose N (the number of stacked PMOS devices) by calculating the fall delay based on supply voltage and Vt of each transistor.
- Verify that the pull-down strength of Mn3 is always stronger than the pull-up strength of Mp3 at process corners.

Among these steps, the sizing of transistors Md1 through MdN is the most difficult to determine analytically since the operating range is mostly between the subthreshold and superthreshold regions. For a better understanding of the tradeoffs, transistor size Wp versus gate delay and power dissipation is simulated and shown in Fig. 6. By taking the maximum of the rise and fall delays, gate delay represents the maximum operating frequency of the level shifter. N is chosen to be 5 and the width of transistor Mn1 is 5μm. When Wp is small, gate delay is dominated by the fall delay. Increasing Wp both decreases the fall delay by reducing the effective pull-up resistance and increases the rise delay as the parasitic capacitance also grows. To illustrate a typical case for subthreshold operation at 300mV, the circuit is running at 100 FO4 delay with an activity factor of 0.1. The cross-bar current dominates other leakage sources in this scenario. Therefore, as Wp increases the power consumption decreases due to the faster rising transition of internal nodes *indp* and *indn*, despite the fact that parasitic capacitances also rise. As expected, power dissipation saturates to a certain value as Wp becomes large and finally will start rising as parasitic capacitances dominate.

4. SIMULATION RESULTS

In this section, we compare the performance of the proposed level shifter to the conventional design in terms of delay, power, robustness, and area. The target output voltage VDDH is 2.5V, which is being converted to from a subthreshold voltage of 300mV. The simulations are conducted using commercial 0.13μm CMOS logic technology. Power values do not include the switching power that drives a physical package pin. As was explained in Section 2, the W/L of pull-up transistors are 5μm/0.36μm for the conventional level shifter.

We first examine the gate delay and power dissipation of both circuits at different temperatures. Worst-case corner (fast PMOS and slow NMOS) is applied for all transistors. In Fig. 7a, gate delay is plotted with respect to temperature. Both circuits can operate sufficiently fast (roughly 5 FO4 delays) above room temperature. However, the conventional circuit runs much slower at low temperatures and even fails to function completely below -10°C. This is due to the pull-down NMOS devices becoming exponentially weaker at low temperature while PMOS become stronger due to their mobility increase (as they are not operating in subthreshold). On the other hand, the gate delay of our proposed circuit remains almost constant in terms of FO4 delays across temperature. The power dissipation of the level converters are calculated with a period of 5000 FO4 inverter delays. Fig. 7b clearly shows that the proposed circuit has lower power than the conventional design. The first reason is due to the fact that the conventional circuit is slower, making it more susceptible to cross-bar current. In addition, large NMOS sizes are required in the DCVS case due to the difficulty in low temperature conversion and result in large parasitic ca-

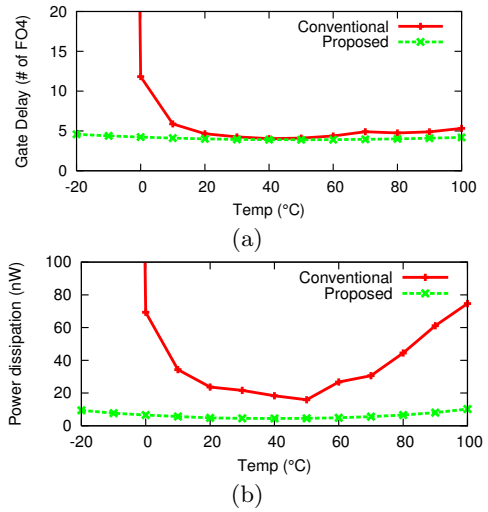

Figure 7: Comparison of level shifters. (a) Gate delay, (b) Power consumption.

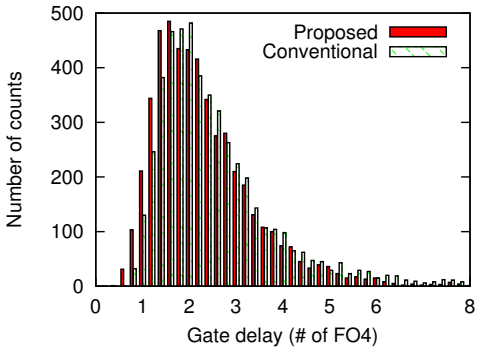

Figure 8: Monte Carlo simulation results showing gate delay variation across process spread.

pacitances. This increases both switching and leakage power components.

Process variation is an important characteristic for sub-threshold circuits. We perform 5000 Monte Carlo SPICE simulations on both level shifters and show the variation in gate delay when converting from 0.3V to 2.5V (Fig. 8). Process related parameters such as Vt and geometry are the sweeping factors in this setup. Both level shifters are configured the same way as the experiment in the previous paragraph. The μ and σ of conventional level shifter are 3.1 and 2.77 in terms of FO4 inverter delay. On the other hand, the μ and σ of our proposed level shifter are 2.63 and 1.13 FO4 delays, respectively. Although the proposed level shifter is smaller in total area and has a more complicated circuit structure, it is still less affected by process variations. The reason is that our proposed circuits with the diode-connected pull-up stack has less contention at the beginning of state switching compared to the conventional one. In other words, speed penalty caused by contention has less impact on our circuits when process parameters vary.

Table 1 summarizes the circuit parameters of the conventional and proposed level shifters at worst-case process corner and room temperature. These values do not include the input buffer to the level shifters to simplify the comparison. Therefore, the power consumption of the conventional

Table 1: Comparison of level shifters.

	Conventional	Proposed
Active energy (fJ)	828	102
Leakage power (pW)	1080	121
Rise delay (# of FO4)	4.74	4.16
Fall delay (# of FO4)	4.64	3.79
Total transistor area (μm^2)	30.58	11.11

one is underestimated due to its larger input capacitances. The conventional level shifter suffers from area (calculated as the sum of transistor areas) and power penalties in order to increase the driving strength of pull-down transistors especially at low temperatures. The routing cost and irregular structure of the proposed circuit will reduce the area difference in physical design, however, it still has a clear edge in this category.

5. CONCLUSION

In this work, we proposed a subthreshold to I/O voltage level shifter that relies on a pull-up transistor stack independent of the input voltage. Through a feedback mechanism that reduces leakage when the input is high, it also improves the transition speed of the circuit. The proposed level shifter was compared to the conventional DCVS-type level shifter, and shows advantages in power dissipation, gate delay and total area. The proposed level shifter is also capable of converting a 0.3V incoming signal to 2.5V output robustly across process variation according to Monte Carlo SPICE simulations.

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