

Low Power System Design

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Course Introduction

- Master-level course that covers low-power system design
- Schedule
 - Monday, 11:30 to 13:45 (with a few exceptions)
- Instructor
 - Dr. Sangyoung Park + Guest lectures
 - sangyoung.park@tum.de
 - Phone: 23565
 - Office: Room 3993
 - Office hours: Monday, 13:45 to 15:00, but feel free to reach me any time

- Homepage
 - Teaching page in RCS website
 - <http://www.rcs.ei.tum.de/en/courses/lectures/lpsd/>
- Information
 - 5 ECTS
 - All teaching, exams, presentation will be done in English
 - Final exam (50%)
 - Student presentation (30%)
 - Term paper (20%)

Course Introduction

- Textbook
 - There is no single textbook for this course
- References
 - Proceedings of relevant ACM/IEEE conferences
- Course materials
 - PDF format slides will be uploaded one by one

- Dr. Sangyoung Park
 - PhD from Seoul National University, Korea
 - Postdoc @ TUM/RCS (Advisor: Prof. Samarjit Chakraborty)
 - Has been writing & reviewing papers in low-power area since 2009
 - Research areas
 - System-level low-power techniques
 - Energy management for mobile, grid-connected systems, electric vehicles, renewable sources
 - Embedded systems design

What to cover

- Review on prerequisite courses
 - MOSFET model
 - MOS capacitances
 - CMOS circuits
- Source of power consumption
 - Dynamic power of CMOS gates
 - Static power of CMOS gates
 - Power and energy consumption

What to cover

- Power estimation
 - Circuit-level estimation
 - Architecture-level estimation
 - System-level estimation
 - Architecture level simulators
 - Power measurement techniques
- Circuit-level low-power techniques
 - Transistor sizing, path balancing, don't care optimization, technology mapping, state encoding
 - Body-biasing, multiple V_t , input vector control

What to cover

- Architecture-level low-power design
 - Low-power bus interconnect
 - Low-power memory architecture, cache
- System-level low-power techniques
 - Dynamic power management
 - Dynamic voltage and frequency scaling
 - Multicore processor power management
- Power generation and conversion for embedded systems
 - Battery characteristics
 - Power distribution network (DC-DC converters, etc.)
- Real-time systems and low-power
 - Wireless sensor networks
 - Power Management for Mobile Gaming

Why Low Power?

- Why do we want to decrease power consumption?
 - Longer battery life
 - Smaller battery size for portable devices
 - Lower power consumption decreases working temperature of the device
 - Lower electric bills (e.g. operating cost of data centers)

Why Low Power?

- Higher performance and longer battery life are conflicting demands in system design
 - Sophisticated design techniques are needed to meet both of them
- Power management is one of the most critical design issues
 - Power consumption has become the limiting factor
 - Thermal design power requirement
 - Meet the demands of the market
 - Keep the working temperature at an acceptable level

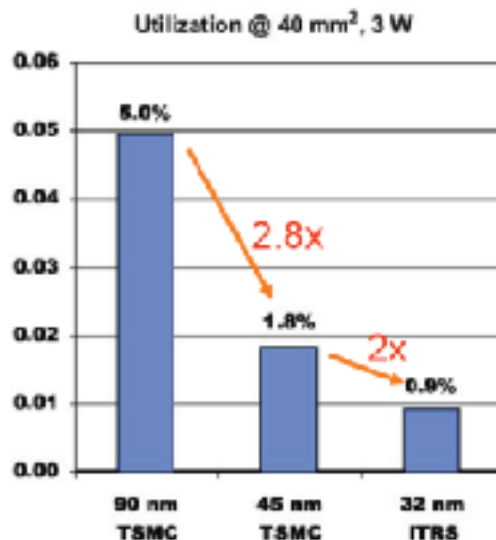
Why Low Power?

- Thermal issues
- Energy issues
- Power issues



Why Low Power?

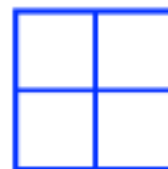
- Power consumption has been the bottleneck over the last decade
- Thermal design power (TDP)
 - Maximum amount of heat generated by the CPU
- Dark silicon era
 - Parts of a chip should be turned off due to TDP



Spectrum of tradeoffs between # of cores and frequency

Example:
65 nm → 32 nm ($S = 2$)

4 cores @ 1.8 GHz



65 nm



2x4 cores @ 1.8 GHz
(8 cores dark, 8 dim)
(Industry's Choice)



4 cores @ 2x1.8 GHz
(12 cores dark)

75% dark after 2 generations;
93% dark after 4 generations

32 nm

Source: Borkar, De Intel

Why Low Power?

- Designing within limits: power & energy
 - Thermal limits (for most parts self-heating is a substantial thermal issue)
 - Package cost (4-5W limit for cheap plastic package, 100W/cm² air cooled limit, 7.5kW 19" rack)
 - Device reliability (junction temp > 125°C substantial reduction in reliability)
 - Performance (25°C to 105°C: loss of 30% of performance)
- Distribution limits
 - Substantial portion of wiring resource, area for power distribution
 - Higher current - lower R, greater dI/dt needs more wire, decoupling capacitors
 - Package capable of low impedance distribution

Why Low Power?

- Energy capacity limits
 - Limits on volume and weight of batteries (portable applications)
 - Energy for IT equipment significant fraction of total cost of ownership

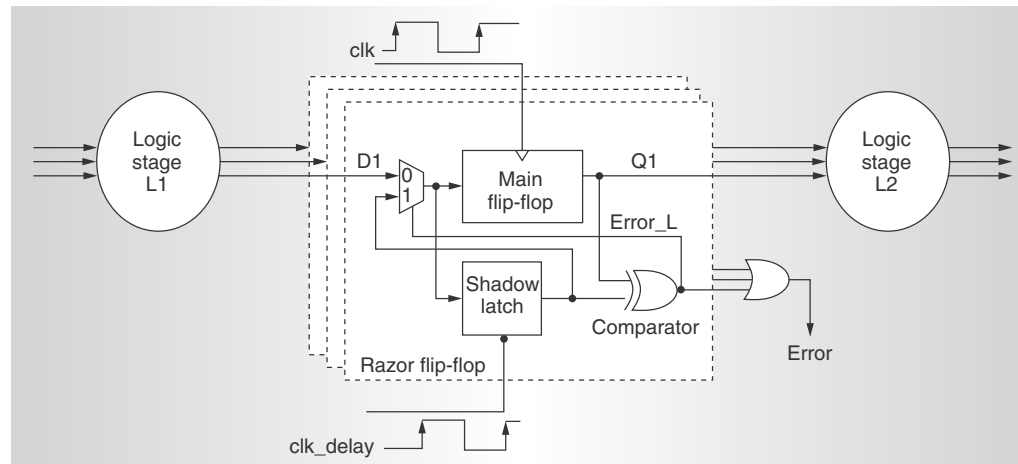
Why Low Power?

- Wearable devices
 - Limited size/weight
 - Energy harvesting
 - Use times



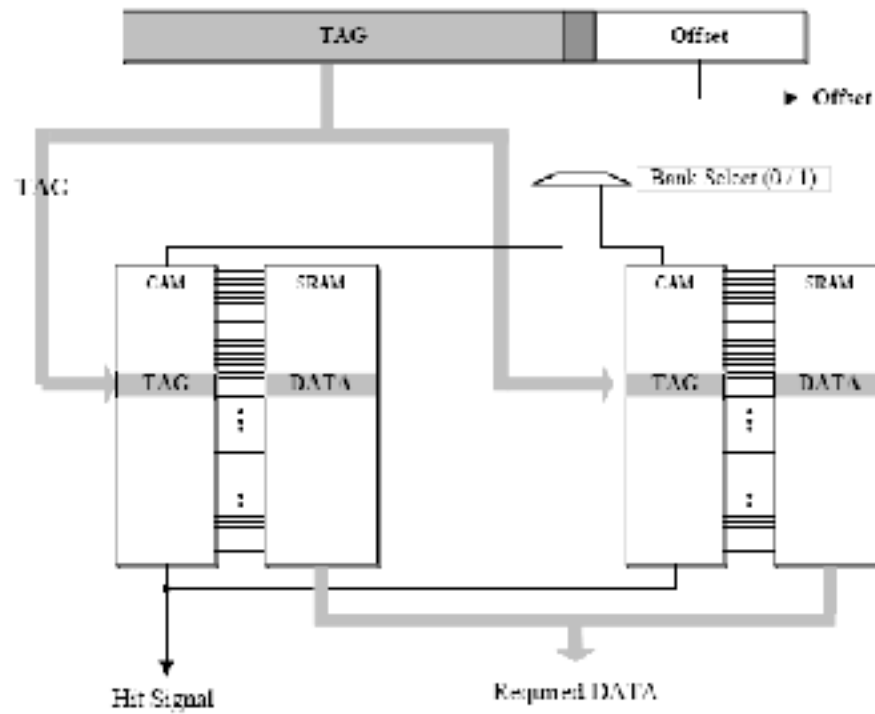
source: <http://www.chinabbb.com/ckfinder/userfiles/images/devices.jpg>

- Low-Power Design @ various abstraction layers
- Circuit-level
 - Low-power techniques applicable at circuit-level
 - Clock-gating, body-biasing, etc.



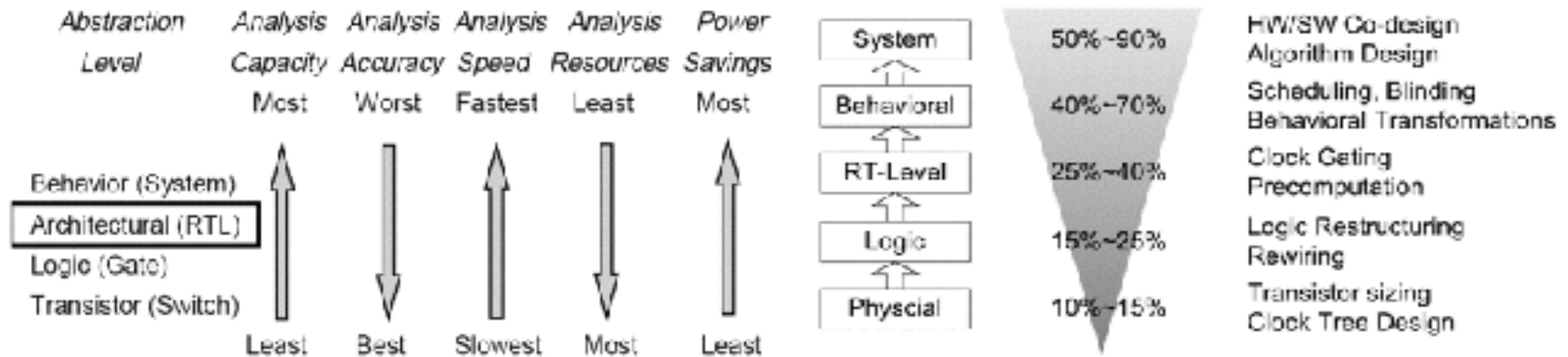
D. Ernst, et al., "RAZOR: CIRCUIT-LEVEL CORRECTION OF TIMING ERRORS FOR LOW-POWER OPERATION", IEEE Micro 04

- Architecture-level
 - Cache/memory architecture
 - Interconnects



System-level energy optimization

- High-level energy reduction
 - RTL or higher level
 - Suitable for complex systems
 - Higher energy gain
 - Based on high-level energy model.
 - High-level energy characterization.
 - Abstraction progressively degrades the quality of power estimation



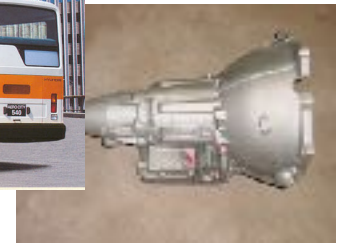
System-level energy optimization

- Low-level energy optimization
 - Has been contributing over dozens of years
 - Enhancement of devices and components
 - General solution applicable to almost all kinds of use
 - City bus service example
 - Objective: more gas mileage
 - New buses, engine swap, aluminum bodies, new transmissions, etc.
 - In the semiconductor world
 - NMOS
 - CMOS
 - MTCMOS

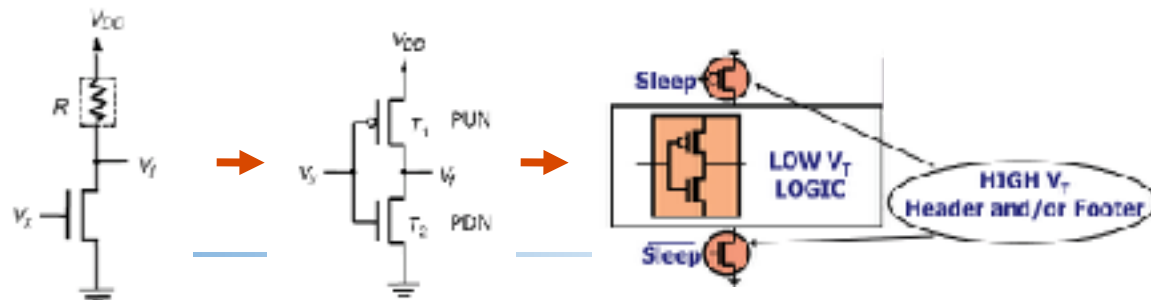
Gas-efficient engine



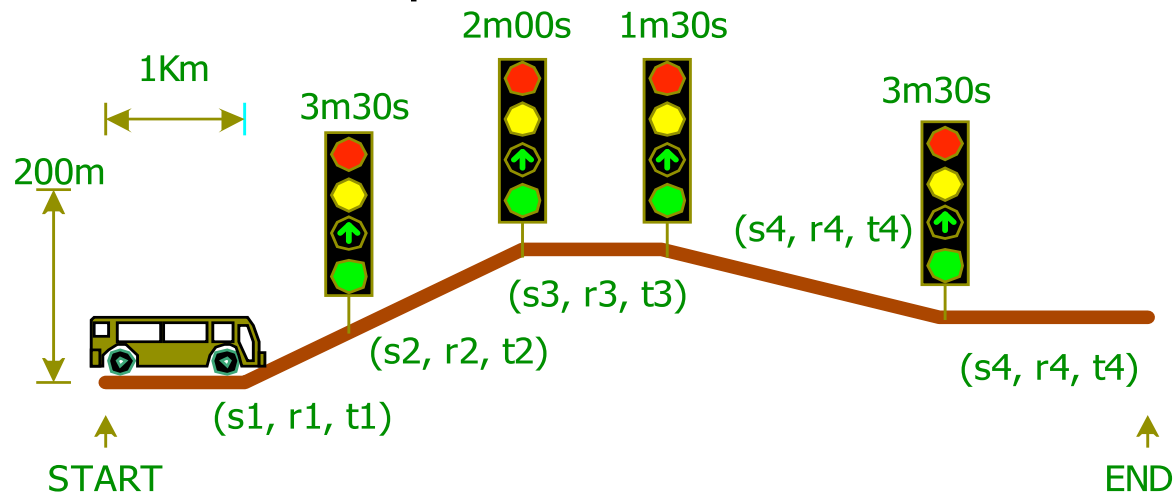
Light-weight bus



Low-loss transmission



- System-software-level energy optimization
 - City bus service example
 - Optimal speed, engine rpm, shift position scheduling w/original hardware
 - Analysis of a target route
 - Use of component characteristics



System-level approaches give us bigger chance to minimize energy consumption!

- Level of abstraction: engine idle gas consumption
 - Model 1: linear gas consumption per speed:
 $g = mv$
 - Model 2: counting idle gas consumption when $v=0$:
 $g = mv + I$
 - Model 3: counting engine restarting cost
 - Applicable gas saving techniques when a vehicle is temporarily parked
- Technique 1: linear gas consumption model
 - No policy when a vehicle is stopping
- Technique 2: Idle gas consumption
 - Stop engine whenever a vehicle is stopped
- Technique 3: Restarting cost
 - Stop engine when stopping time is more than 2 minutes for instance

Proper energy characterization is a primary concern of quality high-level power saving approach

- Study of state-of-the-art low-power techniques and survey presentation
- Latter part of the lecture
 - End of Dec. ~ end of Jan.
 - Will be also an important part of evaluation (30%)
- List of candidate papers will be given and each student will choose based on their preference and topic coverage

- Slides are modified from lecture notes of “Advanced Computer System Design” from Seoul National University (Lecturer: Prof. Naehyuck Chang)