Review: MOSFET Modeling and CMOS Circuits

Sangyoung Park

Chair for Real-Time Computer Systems

Technical University of Munich

sangyoung.park@tum.de

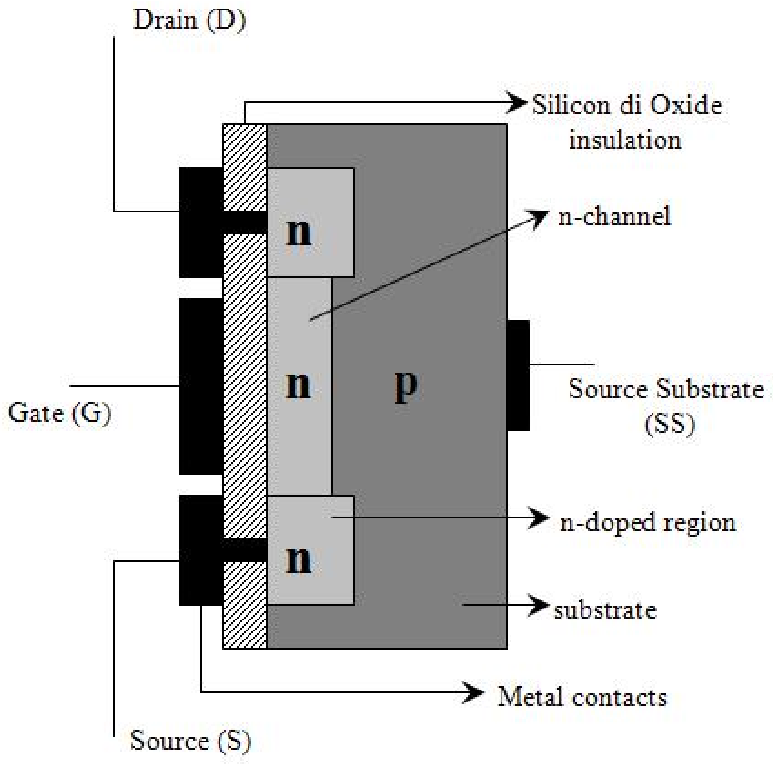
Why Recall MOSFET/CMOS?

- Complementary metal–oxide–semiconductor (CMOS)
  - Nowadays electronics devices are mostly implemented with CMOS technology
  - Need not recall all the details of the equations
  - Understanding qualitative relationship between the key parameters is more important
  - Will be the basis of understanding source of power consumption and low-power techniques

Contents

MOSFET Structure and Operation

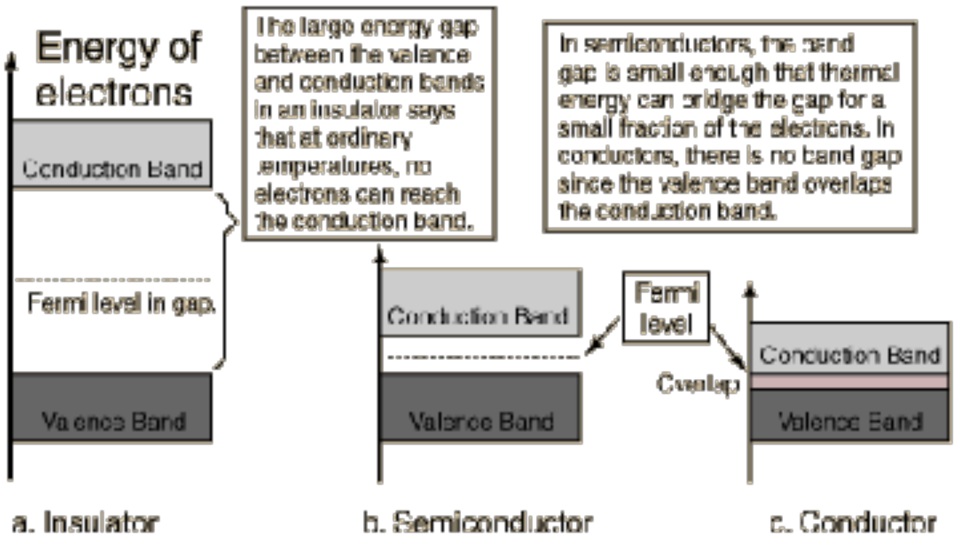
– MOSFET structure



www.wikipedia.com

MOSFET Operation

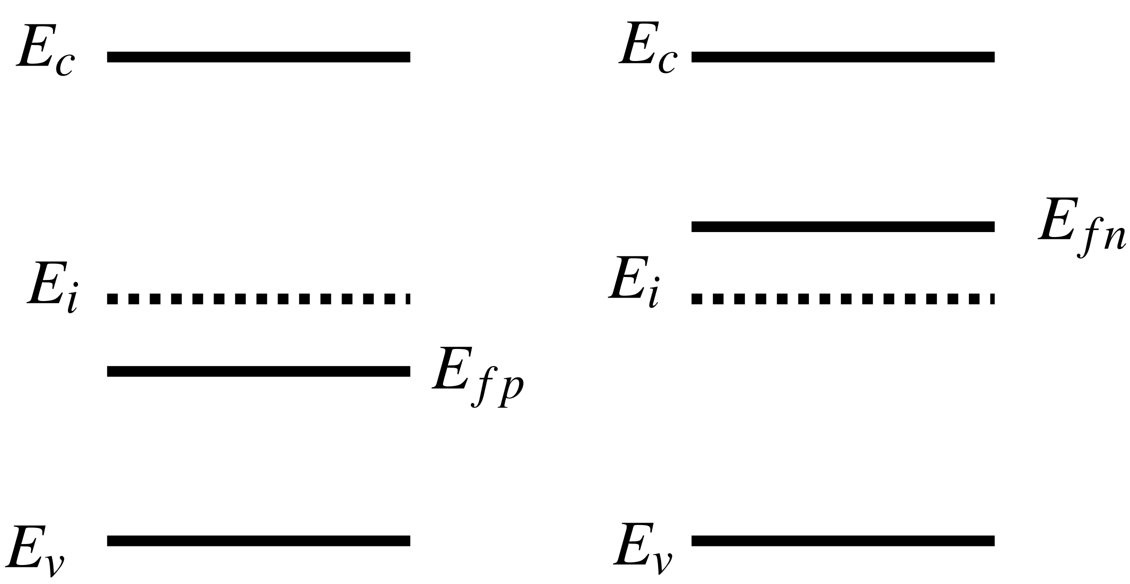
- Energy band diagram
  - Visualization of available energy levels for electrons in solid materials
- Fermi-level
  - Hypothetical energy level that would have 50% probability of being occupied by an electron



source: hyperphysics.phy-astr.gsu.edu

MOSFET Operation

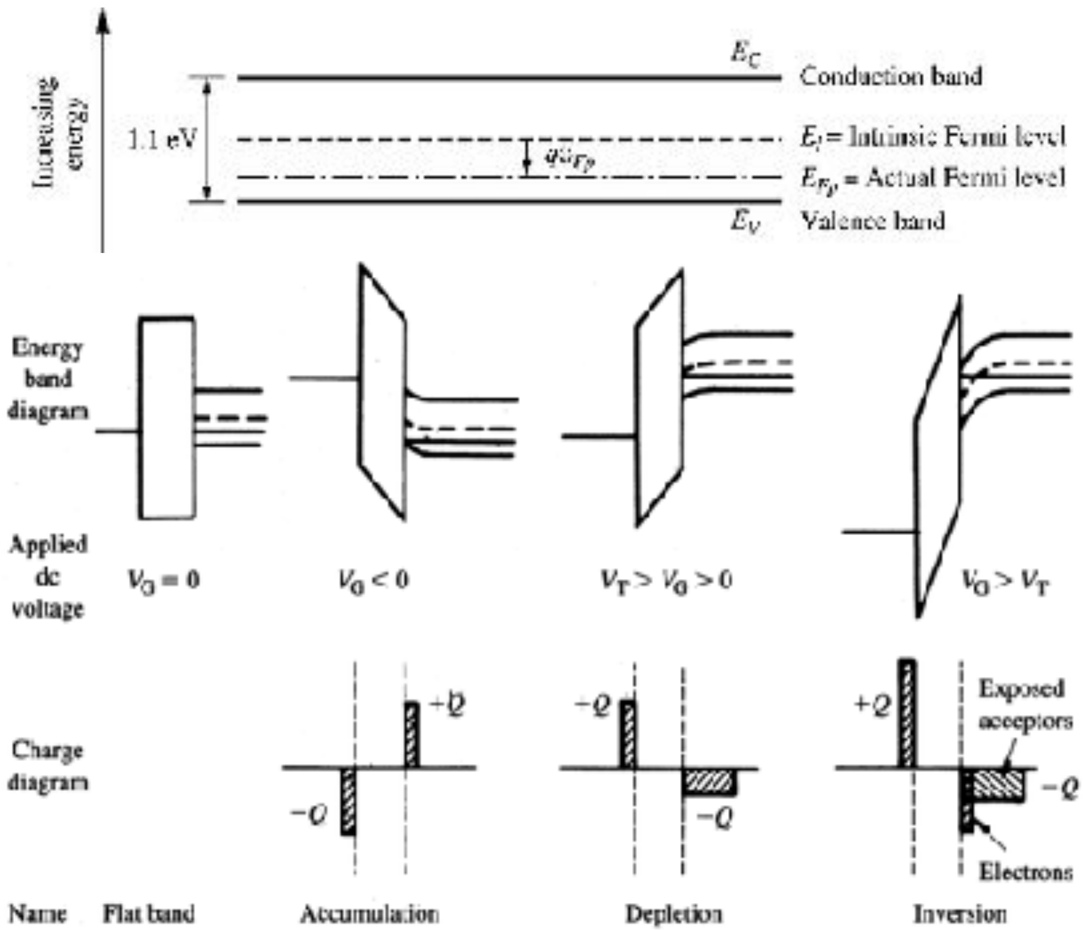
- Fermi level
  - Lies on the halfway in the band gap in case of semiconductors
  - Controllable by doping to p-type or n-type



E_i Intrinsic fermi level (no doping) E_f Actual fermi level (with doping)

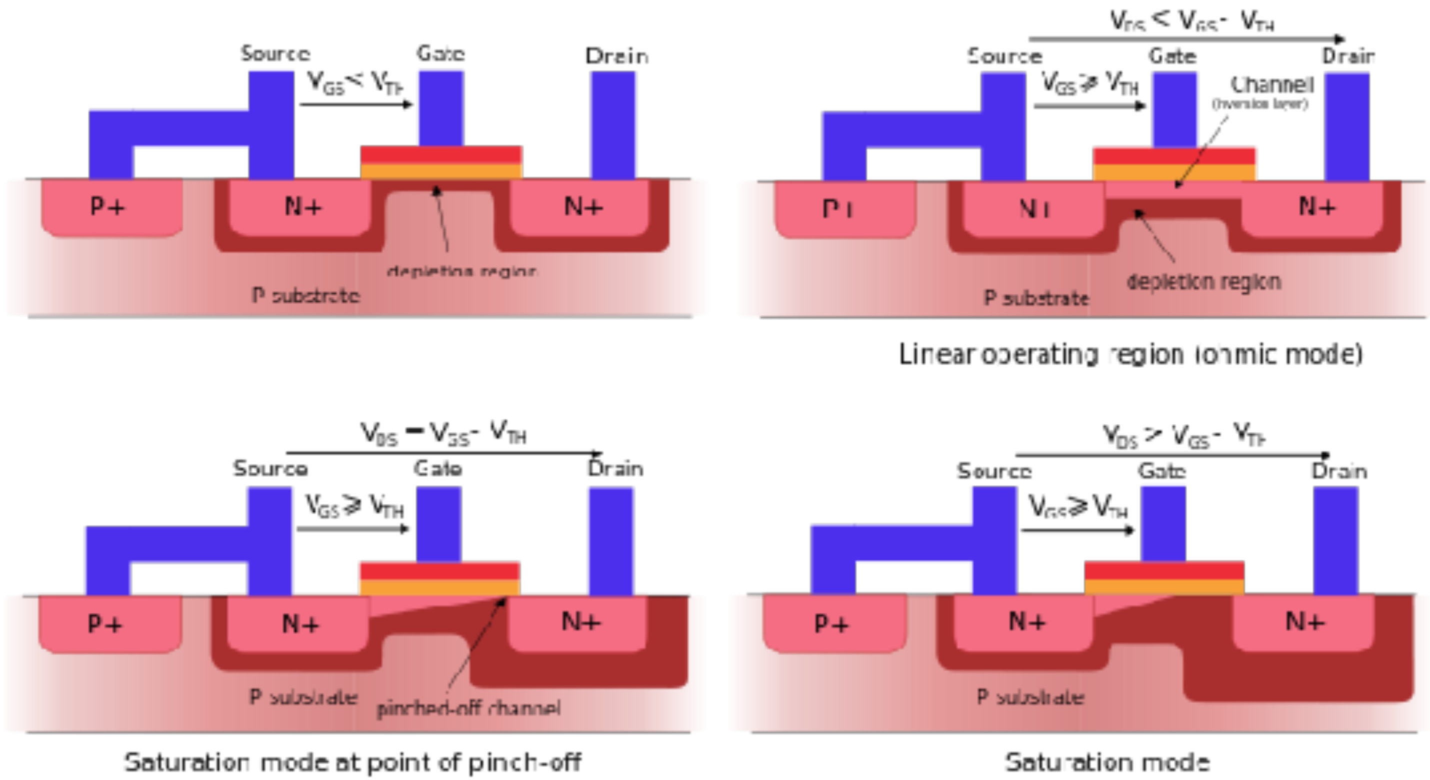
MOSFET Threshold Voltage

– Energy band diagram



MOSFET Structure and Operation

- Cut-off / sub-threshold / weak inversion mode
- Triode mode / linear region
- Saturation / active mode



reference: http://en.wikipedia.org/wiki/File:MOSFET_functioning.svg

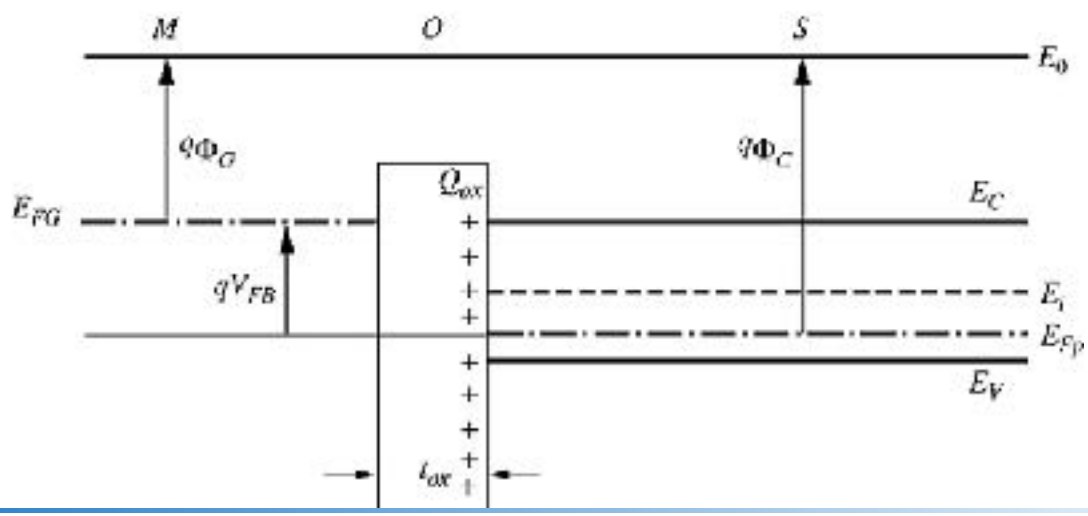
MOSFET Structure and Operation

- Depletion
  - Mobile holes are pushed down under the gate
- Weak inversion
  - Depletion layer thickness increases and an initial layer of mobile electron appears at the surface of the silicon
- Strong inversion
  - The concentration of the mobile electrons is increased until it becomes equal to the concentration of the holes in the substrate
  - Depletion layer thickness remains constant

MOSFET Threshold Voltage

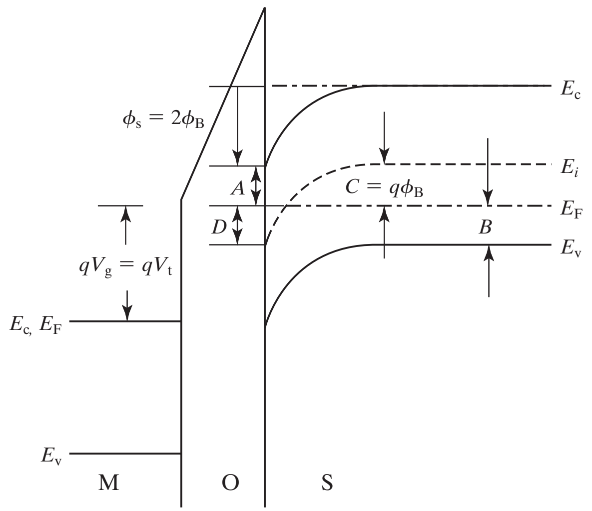
- Flat-band voltage: V_{FB}
  - The voltage that when applied to a MOS Capacitor produces zero net charge in the underlying semiconductor

$$F_{FB} = \phi_C - \phi_G$$



MOSFET Threshold Voltage

– V_{GS} required to produce strong inversion is threshold voltage V_T
  - The semiconductor surface that is normally p-type becomes n-type
  - Gate voltage where surface electron concentration equals bulk doping concentration (e.i. A=B)



Source: Chapter 5. C. Hu., "Modern semiconductor devices for integrated circuits", 2010

MOSFET Threshold Voltage

- Rearrangement of V_T

$$V_t = \phi_{gc} - 2 \cdot \phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$V_t = V_{t0} + \gamma \cdot \left(\sqrt{|-2 \cdot \phi_f + \boxed{V_{sb}}|} - \sqrt{|2 \cdot \phi_f|} \right)$$

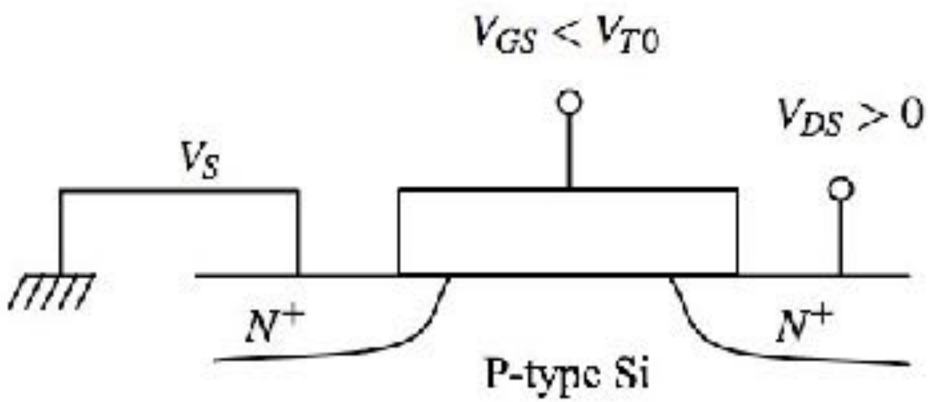
  - Source to bulk voltage has an effect on threshold voltage

- Body effect coefficient

$$\gamma = \frac{2 \cdot N_a \cdot \varepsilon_{si}}{C_{ox}}$$

1st-Order Current-Voltage Characteristics

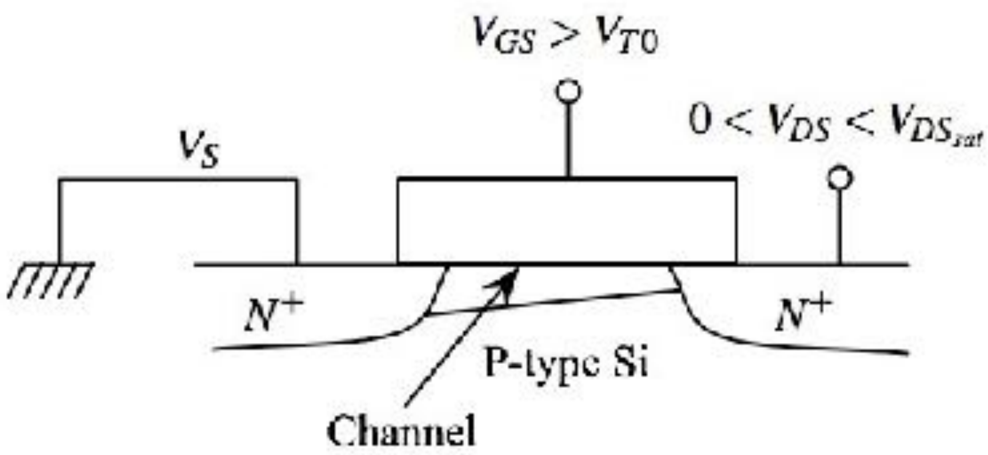
- Cut off
  - No inversion layer exists
  - Drain current is approximately zero



1st-Order Current-Voltage Characteristics

– Linear when

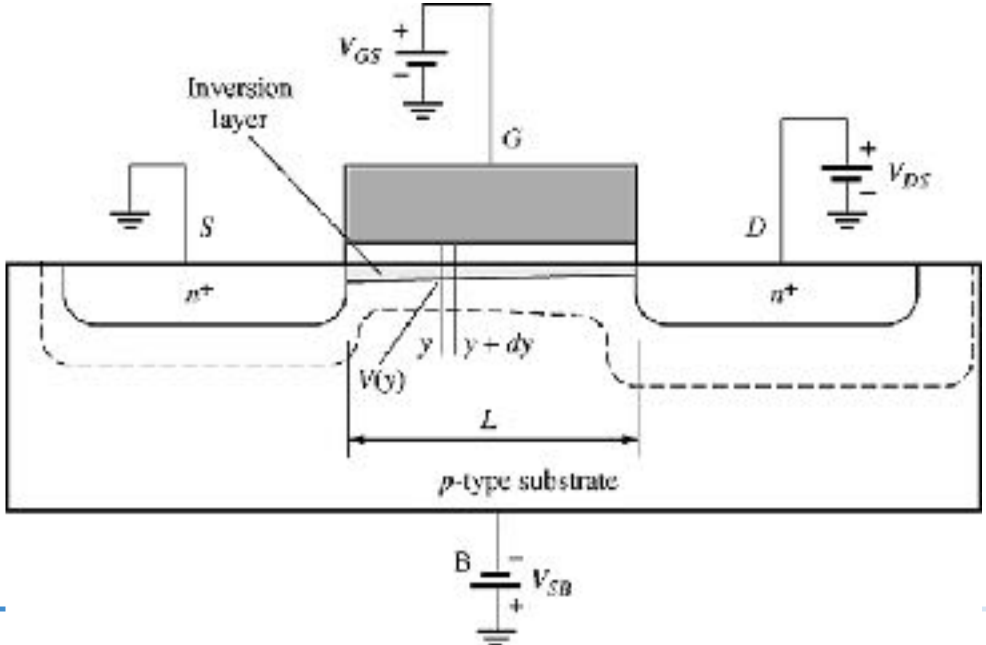
$$V_{GD} = V_{GS} - V_{DS} > V_T$$



1st-Order Current-Voltage Characteristics

- Drain current: $I_{DS} = Q_n \times \nu \times W$
- In the 1st order model, the velocity is linearly proportional to the E field

$$\nu = \mu E \text{ where } E = \frac{dV(y)}{dy}$$



1st-Order Current-Voltage Characteristics

- Drain current

$$I_{DS}dy = W\mu_n C_o x(V_{GS} - V(y) - V_T)dV$$

$$I_{DS}\int_0^L dy = W\mu_n C_{ox}\int_0^{V}{}_{DS}(V_{GS} - V - V_T)dV$$

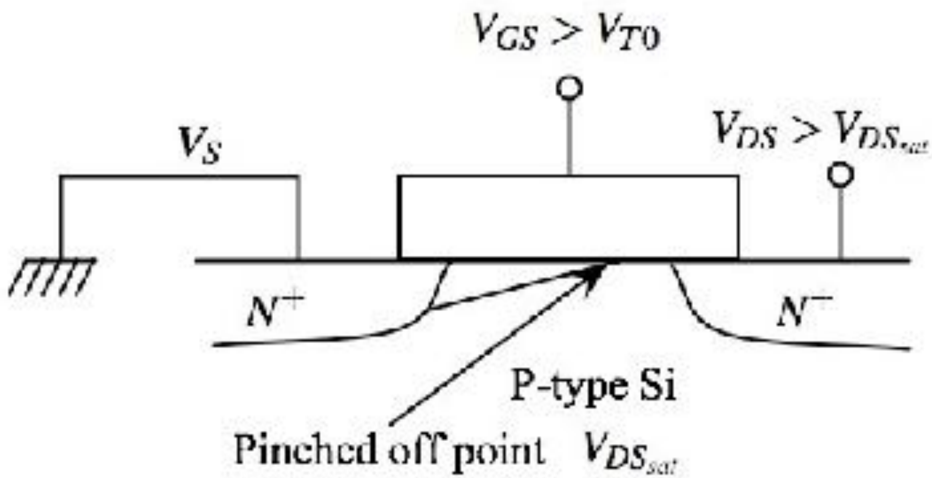
$$\boxed{I_{DS} = \frac{k}{2}\left(2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right)}$$

$$\text{where } k =' \frac{W}{L}, \text{ and } k' = \mu_n C_{ox}$$

1st-Order Current-Voltage Characteristics

− Saturation (pinched off)

$$V_{GS} > V_T, \; V_{DS} > V_{GS} > V_T$$



1st-Order Current-Voltage Characteristics

- Saturation voltage

$$V_{Dsat} = V_{GS} - V_T$$

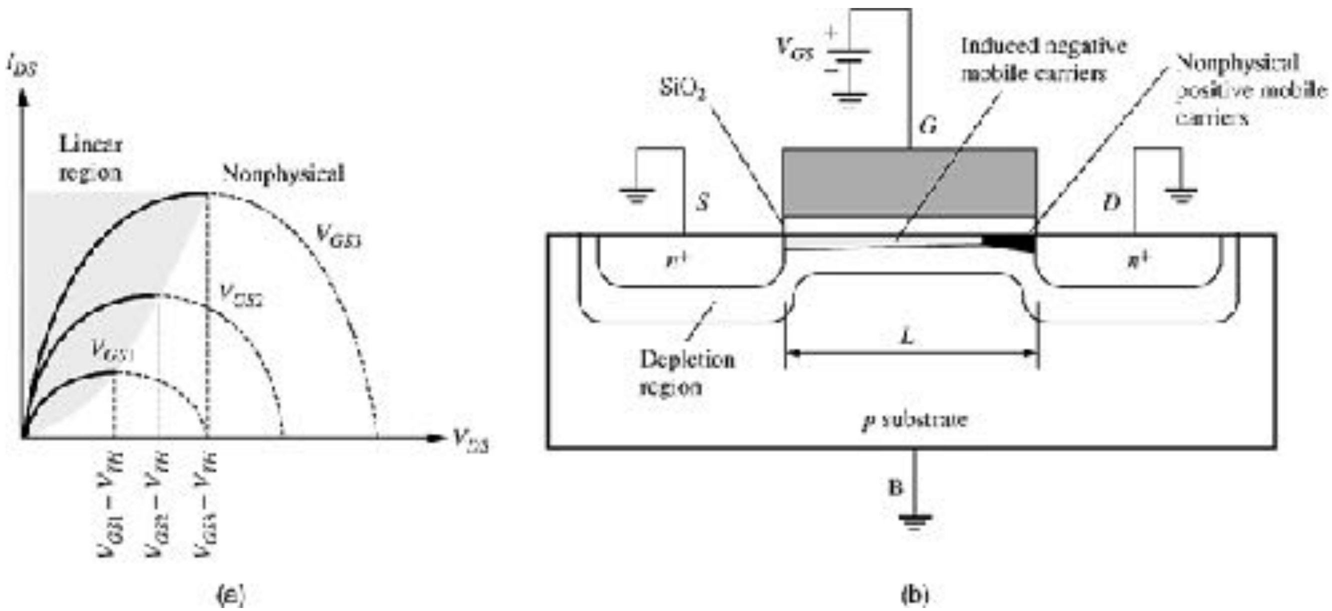
- Beyond the saturation voltage, I_{DS} is obtained by

$$V_{DS} = V_{GS} - V_T$$

$$I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2$$

1st-Order Current-Voltage Characteristics

− Channel-length modulation



1st-Order Current-Voltage Characteristics

- Channel-length modulation
  - Measured V-I characteristics show a weak function of V_{DS}

$$L' = L - \Delta L$$

Width of the depletion layer between the pinch-off point and the drain

$$\Delta L = \sqrt{2\frac{\varepsilon_{si}}{qN_A}(V_{DS} - V_{Dsat})^2}$$

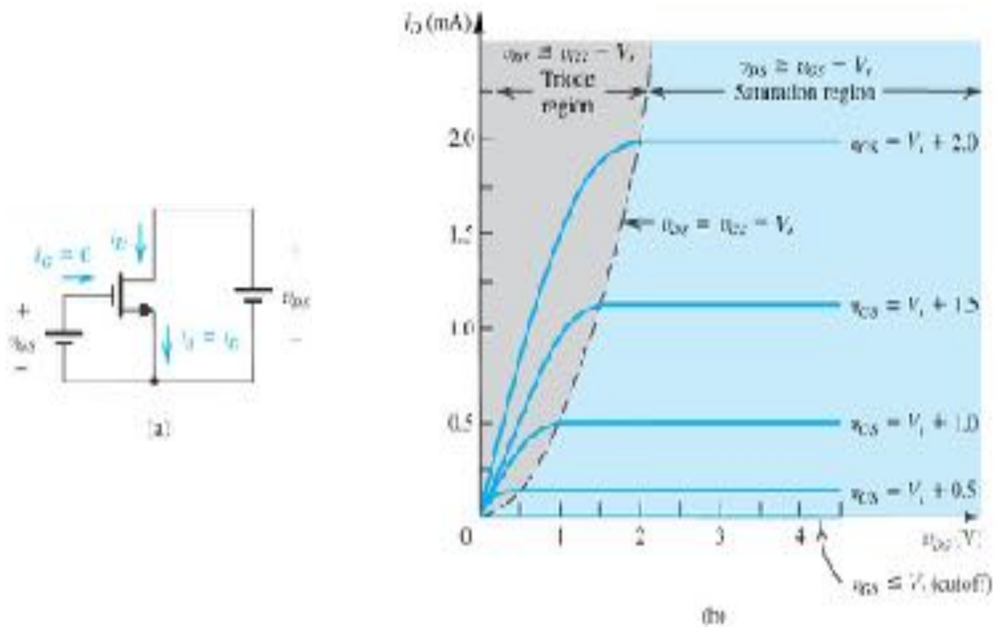
  - Corrected saturation current

$$I_{DS} = \frac{kW}{2L'}(V_{GS} - V_T)^2 = \frac{kW}{2L}(V_{GS} - V_T)^2 \frac{1}{1 - \frac{\Delta L}{L}}$$

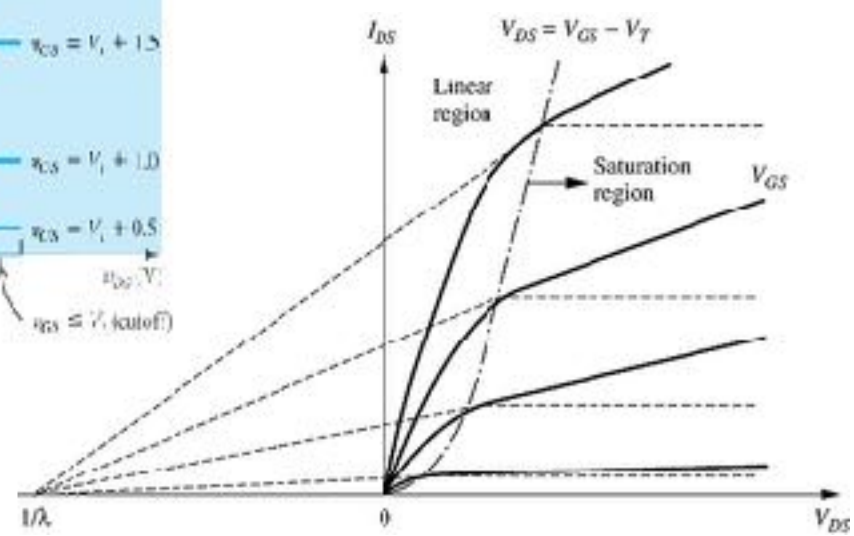
$$I_{DS} = \frac{k'}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

1st-Order Current-Voltage Characteristics

– The i_D–v_{DS} characteristics for a device with k'_n (W/L) = 1.0 mA/ V^2

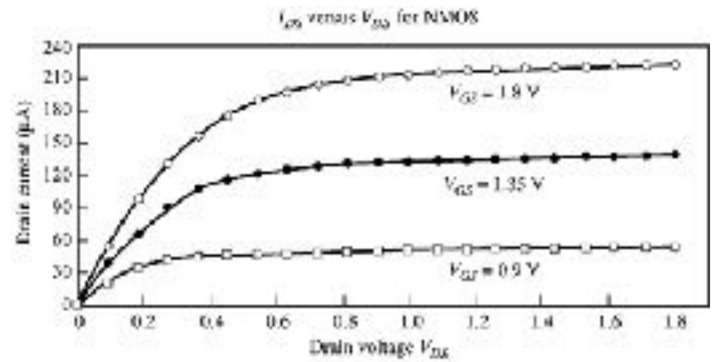


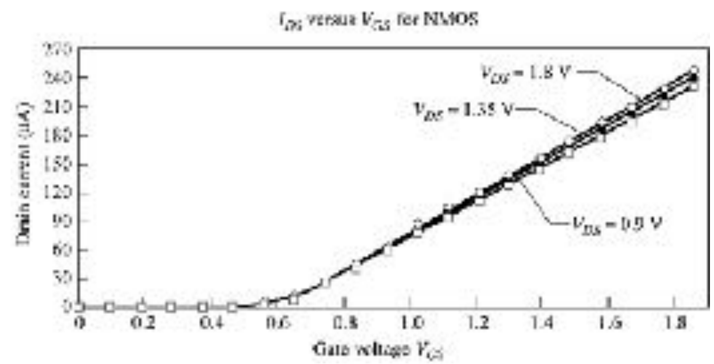
Channel-length modulation



Velocity Saturation

- Quadratic model is valid for long-channel devices
- Modern DSM devices
    - Channel length has been scaled to the point where the vertical and horizontal electric fields may interact
    - Saturation occurs at the pinch-off point is no longer valid
    - Saturation occurs due to velocity saturation
    - 0.18um device is rather linear than quadratic





Velocity Saturation

- Horizontal field acts to push the carriers to their velocity limit and cause
  - Early saturation
  - Mobility degradation
    - Due to electron scattering caused by dangling bonds at the Si-SiO_2 interface

$$\mu_e = \frac{\mu_o}{1 + \left(\frac{V_{GS} - V_T}{\theta t_{ox}}\right)^{\eta}}$$

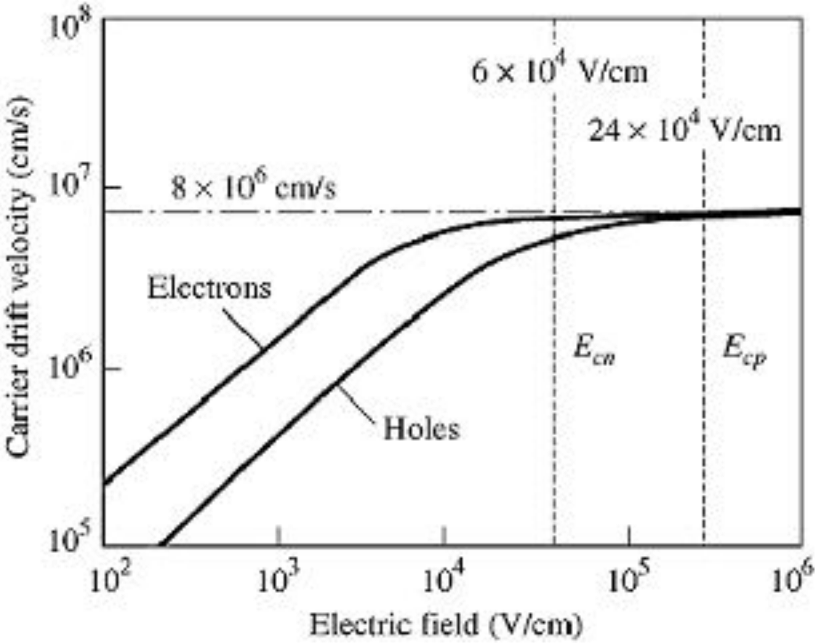
Empirical values

Velocity Saturation

– Piece-wise continuous model

$$\nu = \mu_e \frac{E_y}{1 + \frac{E_y}{E_C}} \qquad E_y < E_c$$

$$v = v_{sat} \; E_y \geq E_c$$



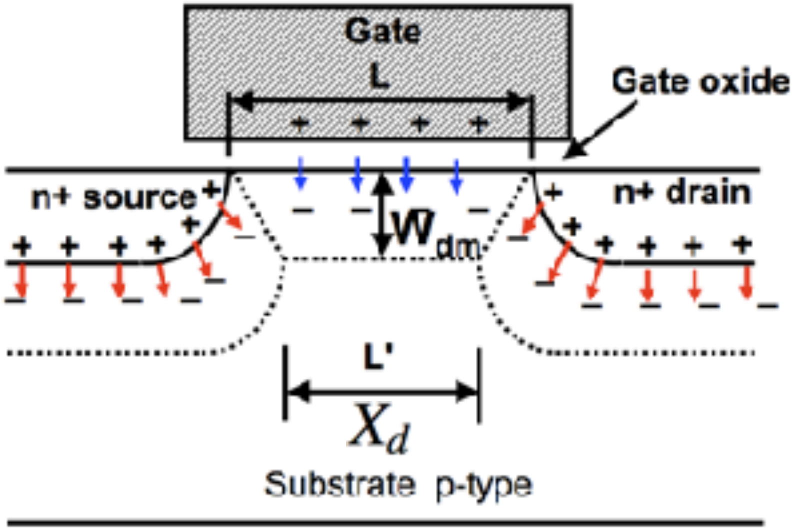
– Drain current

$$I_{DS} = W \nu_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{V_{GS} - V_T + E_c L}$$

Short-Channel Effect

− Short-channel effect
  - V_T roll-off: charge partitioning model

$$V_T = V_{FB} - 2\phi_F - \frac{Q_B}{C_{ox}}$$



  - Long channel

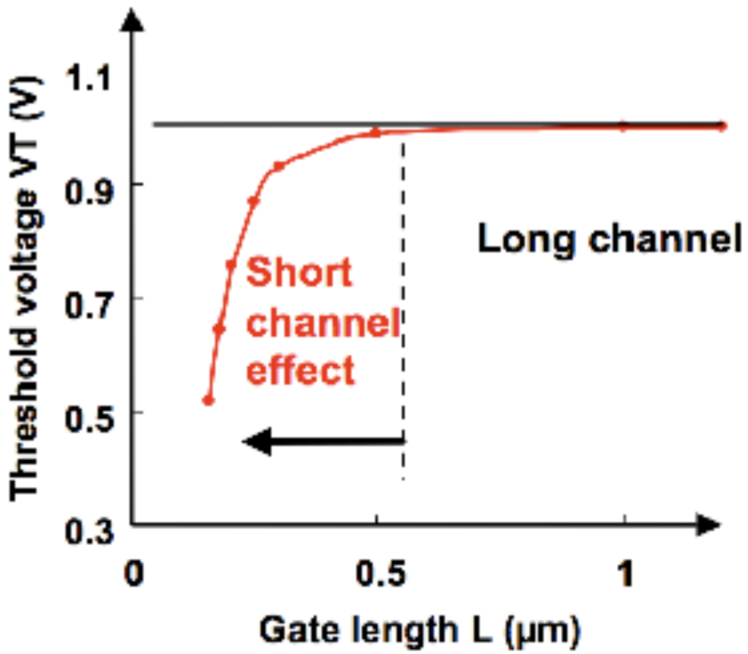
$$Q_B \propto X_d \times L$$

  - Short channel

$$Q_B' \propto X_d \times \frac{L+L'}{2} < Q_B \rightarrow V_T \text{ decreases}$$

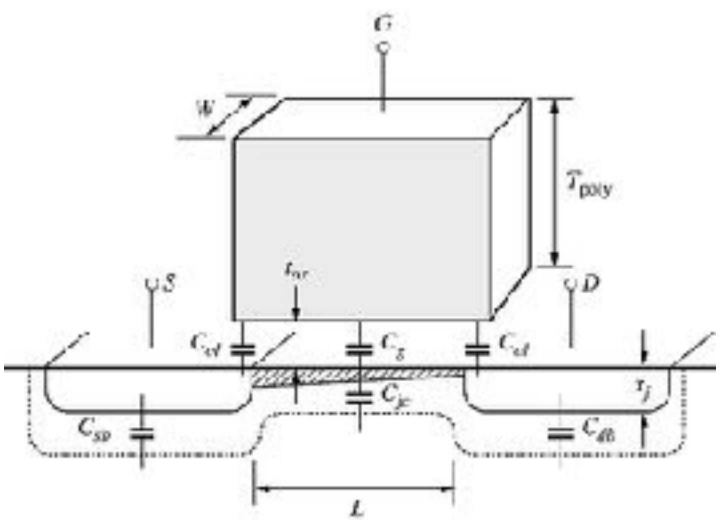
Short-Channel Effect

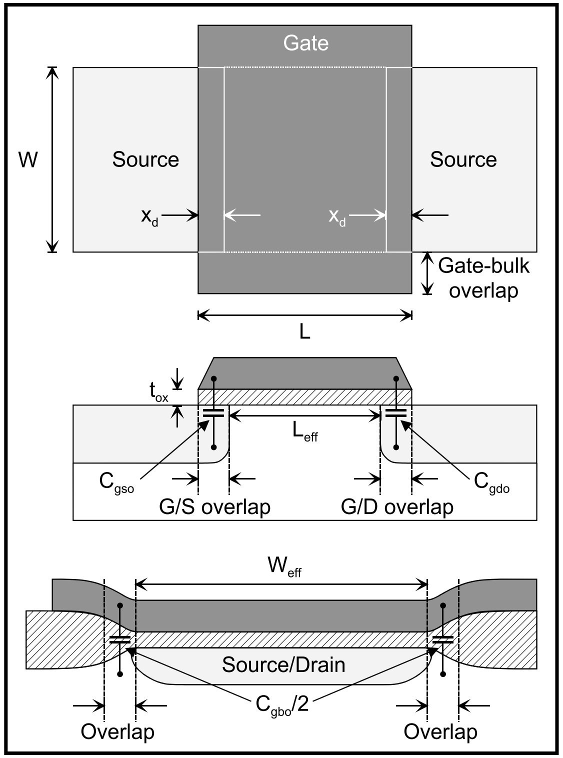
- V_T roll-off impact
  - Threshold voltage reduces as L reduces
  - I_{off} increases
  - Reduced control of the gate on the channel



MOS Capacitance

- Very important for transient simulation
  - Thin oxide capacitance: C_{gs}, C_{gd} and C_{gb}) represented by C_g
  - Junction capacitance (C_{sb} and C_{db})
  - Depletion layer capacitance (C_{jc}) associated with C_{gb}

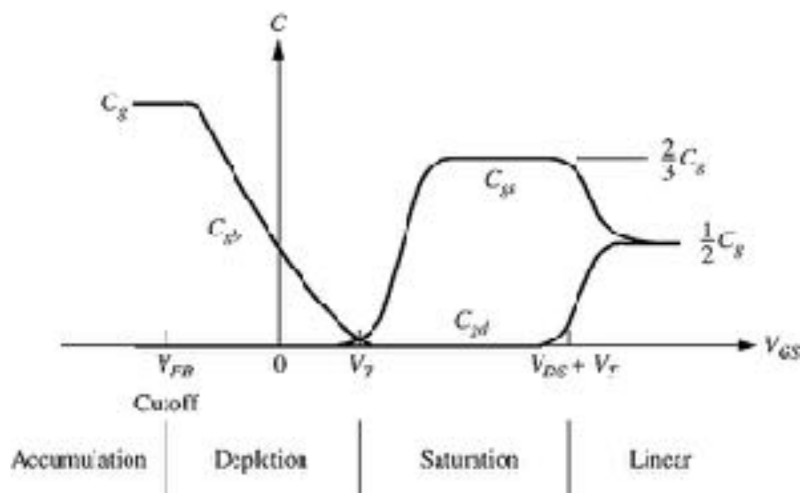




MOS Capacitance

- Thin oxide capacitance
  - The most important MOS capacitance
  - Two plates of the capacitance are defined as the gate and the channel
  - Cg remains constant for over 25 years because both L and t_{ox} are scaled at the same rate

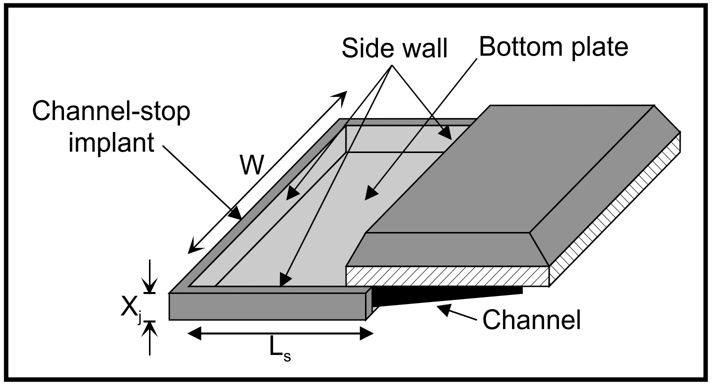
$$C_G = WLC_{ox} = WL\frac{\varepsilon_{ox}}{t_{ox}} = WC_g$$

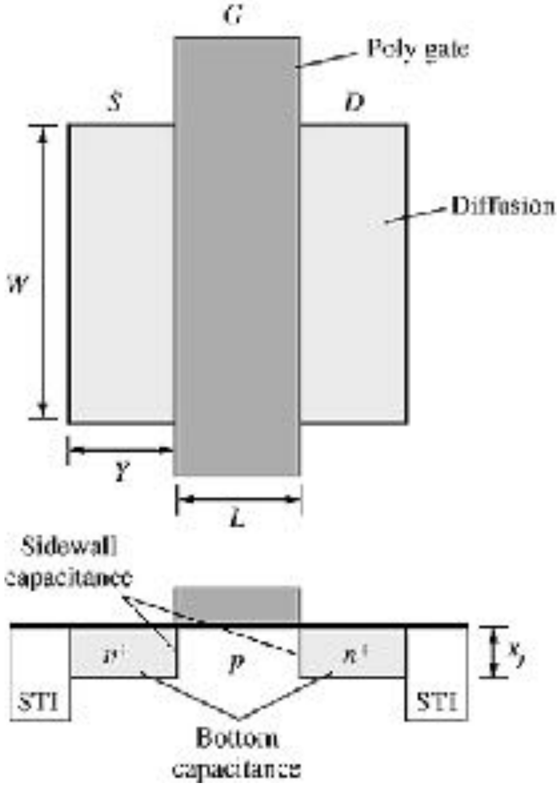


MOS Capacitance

- Area of source and drain
  - Bottom area: A_b=WY
  - Side wall area: A_{sw}=Wx_j
- Junction capacitance

$$C_J = \frac{C_{jb}A_b}{\left(1-\frac{V_J}{\phi_B}\right)^{mj}} + \frac{C_{jsw}A_{sw}}{\left(1-\frac{V_J}{\phi_B}\right)^{mjsw}}$$





Note

- Slides are modified from lecture notes of "Advanced Computer System Design" from Seoul National University (Lecturer: Prof. Naehyuck Chang)