Low power reduction techniques for Ultra Low Power Processors

Karthik Sukumar
Department of Electrical and Computer Engineering
Technical University Munich (TUM)
Munich, Germany
karthik.sukumar@tum.de

***Abstract*—In this paper the works of J.Zhou et al. [1] and J.Tang et al. [2] on design techniques for an ultra low-power processor is reported.**

J.Zhou et al. focusses on Near-Threshold processor design for Ultra low power processors. The paper discusses these design challenges, performance issue and solutions of the above. The circuit level power reduction techniques are addressed here.

J.Tang et al. discusses a case study by using GPS to demonstate that an Ultra-low power processor used along with a heavy applications processor can lead to further power savings. The architectural level power reduction techniques are addressed here. reduction techniques.

***Index Terms*—Near threshold, Ultra low power, GPS, Offload Co-processor, Interrupt service routines**

I. Introduction

Power constraint portable devices (e.g. Mobile phones, wearables, IoT devices) require ultra low power processors in order to save battery life. Such low power devices enable operation with energy harvesters or small baterries. Sub and Near-Threshold devices have been shown to have an overall low power consumption and past works confirm that Near Threshold designs are more efficient than using clock and power gating.

For further reduction of power consumption without loss of performance we need to look at architectural level improvements to preseve scalabililty.

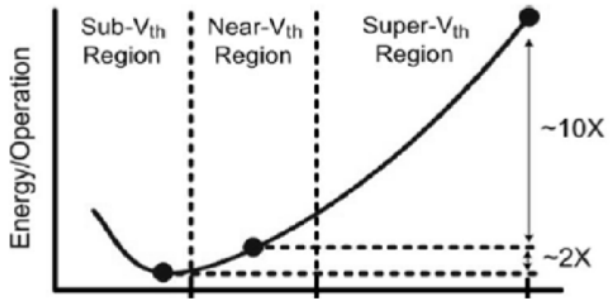

Fig. 1. Sub/Near-threshold operation. Source: [1]

The major advantage of using the near threshold devices is the decrese in Near-Threshold designs refer to operating the transistor slightly above the threshold region.

Dynamic power per operation is given by ($P_{dyn} = fC_LV_{DD}^2$), and increases quadratically with voltage but static power per operation increases with decreasing voltage. This is because the static power is constant and it increases as the time period per operation increasing. Hence by adding the two we get a relationship as shown in Fig. 1. Although we see that the sub-threshold operation has lower energy than the near-threshold, we want to find a balance between performance and energy per operation and hence we will investigate the functionality, variability issues and performance challenges of Near-Threshold design in this paper.

II. Functional Challenges of Near-Threshold Design

In the past many works have shown that Near-threshold design is easy to implement for ALUs and logic gates. But SRAM and level Shifter have their challenges in operating in the near-threshold region.

A. Level Shifters

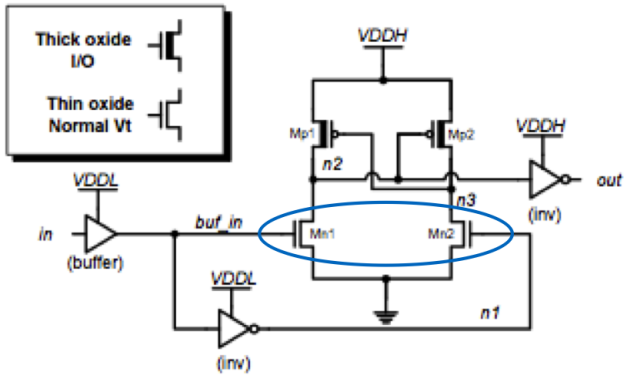

Fig. 2. Weak Pull ups Source: [3]

In the near-threshold operation the pull down network as shown in the Fig. 2 is weaker than the pull up network and consequently the the level shifter cant pull down to ground.

The issue of converting a near-threshold voltage to a super-threshold voltage therefore needs complex circuitry which is not only low power in nature but also scales in performance with voltage.

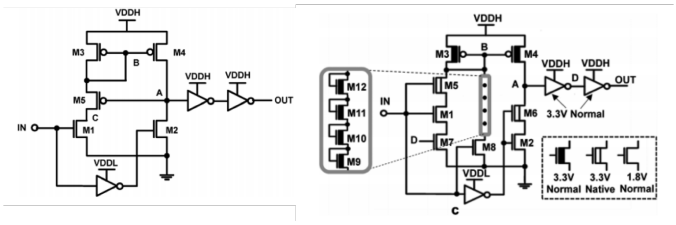

Fig. 3. Weak Pull ups Source: [6]

In [4] [5] [6], current mirrors based design is suggested which provides performance scalablity and high energy efficiency as shown in Fig. 3.

B. SRAM Design Challenges

SRAM prefers small transistors for increased density but

III. Performance Improvement for Near-Threshold Devices

A. Near-Threshold Device Sizing

B. Wide Dynamic Voltage Scaling

C. Parallel Processing

IV. Manufacturing Variabilty Challenges

A. Library Pruning

B. Pipeline Optimization

V. Architectural Level Power Reduction Techniques

For high performance embedded devices we need to consider architectural design changes to maintain the performance. The Application Processor(AP) is the most power consuming component in the design. In order to reduce the power consumption as much as possible we need to wake up the AP only when its absolutely necessary. Given that the peak workload on most mobile embedded devices is often periodic interrupts or user requests we can utilise this to offload the AP of servicing these routines.

This is illustrated with the help of a case study to show the advantages of using an Ultra Low Power Offload Co-processor(OCP), which could be one of the processors incorporating all the circuit level design techniques described in the earlier sections.

A. Case Study: GPS

GPS is chosen for our case study as it usually samples at 1Hz and is a periodic event. Research has shown that GPS can consume upto 95% of the total power consumption of the mobile device [7].

The system we are considering here is a typical ARM11 micro-processor which is commonly found in most mobile phones these days. Fig. 4 shows that intially the CPU is in sleep mode consuming 20mW before the interrupt occurs. The interrupt is excuted in 2ms (at 1000mW) and then cant drop straight away to sleep mode, instead it must operate at a lower frequency consuming 650mW for 100ms. It drops into another mode at 400mW for another 100ms. Only after excuting in all these intermediate modes does the CPU go back into deep sleep. Therefore although the interrupt only takes 2ms to execute the application processor remains active for over 200ms consuming 60mJ of energy.

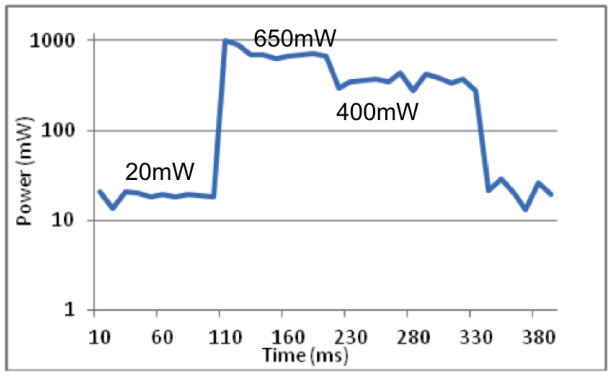

Fig. 4. Power Profile when a GPS interrupt occurs for an ARM11 CPU: [2]

An alternative SoC design with a OCP is shown in Fig. 5. In our case study the Application Processor is an ARM11 CPU and the OCP is a MIPS32 4KS.

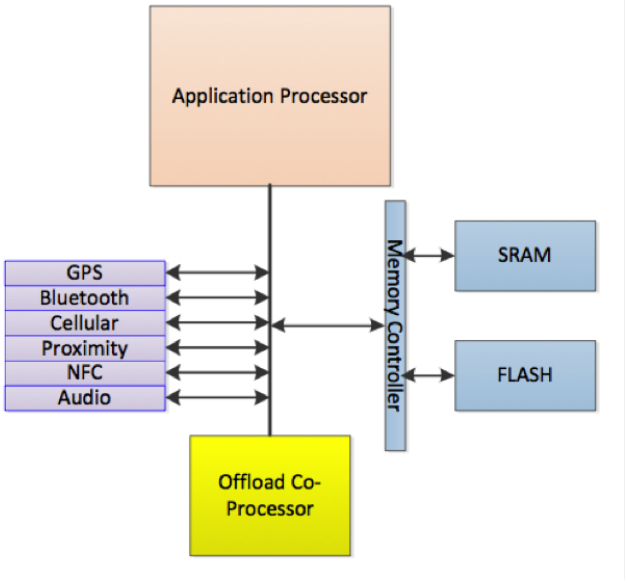

Fig. 5. SoC Design with Offload Co-Processor(OCP): [2]

B. Considerations for OCP Design

1) Different ISA:

VI. Conclusion

Circuit design techniques are required to tackle the major challenges of the near-threshold processor design. Architectural design techniques are required to add additional power and energy saving. We have demonstrated from the OCP based SoC design that the battery life can be extended by 3.5 times by adapting the hybrid approach.

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