

Experimental Evaluation of Machine Learning based Wireless Communication Algorithms

Master Thesis

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Abstract

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Acronyms

| | |
|--------------|----------------------------------------------------|
| AFW | Application Framework. |
| AWGN | Additive White Gaussian Noise. |
| BS | Base Station. |
| CRS | Cell Specific Reference Signal. |
| FPGA | Field Programmable Gate Array. |
| GSM | Global System for Mobile communication. |
| IEEE | Institute of Electrical and Electronics Engineers. |
| LTE | Long Term Evolution. |
| MIMO | Multiple Input Multiple Output. |
| OCXO | Oven Controlled Oscillator. |
| OFDM | Orthogonal Frequency Division Multiplexing. |
| PCIe | Peripheral Component Interconnect Express. |
| PDCCH | Physical Downlink Control Channel. |
| PDSCH | Physical Downlink Shared Channel. |
| PLL | Phase Locked Loop. |
| PPS | Pulse Per Second. |
| PSS | Primary Synchronisation Signal. |
| RF | Radio Frequency. |

Acronyms

| | |
|------------|-----------------------------------|
| SNR | Signal to Noise Ratio. |
| SSS | Secondary Synchronisation Signal. |
| UE | User Equipment. |
| VCO | Voltage Controlled Oscillator. |

Introduction 1

System Model 2

As mentioned in Chapter 1, the goal of this thesis is to obtain measurement data from the MIMO setup. This collected experimental data will be applied to the machine learning model which has been developed in parallel with this thesis. In this chapter the relevant fundamentals of the LTE standard, which will be used as a basis for our experiments are described on a high level.

2.1 LTE

LTE stands of Long Term Evolution and is a successor standard to UMTS. LTE is a multicarrier approach for multiple access which uses Orthogonal Frequency-Division Multiple Access (OFDMA) in the physical layer. OFDM uses multiple carriers (known as sub carriers) spaced equally apart and can transmit independent data streams on each sub carrier [2].

Hence an LTE frame is commonly represented as a 2D time frequency grid, where the vertical axis represents the sub-carriers(Frequency) and the horizontal axis represents time. LTE also comes in 2 flavours Frequency Division Duplexing (FDD) and Time Division Duplexing (TDD). In this thesis the focus will be on FDD systems, which use seperate frequency bands, for uplink and for downlink data respectively. The advantage of an FDD system is that the uplink and downlink transmission can happen simultaneously.

LTE has a certain predefined signal symbol structure according to the standard [3]. In the following sections the frame structure and the different symbols in the LTE Frame shall be introduced.

2.2 LTE Waveform Processing

LTE stands of Long Term Evolution and is a successor standard to UMTS. LTE is a multicarrier approach for multiple access which uses Orthogonal Frequency-Division Multiple Access (OFDMA) in the physical layer. OFDM uses multiple carriers (known as sub carriers) spaced equally apart in frequency and can transmit independent data

streams on each sub carrier [2]. LTE also comes in 2 flavours Frequency Division Duplexing (FDD) and Time Division Duplexing (TDD). In this report the focus will be on FDD systems, which uses separate frequency bands for uplink and for downlink data so that the uplink and downlink data can be transmitted simultaneously.

LTE was chosen as a standard to use for the communication system given the integrated support of simulation environments like MATLAB and Simulink and that it is currently widespread in the telecommunications industry.

2.2.1 Transmission

A dual antenna transmitter using a USRP software defined radio as mentioned in 4.1 is used for the interface. A modified version of the LTE Application framework with MIMO 2x2 extension is used to log the data and run with different parameters. The transmitter USRP is connected to a Host PC using a 4-lane PCIe connection. This is necessary for the high data throughput exchanged between the host and the devices.

LTE has a standardized frame structure which is commonly represented as a 2D time frequency grid, where the vertical axis represents the sub-carriers and the horizontal axis represents time. LTE also uses a predefined signalling structure according to the standard [3]. In the following sections the frame structure and the symbols relevant to channel estimation shall be introduced.

2.2.1.1 LTE Frame

A single frame is 10ms long and consists of 10 smaller units called subframe, each 1ms long. A symbol is the smallest unit of time for an LTE system and one subframe has 14 such symbols each approximately 66.7us long. Scheduling is normally done on a subframe basis for both uplink and downlink communication.

LTE's time frequency grid contains many different signals each performing specific functionality like broadcasting, control channel information, data transfer, among other functions.

For the purpose of channel estimation, the most important signals are Primary Synchronisation Signal(PSS), Secondary Synchronisation Signal (SSS) and Cell Specific Reference Signal (CRS) which are described in detail in the subsequent sections.

2.2.1.2 Primary Synchronisation Signal (PSS)

OFDM is extremely time and frequency sensitive, hence it is very important to know the exact start of every frame. The PSS helps to achieve the synchronisation of

the frame by using a specific sequence called the Zadoff-Chu sequence [3]. The Zadoff-Chu sequence has the property of constant amplitude zero autocorrelation waveform (CAZAC sequences) that cyclically shifted versions of the waveform are orthogonal to each other. The sequence is described in Equation 2.1 where u can be 25, 29 or 34 depending on the cell ID. The PSS is broadcast twice every radio frame and the symbols are identical each time.

$$d_u(n) = \begin{cases} e^{-j \frac{\pi u n(n+1)}{63}} & n = 0, 1, \dots, 30 \\ e^{-j \frac{\pi u n(n+1)(n+2)}{63}} & n = 31, 32, \dots, 61 \end{cases} \quad (2.1)$$

2.2.1.3 Secondary Synchronisation Signal (SSS)

The SSS is a 62 bit pseudo random sequence [3]. It is broadcast twice in a frame once in subframe 0 and once in subframe 5, one symbol before the PSS. The 2 sequences of transmission in a frame are different so that the UE can identify which position in the frame the synchronisation happens.

2.2.1.4 Cell Specific Reference Signal (CRS)

As mentioned in Chapter 1 the channel needs to be estimated in order to reverse the channel propagation effects. With the help of CRS the channel can be estimated by placing equally spaced reference symbols along every 6 subcarriers starting from subcarrier 2 on symbols 1, 8, 15, etc... and every 6 subcarriers starting from subcarrier 5 on symbols 5, 12, 19, etc...[3]. The signals received by the UE and the channel effects are inferred based on amplitude damping and phase shift. Placing the signals in the above defined spacing gives the best coverage to interpolate over in time and frequency.

The signals to be placed on the grid are decided by the Equation 2.2 as shown below, with the parameters defined in Table 2.1 [3].

$$r_{l,n_s}(m) = \frac{1}{\sqrt{2}}(1 - 2 \cdot c(2m)) + j \frac{1}{\sqrt{2}}(1 - 2 \cdot c(2m+1)), \quad m = 0, 1, \dots, 2N_{RB}^{max,DL} - 1 \quad (2.2)$$

| Parameter | Description |
|-------------------|---------------------------------------------|
| $c(m)$ | Pseudo Random Sequence defined in [3] |
| $N_{RB}^{max,DL}$ | Maximum number of Downlink resources blocks |
| n_s | Slot number in the frame |
| l | OFDM Symbol number in the frame |

Table 2.1: Parameter definitions for evaluating CRS Symbols

2.2.1.5 Final Waveform

All the signals mentioned in Section 2.2.1.1 are generated in Labview using the LTE Application Framework Software and arranged in a 2D grid of frequency and time as shown below in Figure 2.1. The CRS are placed every 6 subcarriers in the frequency domain and every 3 or 4 time symbols apart, according to the position on the grid. Where as the PSS and SSS only repeat every 5 subframes.

Figure 2.1: Resource Block Grid for 2 sub frames

One of the disadvantages of using OFDM in the physical layer is the high peak to average power ratio (PAPR) of the signal. High PAPR translates to high fidelity requirements of power amplifiers on the transmitter side. It also induces non-linear distortions to the signal [2]. To ensure that the PAPR of the signal is as low as it can be, random QPSK symbols are transmitted on the unused slots instead of 0s.

2.2.2 Reception

For the LTE receiver processing a USRP captures in bursts and streams the data to a laptop connected via a USB interface. The signals are processed by a custom MATLAB application which performs the necessary steps to decode the LTE Frames, estimate the channel and display the information as a 3D surface. For the case of the demo the data was processed as soon as they were received from the USRP and the channel estimate was displayed in realtime. The data can alternatively be logged for offline postprocessing to get better granularity as intermittent processing delays dont appear.

Once enough samples have been captured (usually 2 or more Frames) the data can be processed in the following steps.

2.2.2.1 Carrier Offset Estimation and Correction

OFDM is extremely sensitive to frequency shifts in the received signal. In the case that the receiver or transmitter center frequency clock was not accurate enough, the frequency shift needs to be estimated and corrected. This is the very first step before processing the baseband waveform.

2.2.2.2 Frame synchronisation

As mentioned in Section 2.2.1.1 the synchronisation is a very important part of knowing where the LTE frame begins. This is done by correlating the received signal with the known Zadoff Chu Sequence and to look for the peak. Figure 2.2 shows an example correlation of a Zadoff Chu sequence and a received signal containing 307200 samples in total amounting to 2 frames of a 10MHz Bandwidth LTE signal. 4 peaks are to be expected here as there are 2 frames, each containing 2 PSS sequences.

Figure 2.2: PSS Correlation

2.2.2.3 Channel Estimation

Once the frame has been demodulated and the 2D OFDM grid has been obtained, the channel can be estimated based on the original pilot symbols structure known to the receiver, hence the phase and amplitude of the particular sub carrier can be obtained. A 2D Wiener filter is applied in both the time and frequency axis to interpolate the channel estimate. More explained in the Chapter 3.

2.2.3 Antenna

The analog time domain signal is transmitted from the USRP (Section 4.1) over the air using a Triband antenna. For the setup an omni directional Antenna from TODO capable of transmitting and receiving around frequencies of 144, 400 or 1200 MHz. This antenna shown in Figure 2.3 was used as the transmit and the receive antenna for the demo setup.



Figure 2.3: Narrowband Omnidirectional Antenna used for transmitting and receiving the LTE Signals

Channel Estimation 3

LTE was chosen as the standard to use here as it is very mature and has readily available MATLAB/Labview based implementation. In the case of this thesis the aim is not to reinvent standard by redesigning pilot symbol placements. Instead existing standards were used in order to collect experimental data. This reduces design time and focusses more on the issue at hand which is channel estimation data of a MIMO Channel.

3.1 OFDM

LTE is based on OFDMA in the physical layer which is a multi carrier communication scheme [4]. As the name suggests OFDM uses orthogonal sub carriers from an orthonormal system to form the basis for independent data streams. For band limited transmission systems with finite access time per channel use the dimension of the parallel data stream is given by the equation 3.1 [1].

$$N = BT \quad (3.1)$$

| Parameter | Description |
|-----------|---------------------|
| N | Dimension of system |
| B | Signal Bandwidth |
| T | Channel access time |

Table 3.1

The orthonormal basis function can be mathematically modelled as the equation 3.2 [1].

$$\begin{aligned} \psi_{b,q} &= p_{T_b}(t) \exp(j2\pi q \frac{t}{T}) \\ p_{T_b}(t) &= \begin{cases} 1; & t \in T_b \\ 0; & otherwise \end{cases} \end{aligned} \quad (3.2)$$

| Parameter | Description |
|--------------|-----------------------------------------|
| $\psi_{b,q}$ | normalized orthogonal basis functions |
| b | channel access slot |
| q | sub carrier index |
| T | channel access time |
| T_b | $bT \leq t < (b+1)T \subset \mathbb{R}$ |

Table 3.2

The transmitted data can hence be modelled as the following

$$x_b(t) = \sum_{q=0}^{N-1} \underbrace{X_{b,q}}_{\text{data}} \psi_{b,q}(t) \quad (3.3)$$

For a given ideal AWGN Channel, where there is no delay spread or multipath propagation, the corresponding received data is modelled as

$$y_b(t) = \sum_{q=0}^{N-1} x_b(t) \psi_{b,q}(t) + \eta_b(t) \quad (3.4)$$

where $\eta_b(t)$ is the additive noise

The demodulation is based on the same set of orthonormal basis vectors as that of the transmitter, hence we have

$$\hat{x}_{b,q} = \langle y, \psi_{b,q}(t) \rangle + \langle \eta_b, \psi_{b,q}(t) \rangle = x_{b,q}(t) + \eta_{b,q} \quad \forall q = 1, \dots, N \quad (3.5)$$

In the case of a channel with a delay spread (also referred to as multipath propagations) we model it as the following

$$h(t) = \sum_{l=0}^{L-1} h_l \delta(t - l \frac{T}{N}) \quad (3.6)$$

this causes the term $h_l x_{b,q} \psi_q(t - l \frac{T}{N} - bT)$ which leads to interference between adjacent channels T_{b-1}, T_b, T_{b+1} , etc.

3.1.1 Cyclic Prefix

As a result of Equation 3.6 we have to compensate for the interference of the symbols of the b_{th} channel with the other channels. A simple solution to this interference

is a Cyclic prefix. As the name suggests it is a cyclic addition of the signal at the transmitter end, which means copying the beginning of the signal and adding it to the end. To this end $T = T + T_p$, where T_p is the duration of the cyclic prefix. In the LTE standard the durations are predefined based the normal or extended mode [3]

$$\psi_{b,q}(t) = p_{T_b}(t) \exp\left(j2\pi q \frac{t}{T}\right) \quad (3.7)$$

where $\psi_{b,q} \in T_b = [-T_p + bT_s, bT_s + T[$

This is illustrated in the Figure 3.1

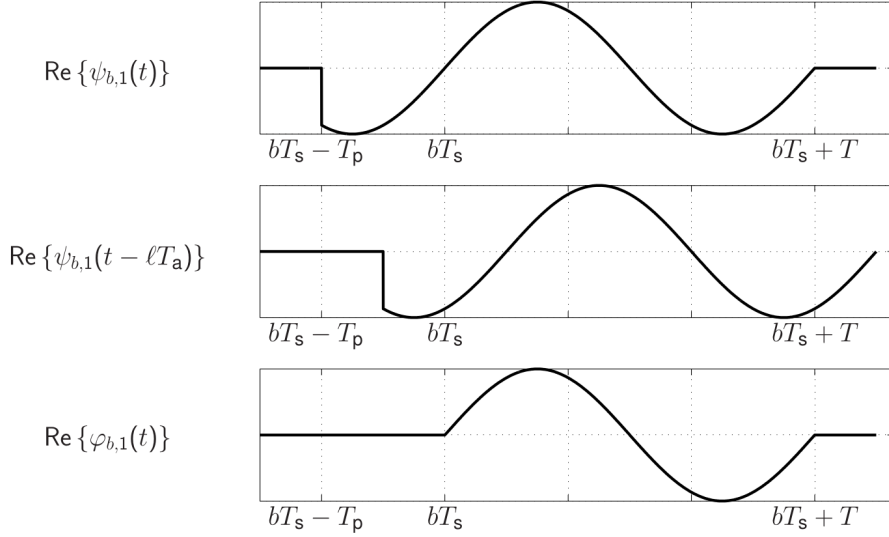


Figure 3.1: Cyclic prefix addition [1]

On the receiver end

$$y_{b,n} = \sum_{l=1}^{L-1} h_l \delta_{n-l} * \sum_{k=-N_p}^{N-1} x_{b,k} \delta_{n-k} = \sum_{l=1}^{L-1} \sum_{k=-N_p}^{N-1} h_l x_{b,k} \delta_{n-l-k} \quad (3.8)$$

subject to $L - 1 \leq N_p$, where N_p is the number of samples of the cyclic prefix

$$y_{b,n} = \sum_{l=1}^{L-1} h_l x_{b,n-l} = \sum_{l=1}^{L-1} h_l x_{b, \text{mod}_N(n-l)}, \quad n, q \in 0, \dots, N-1 \quad (3.9)$$

$$y_{b,n} = h_n \circ x_{b,n} \Leftrightarrow \frac{1}{N} Y_{b,q} = H_q X_{b,q}, \quad n, q \in 0, \dots, N-1$$

$$\begin{bmatrix} y_{b,-2} \\ y_{b,-1} \\ y_{b,0} \\ y_{b,1} \\ y_{b,2} \\ y_{b,3} \end{bmatrix} = \begin{bmatrix} h_0 & & & & & \\ h_1 & h_0 & & & & \\ h_2 & h_1 & h_0 & & & \\ & h_2 & h_1 & h_0 & & \\ & & h_2 & h_1 & h_0 & \\ & & & h_2 & h_1 & h_0 \end{bmatrix} \begin{bmatrix} x_{b,-2} \\ x_{b,-1} \\ x_{b,0} \\ x_{b,1} \\ x_{b,2} \\ x_{b,3} \end{bmatrix} + \begin{bmatrix} h_2 & h_1 & & & & \\ & h_2 & & & & \\ & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \end{bmatrix} \begin{bmatrix} x_{b-1,2} \\ x_{b-1,3} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} \eta_{b,-2} \\ \eta_{b,-1} \\ \eta_{b,0} \\ \eta_{b,1} \\ \eta_{b,2} \\ \eta_{b,3} \end{bmatrix} \quad (3.10)$$

With a cyclic prefix chosen such that $x_{b,-n} = x_{b,N-n}$, $n \leq N_p$, then $x_{b,-1}$ and $x_{b,-2}$ can be deleted and equation 3.10 can be rearranged as the following

$$\begin{bmatrix} y_{b,0} \\ y_{b,1} \\ y_{b,2} \\ y_{b,3} \end{bmatrix} = \begin{bmatrix} h_0 & & h_2 & h_1 \\ h_1 & h_0 & & h_2 \\ h_2 & h_1 & h_0 & \\ & h_2 & h_1 & h_0 \end{bmatrix} \begin{bmatrix} x_{b,0} \\ x_{b,1} \\ x_{b,2} \\ x_{b,3} \end{bmatrix} + \begin{bmatrix} \eta_{b,0} \\ \eta_{b,1} \\ \eta_{b,2} \\ \eta_{b,3} \end{bmatrix} \quad (3.11)$$

Taking the DFT of equation 3.11 gives

$$y_b = \hat{H} x_b + \eta_b \Leftrightarrow Y_b = \frac{1}{N} F \hat{H} F^H X_b + F \eta_b \quad (3.12)$$

Where F is the Fourier matrix. Since \hat{H} is a circulant matrix (also a convolutional matrix) it can be broken down as equation 3.13 [5]. The eigenvalues of the circulant matrix are the Fourier transformed coefficients of the first column while the eigenvectors are the columns of the inverse Fourier transform matrix. Equation 3.13 presents a eigenvector decomposition of matrix H where F^H is the inverse DFT matrix and Λ is the diagonal matrix with entries being the Fourier transform terms of the first column of the matrix H .

$$\hat{H} = U \Lambda U^{-1} = \frac{1}{N} F^H \Lambda F$$

$$\frac{1}{N} F \hat{H} F^H = \Lambda \quad (3.13)$$

Therefore equation 3.12 simplifies to

$$\begin{aligned}
Y_b &= \Lambda X_b + F\eta_b \\
\text{or} \\
Y_b &= \text{diag}(X_b)H + F\eta_b
\end{aligned} \tag{3.14}$$

where Λ , is a diagonal matrix and H is the vector of channel coefficients in the frequency domain and decouples the subcarrier distortions with each other. Because of the cyclic prefix converting linear convolution into cyclic convolution, the received signal in the frequency domain is linearly dependent **only** on the corresponding frequency component of the channel propagation effect.

3.1.2 Pilot assisted channel estimation

In order to determine the channel propagation effects known pilot symbols are inserted in the transmit frames as mentioned in section 2.2.1.4 and the channel effects are inferred from the demodulated symbol on the receiver side. Although populating all the subcarriers with pilots is the best approach, this leads to high channel reference signal overheads and less data bandwidth. Hence in practical system implementations the only P out of N subcarriers carry the pilots and the rest are interpolated.

$$Y = XSH + \eta \tag{3.15}$$

$Y \in \mathbb{C}^P, H \in \mathbb{C}^N, \eta \in \mathbb{C}^P$ are vectors

$X = \text{diag}[X_1, \dots, X_P] \in \mathbb{C}^{P \times P}$

and $S : \mathbb{C}^N \rightarrow \mathbb{C}^P \Rightarrow H \mapsto H_P = [H_{s1}, \dots, H_{sp}]^T$. where S is the selector matrix which selects P out of N subcarriers which carry the pilot symbols.

For non fully loaded OFDM systems which is typical in the real world the equation 3.15 reduces to the equation below.

$$Y_P = XH_P + \eta \tag{3.16}$$

where $H_P = SH$. A least squares estimate of the H_P gives

$$\hat{H}_{P,LS} = X^{-1}Y_P \tag{3.17}$$

H_P is then subsequently interpolated across all the N subcarriers. This can be done in many ways using either

- Linear interpolation
- Sinc interpolation

- Cubic/Spline interpolation
- Wiener filters

3.2 MIMO Channel Estimation

For the MIMO channel estimate the basics is the same as described in the section 3.1.2, except in a $N_t \times N_r$ system we have $N_t N_r$ possible channels per subcarrier. This is explained as follows, from figure 3.2 it can be seen that there are $N_t N_r$ channels per subcarrier in the frequency domain. Equation 3.15 is used to calculate each channel. This is enabled by non interfering pilots for different antennas. This **must** be followed for faithful channel estimation and is a necessary criteria which has been followed in the LTE standard.

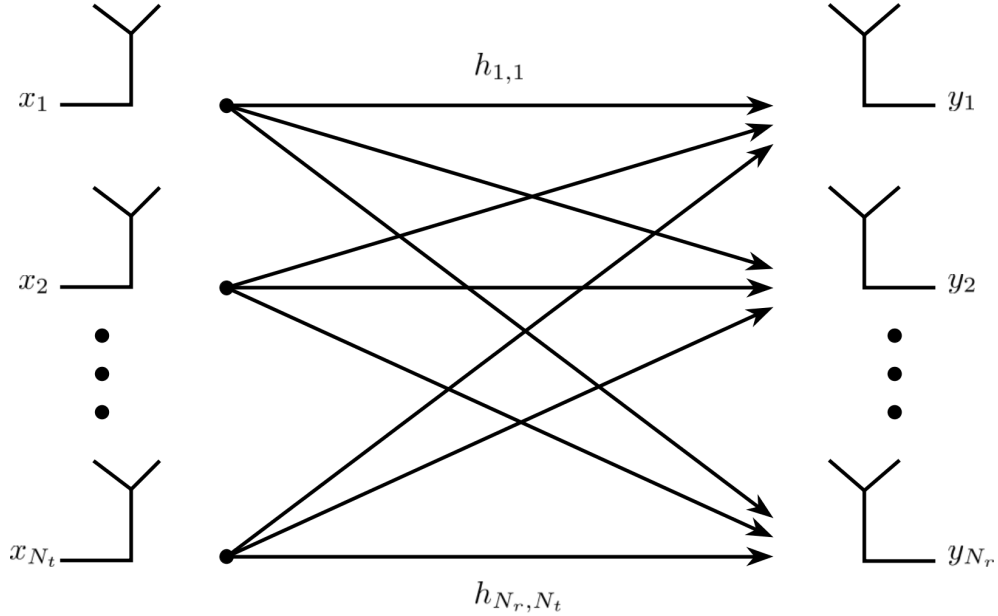


Figure 3.2: MIMO channel model

$$\hat{x} = Wy \quad (3.18)$$

Once the channels propagation effects have been calculated each symbol has to be equalized to compensate the distortion effect caused by the dispersive channel. In the case of a MIMO channel there are 3 main algorithms which are

3.2.1 Maximum Ratio Combiner

$$W_{MRC} = C \hat{H}^H \quad (3.19)$$

where C is a diagonal matrix with

$$C_{k,k} = \left(\sum_m |H_{m,k}|^2 \right)^{-1} \quad (3.20)$$

and can be considered as a normaliser for the columns of the matrix H .

3.2.2 Zero Forcing

$$W_{ZF} = (\hat{H}^H \hat{H})^{-1} \hat{H}^H \quad (3.21)$$

Zero forcing is an algorithm that is avoided although given its simplicity, the reason being that the noise can be amplified in the case of a low SNR situation. Hence in practice this algorithm is avoided. The implementation is a Least squares estimate of the vector \hat{x}

3.2.3 MMSE

$$W_{MMSE} = (\hat{H}^H \hat{H} + \sigma^2 I)^{-1} \hat{H}^H \quad (3.22)$$

where σ is the inverse SNR.

MMSE algorithm performs the best under all situations. For high SNR scenarios it converges to an ZF algorithm and for a low SNR situation it converges to the MRC algorithm.

Potential Hardware Setups

4

MIMO channel measurements can be achieved using multiple methods. This chapter discusses some of the potential approaches which were tested and elaborates each of their advantages and disadvantages. A detailed final implementation is described in Chapter 5 where the setup configurations are discussed. The following are some possible realisation for a MIMO Setup.

4.1 Software Defined Radios USRP

USRP is a Software Defined Radio (SDR) designed by National Instruments that enables quick prototyping of different wireless applications. It is aimed at hobbyists, research labs, universities, etc... or anyone interested in evaluating custom algorithms. The SDR used in this masters thesis is a USRP2940, specifications of which are described in Table 4.1.

| | |
|-------------------------|-----------------------------|
| Model | USRP2940 |
| Baseband Bandwidth | 40MHz |
| RF-Operating Frequency | 50MHz-2200MHz |
| FPGA | Kintex-7 410T |
| No of Transmitters | 2 |
| No of Receivers | 2 |
| Connectivity | MXIe, Ethernet |
| Oscillator | Internal Crystal |
| ADC/DAC | 14 (For Rx)/16 (For Tx) bit |
| Frequency Accuracy | 2.5 ppm |
| Maximum Power Output | 20dBm |
| Maximum I/Q Sample Rate | 200MHz |

Table 4.1: USRP2940 SDR Product details

4.1.1 PCIe-8371

The USRP SDRs are PXIe communication based devices. They connect to a Host/PC using a 1/4/8 way PCIe slot. For this setup a 4 lane PCIe daughter card (*PCIe-8371*) was installed on the motherboard of the host PC to provide a dedicated PCIe communication port for the USRP.

4.1.2 Host

The host chosen to be used here is a Fujitsu Celcius M770 with the following specifications.

| | |
|----------------------------------|-----------------------------------------------------------------------------------|
| OS | Microsoft Windows 10 Education |
| Version | 10.0.18363 Build 18363 |
| OS Manufacturer | Microsoft Corporation |
| Systemname | TUEIMSV-PRAKT01 |
| Manufacturer | FUJITSU |
| Systemmodel | CELSIUS M770 |
| Systemtype | x64-based PC |
| System-SKU | S26361-Kxxx-Vyyy |
| Processor | Intel(R) Xeon(R) W-2123 CPU @ 3600 MHz 4 Cores, 8 logical Processors |
| BIOS-Version/-Date | FUJITSU // American Megatrends Inc. V5.0.0.13 R1.8.0 for D3498-A1x, 08.10.2019 |
| SMBIOS-Version | 3.2 |
| BIOS-Modus | UEFI |
| BaseBoard-Manufacturer | FUJITSU |
| BaseBoard-Product | D3498-A1 |
| BaseBoard-Version | S26361-D3498-A1 |
| Platform Type | Workstation |
| Installed Physical Memory | 16,0 GB |
| Total Physical Memory | 15,6 GB |

Table 4.2: Fujitsu Celcius M770 Configuration

Streaming a Custom LTE Waveform into the 2 separate USRP trasnmitters, would have been the simplest and the ideal solution. However since the 2 transmitters on a single device are not time synchronised, which is essential for MIMO transmission

and reception, this was not an option. The details of the issues are described in the Appendix A.2.

4.2 MIMO Application Framework (MIMO AFW)

MIMO Application Framework (MIMO AFW) is a Software developed by National Instruments, that offers a comprehensive plug and play MIMO setup. This setup requires a host of additional hardware which are required for the functioning of the MIMO AFW [6]. When setup with all the required Hardware MIMO AFW can support a Multi-user system with a maximum of 128 Antennas on the Base Station (BS) side and upto 12 Antennas on the User Equipment (UE) side.

A list of different Hardware parts needed to run this MIMO AFW is listed in Table 4.3. There are many different MIMO configurations possible and the hardware requirements of each of these configurations are mentioned in Table 4.4. A high level system overview of the main features of MIMO AFW is as follows

- Multi-User MIMO transmission between one Base Station (BS) with up to 128 Antennas and up to 12 single antenna Mobile Stations (MS)
- Single-user MIMO transmission between one BS with up to 128 antennas and one MS with up to 12 antennas
- Modulation Schemes from QPSK to 256 QAM
- Automatic gain control (AGC) at the BS and MS
- FPGA based real time signal processing such as modulation, over-the-air synchronization, MIMO equalization and MIMO precoding
- Scalable number of antennas (multi-antenna MS: between 2 and 12; BS: between 2 and 128). Interfaces and configuration adapt automatically
- Fully reconfigurable LTE like radio frame structure
- Bi Directional TDD and FDD functionality transmission of 20MHz bandwidth
- FPGA based real time signal processing such as modulation, over-the-air synchronization, MIMO equalization and MIMO precoding

| Part Number | Description |
|-------------|-------------------------------|
| USRP-2940 | SDR |
| PXle-7976 | FPGA Module for FlexRIO |
| CDA-2990 | Clock Distribution Device |
| CPS-8910 | Switch Device for PCI Express |
| PXle-6674T | Synchronization Module |
| PXle-1085 | Chassis |
| PXle-8135 | Controller |

Table 4.3: Additional Hardware for required for MIMO AFW to function

| | 128-antenna BS 8 subsystems | 64-antenna BS 4 subsystems | 32-antenna BS 2 subsystems | 16-antenna BS 1 subsystems | 8-antenna BS 1 subsystems |
|--------------------------------------------------------------|--------------------------------|-------------------------------|-------------------------------|-------------------------------|------------------------------|
| USRP-29xx SDR Reconfigurable Device | 64 | 32 | 16 | 8 | 6 |
| PXle-1085 Chassis (18-Slot, 24 GB/sSystem Bandwidth (BW)) | 1 | 1 | 1 | 1 | 1 |
| PXle-8135 Controller | 1 | 1 | 1 | 1 | 1 |
| PXle-7976 FPGA Module for FlexRIO | 5 | 3 | 2 | 2 | 2 |
| PXle-6674T Synchronization | 1 | 1 | 1 | 1 | 1 |
| CDA-2990 Clock Distribution Device | 8 | 5 | 3 | 1 | 1 |
| CPS-8910 Switch Device for PCI Express | 8 | 4 | 2 | 1 | 1 |

Table 4.4: MIMO Configurations and HW requirements

4.2 MIMO Application Framework (MIMO AFW)

4.2.1 USRP 2940

As mentioned in Section 4.1, this is the backbone of the architecture. The Software defined radio (USRP2940) is used as an air interface for over the air transmission. There are host of other options that can be used here instead of the USRP2940. Table 4.5 lists the alternatives with an overview of the functionality of each of the parts.

4.2.2 PXIe-7976

MIMO has very demanding operations that are quite compute intensive such as precoding, equalization as well as channel estimation in the frequency domain. In addition to the aforementioned processing tasks this FPGA card also perform the *bit processing*. This PXIe communication based FPGA card contains a Xilinx Kintex-7 FPGA and moves data in and out using an 8 lane PCIe slot.

4.2.3 CDA-2990

This device also known as the Octoclock is a clock distribution accessory. It can either receive an input reference clock and distribute the clock to 8 other devices synchronously along with a PPS (Pulse Per Second). The CDA-2990 also contains an input for a GNSS Antenna which uses the GNSS signal to generate a PPS signal. In the absense of a GNSS Antenna the device generates its own internal clock based on an internal oven controlled oscillator (OCXO).

4.2.4 CPS-8910

The CPS-8910 is a 8 way PCIe data aggregator and has 2 upstream ports. With the 8 downstream ports it can aggregate large amounts of data from a maximum of 8 USRPs and send them out to a PC/Controller via the 2 other upstream ports. This is essential for Massive MIMO applications.

4.2.5 PXIe-1085

National instruments is a company that manufactures devices intended for different industries and end applications. Hence they follow a modular approach to their designs. The PXIe-1085 is an 18 slot chassis, which can be populated by many different daughter cards suitable to the customers needs. Out of the 18 slots 16 are hybrid that can be populated with various add ones, and one slot is reserved for a timing and synchronisation slot as described in section 4.2.6 and the other reserved for a

PXI-controller which is define in section 4.2.7. The chassis is capable of supporting a throughput of upto 24GBps.

4.2.6 PXIe-6674T

The PXIe-6674T generates and routes clocks and trigger signals (PPS Signals) between PXI devices or chassis. This timing and synchronisation card not only generates an accurate clock but can also shift levels of an input signal according to the user's settings. Although the octoclock distributes the clock, it is generated, synchronised and level shifted by the PXIe-6674T.

4.2.7 PXIe-8135

The PXIe-8135 is a PXI Controller needed to handle the different slot daughter cards installed in the *PXIe-1085* (section 4.2.5). Its a Intel Core i7 based embedded controller for PXI express systems. The controller also has a variety of ports to support the 10/100/1000BASE-TX Gigabit Ethernet, 2 SuperSpeed USB ports and four Hi-Speed USB ports, as well as an integrated hard drive, serial port, and other peripheral I/O.

4.2.8 Implementation Advantages and Disadvantages

The advantages of using MIMO AFW is that it reduces time to prototype as the functionality is readily available in the form of Hardware and Software, it is also a scalable model providing a solution with up to 128 BS antennas and 12 MS antennas. But given the amount of hardware required to have a minimum viable product, it is quite an expensive undertaking (over €100.000) and is hence cost preventative. Apart from that there is also the time cost to setup the instrument and check it functionality which is not to be neglected.

| Model | RF-Frequency Range | RF-Frontend Bandwidth | FPGA | Inputs | Outputs | Communication | GPS Osillator |
|--------------|---------------------------|------------------------------|---------------|---------------|----------------|----------------------|----------------------|
| USRP-2940 | 5 MHz - 2.2 GHz | 40 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | No |
| USRP-2940 | 50 MHz – 2.2 GHz | 120 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | No |
| USRP-2942 | 400 MHz - 4.4 GHz | 40 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | No |
| USRP-2942 | 400 MHz - 4.4 GHz | 120 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | No |
| USRP-2943 | 1.2 GHz - 6 GHz | 40 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | No |
| USRP-2943 | 1.2 GHz – 6 GHz | 120 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | No |
| USRP-2944 | 10 MHz - 6 GHz | 160 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | No |
| USRP-2945 | 10 MHz - 6 GHz | 80 MHz | Kintex-7 410T | 4 | 0 | MXIe Ethernet | No |
| USRP-2950 | 50 MHz - 2.2 GHz | 40 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | Yes |
| USRP-2950 | 50 MHz - 2.2 GHz | 120 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | Yes |
| USRP-2952 | 400 MHz - 4.4 GHz | 40 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | Yes |
| USRP-2952 | 400 MHz - 4.4 GHz | 120 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | Yes |
| USRP-2953 | 1.2 GHz - 6 GHz | 40 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | Yes |
| USRP-2953 | 1.2 GHz - 6 GHz | 120 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | Yes |
| USRP-2954 | 10 MHz - 6 GHz | 160 MHz | Kintex-7 410T | 2 | 2 | MXIe Ethernet | Yes |
| USRP-2955 | 10 MHz - 6 GHz | 80 MHz | Kintex-7 410T | 4 | 0 | MXIe Ethernet | Yes |

Table 4.5: List of alternative Software defined radios offered by National Instruments

4.3 LTE Application Framework

LTE Application Framework is a Software that National Instruments designed and offers to provides us a *Downlink ONLY* 2x2 LTE setup. This setup does not require the additional hardware which are required for the functioning of the MIMO AFW.

4.3.1 Hardware Requirements

This setup is quite a simplified version of the MIMO AFW and only requires a pair of USRPs (4.1), a pair of the PCIe daughter cards(4.1.1) and a host PC(4.1.2). One USRP acts as a eNodeB with 2 antennas (Base Station) and the other USRP acts as a UE with 2 antennas.

4.3.2 Software Requirements

The LTE AFW Software template that NI provides in its example libraries only has a LTE SISO implementation. But an internal development version of a 2x2 MIMO Extension was issued to TUM for the sake of expediting the experimental setup since MIMO AFW was not a financial viable option. However the NI internal development version of the code was meant to be run on a version 2.1 of Labview Communication Suite which is not supported on Windows 10. Hence the project had to be ported to the latest version of Labview Communications Suite (now called Labview NXG). Details of the software project are described in Chapter 5

4.3.3 Implementation Advantages and Disadvantages

The advantages of using LTE AFW is that it works with minimum hardware, albeit with a limited capability of providing only a 2x2 MIMO system. Unlike MIMO AFW which is capable of bidirectional MIMO communications, LTE AFW can only perform unidirectional communications, namely from the eNodeB(Base station) to the UE. However given all the time and budget constraints, LTE AFW was chosen as the preferred solution. The architecture of the software and the modifications are explained in the following chapter.

Experimental Setup 5

Chapter 4 discussed the possible options to implement a MIMO setup. The first option (section 4.1) was not viable due to technical limitations as it is described in Appendix A.2.

The second option (section 4.2) was financially unfeasible as the additional hardware for the modular MIMO set was to cost over €80.000.

The only viable option was to use the LTE AFW with a MIMO Extension, although limited to a 2x2 MIMO system, was sufficient in this case.

5.1 LTE Application Framework MIMO Extension

LTE AFW is a SISO LTE Release 10 implementation, where as LTE AFW 2x2 MIMO Extension was developed internally by NI as a plugin to the SISO framework. This software is not readily available for customers to purchase, but it was given to MSV as a workaround for the MIMO implementation.

For the implementation of the LTE AFW MIMO Extension as outlined in Chapter 4.3 the equipment required is minimal. A set of 2 USRPs, one acting as a UE (Receiver) and the other acting as a Base Station (eNodeB) completes the transmitter chain and Host PC does the graphing and data visualisation and device setup. The part numbers are described in section 4.3.1. Below is an illustration of the simple HW connections required to make the device communicate with the host.

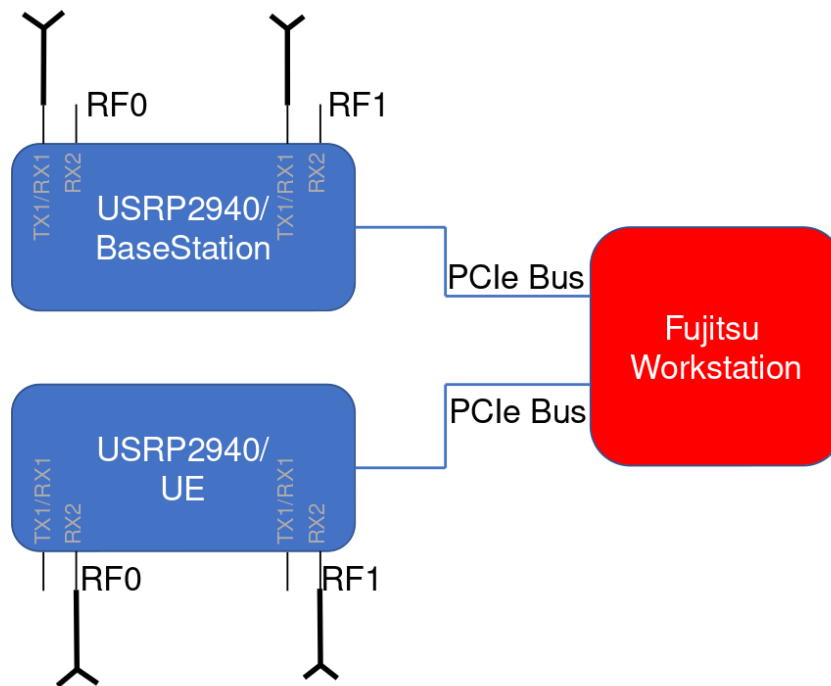


Figure 5.1: Overview of the LTE 2x2 MIMO HW connection setup

5.1.1 LTE AFW MIMO Externsion Architecture

Placeholder

5.1.2 LTE AFW Host Software

5.1.3 LTE AFW FPGA

LTE has demanding and resource intensive processing requirements. LTE AFW aims to

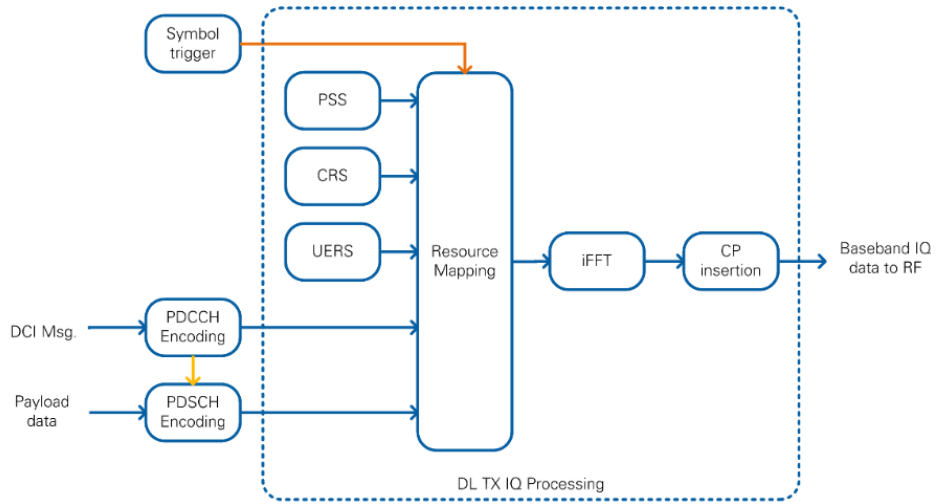


Figure 5.2: Simplified implementation of the DL TX processing block of the FPGA

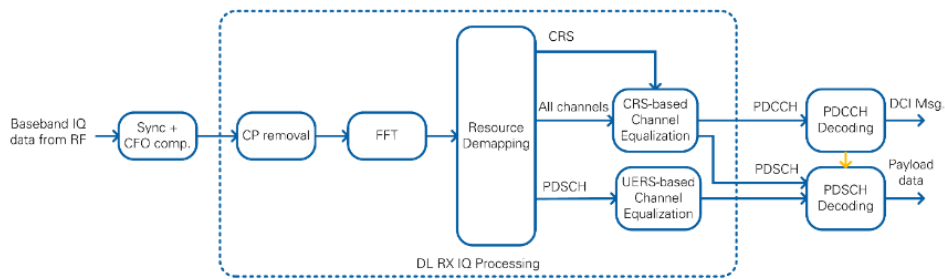


Figure 5.3: Simplified implementation of the DL RX processing block of the FPGA

5.2 Application Example

Results 6

Over the course of the internship many different parameters had to be determined and set up for the final demo. This chapters documents the results of all the experiments performed as well as the final demo of the working setup.

6.1 Data Loss

Following the data transmission through over the air using LTE AFW, benchmarks were run to check the loss of data over the wireless medium. Tests were run using *iperf* version 2.0.9.

Conclusion and Outlook 7

7.1 FPGA File Port

7.2 Experiment with structured Channel

Troubleshooting

A.1 Boot Order

The communications protocols between the USRP and the host follows the PCIe standard. It is essential that the drivers are loaded in during boot up. It is highly advised against hot swapping or unplugging PCIe cables while the host is booted up and running. Secondly care must be taken while booting up the system by following the sequence recommended by NI in order to avoid synchronisation issues.

1. Connect the PCIe cables from the PCIe port of the USRPs to the PCIe cards mounted on the Host (section 4.1.1)
2. Power up the USRPs once the above step has been completed
3. Power up the PC and wait for the device to boot up
4. Check the NI MAX (NI's software for managing NI devices) Software to see if the devices have been recognised by the PC
5. When all the USRPs appear on the NI MAX they are ready to be used

A.2 Synchronisation of the USRPs

USRPs are complex devices which combine analog transceivers and digital Xilinx Kintex-7 FPGA, which does all the compute intensive tasks. Figure A.2 shows a block diagram of a **single** RF channel with the internal components of the USRP. There are two such channels in a given USRP 2940.

The figure shows that a single RF channel can be used either as a single antenna transmitter (**TX1**) or a single antenna receiver (**RX1/RX2**). RX1 and RX2 **cannot** be used simultaneously.

The 2 radio channels within a USRP are either synchronised using the REF IN signal which is a 10 MHz supplied by an external clock distributor (section 4.2.3) or by using the internal 10MHz oscillator. They share the same reference clock for all the

PLLs and the VCOs as illustrated in figure A.2. It was inferred from tests that the RF path delay for the Low Noise Amplifiers (LNA) are not matched between the channels in the USRP and therefore leading to phase shifts between the 2 RF channels on the single USRP. This results in unsynchronous transmit and receive data between the channels which is not the preferred mode of operation for a MIMO setup as receive and transmit synchronisation is key. Furthermore the delay is not a constant for every new run of the system, rather its a new delay for every rerun. This is the limitation of the hardware and caused by delays in the RF analog path. The delay does remain constant within the duration of a run.

The Octoclock provides a common 10 MHz sampling clock which all the USRPs synchronize to. The Octoclock also has a PPS Trigger which is a pulse per second trigger which is used as a sampling trigger for different USRPs.

Figure 3. Synchronizing Multiple USRP RIO Devices with the CDA-2990

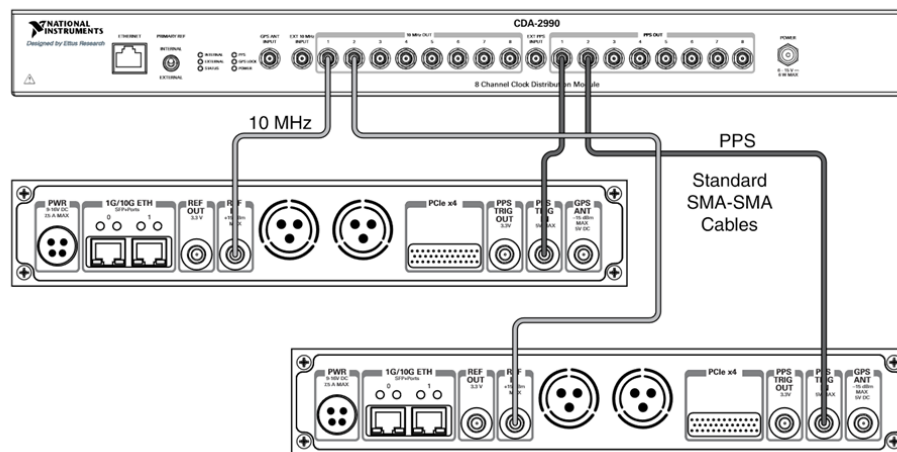


Figure A.1: The connections from the Octoclock to the USRP

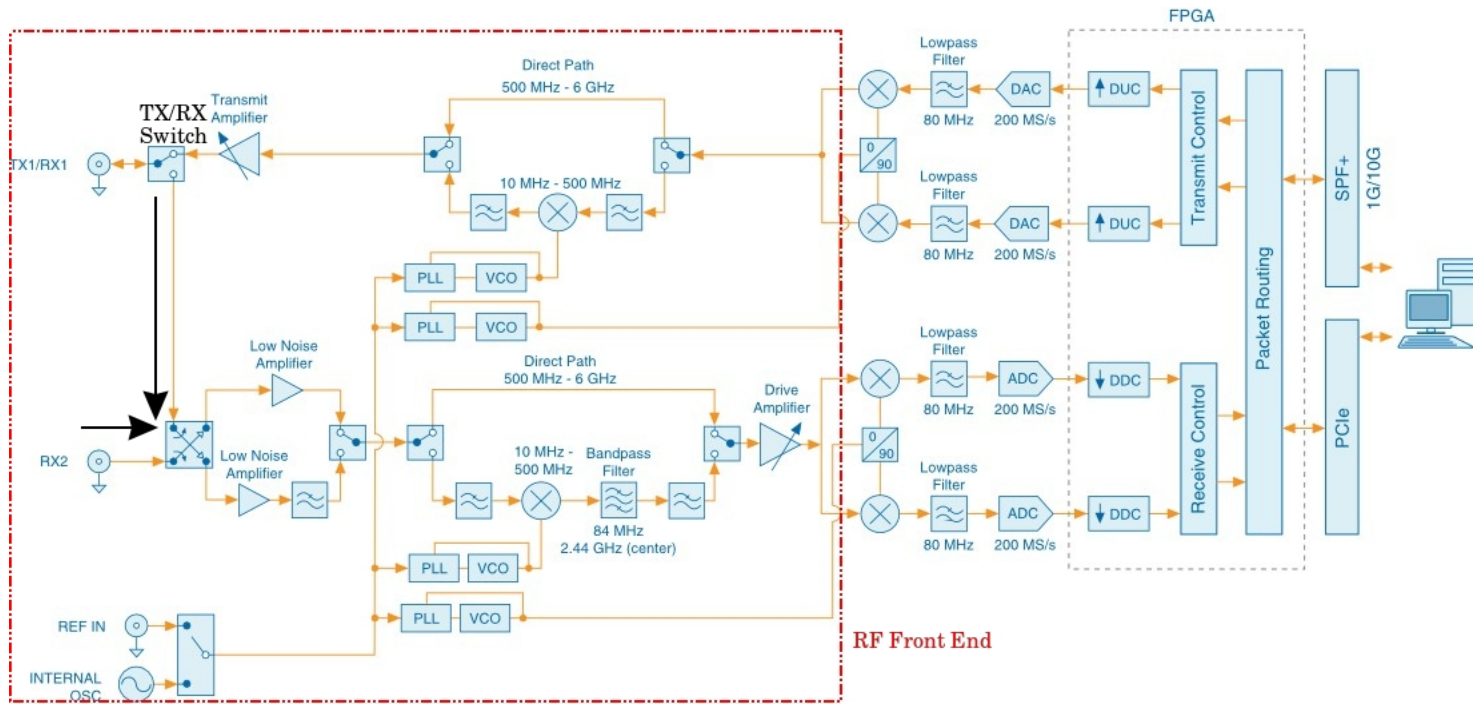


Figure A.2: USRP 2940 Internal Components

Appendix A. Troubleshooting

The following section describes the test setup used to verify the functional specification of the Octoclock. Figure A.3 show the REF IN coming in from 2 different ports of the octoclock each terminated with a 50 Ohm resistor and measured with an oscilloscope. The experiment was carried out to verify the synchronicity of the reference clocks from two different ports of the octoclock. The FFT of the signal also shows that the tone lies at 10 MHz.



Figure A.3: The 10 MHz REF IN clock as seen at the output of two respective channels of the Octoclock. The yellow is from ch1 and the green is from channel 2 which are connected to USRP1 and USRP2 respectively. The top half is the Fourier transform and the bottom half is the time domain signal

Figures A.4 and A.5 show 2 PPS (Pulse per Second) triggers received from 2 ports of the octoclock each terminated with a 50 Ohm resistor and measured using an oscilloscope. The signals found to be aligned and have a rising edge every second as we expect.

It can be inferred from the design of the Octoclock B that the REF IN is internally generated by the Octoclock and distributed among all the ports. Alternatively there is an option to feed the an external reference input to the octoclock and distribute this reference among the other ports.

A.2 Synchronisation of the USRPs



Figure A.4: Figure shows a zoomed-out view of the PPS Trig Out which occurs every 1s and the high pulse is 200ms long.

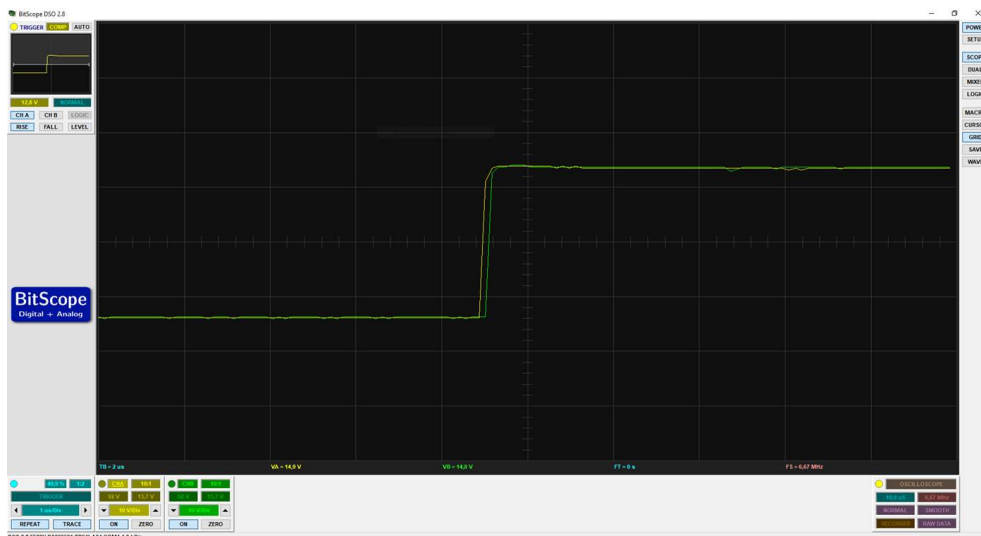


Figure A.5: Figure shows the PPS trigger signal from the Octoclock. The slight shift is potentially an artifact from the measurement instrument as the bandwidth of the measurement tool was limited (20MHz).

Finally after verifying the Octoclock functionality, a test was devised to measure

Appendix A. Troubleshooting

the synchronicity of the Tranceiver. For this 2 USRP devices were connected as shown in A.1 and tests were run in loopback mode where the TX1 of each RF channel was connected to the respective RX2 of the same RF channel. A pure tone is sent as IQ samples from each TX1 port of each USRP 1 and USRP 2. This test was conducted by using 1m 50 Ohm cables to eliminate the air interface. Matched length cables avoid phase delays and are critical in this measurements.

The function sent at the transmitter side is described as follows

$$y(t) = \cos(\omega t) + j * \sin(\omega t) \quad (\text{A.1})$$

where the I Signal is $\cos(\omega t)$ and the Q Signal is $\sin(\omega t)$.

Ideally the same signal should be received on all RX ports, where as the signals are received with a relative random phase shift. Figure A.6 below shows the results of the tests showing the phase difference when one USRP transmits the same sine tone on the 2 respective TX1 channels of the 2 USRPs, while the signals are received on the respective RX2 channels of each RF channel.

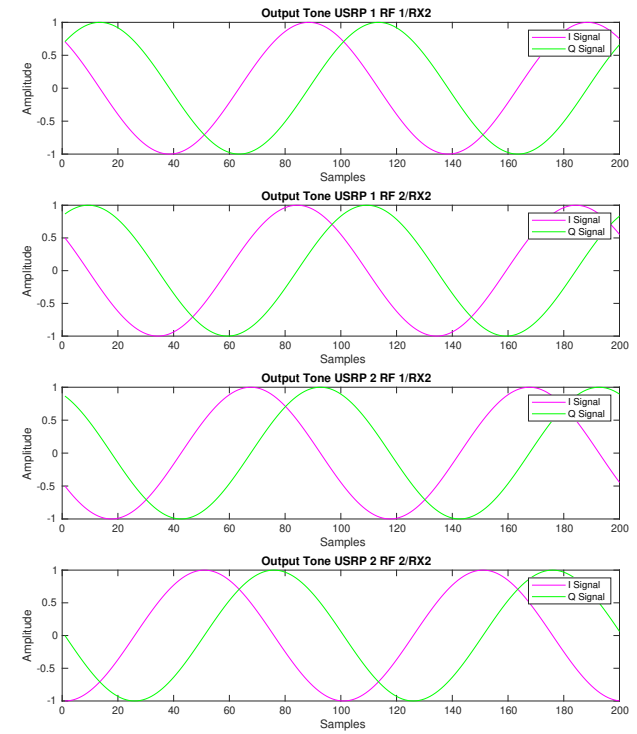
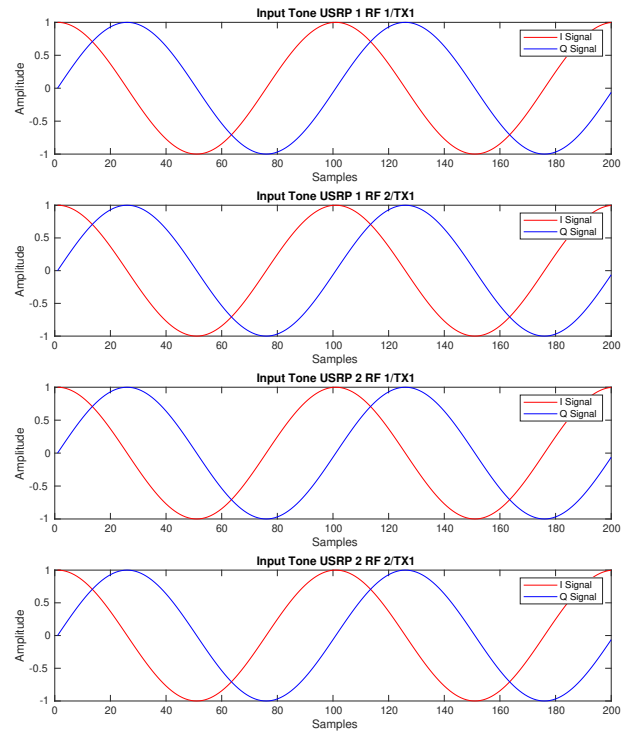


Figure A.6: The left waveforms are the TX waveforms and the right waveforms are the RX waveforms. It can be seen that the received IQ waveforms are unsynchronised and clearly have a phase shift

Schematic Octoclock B

Front Panel

8x 10 MHz out

8x PPS out

GPS In

10 MHz In

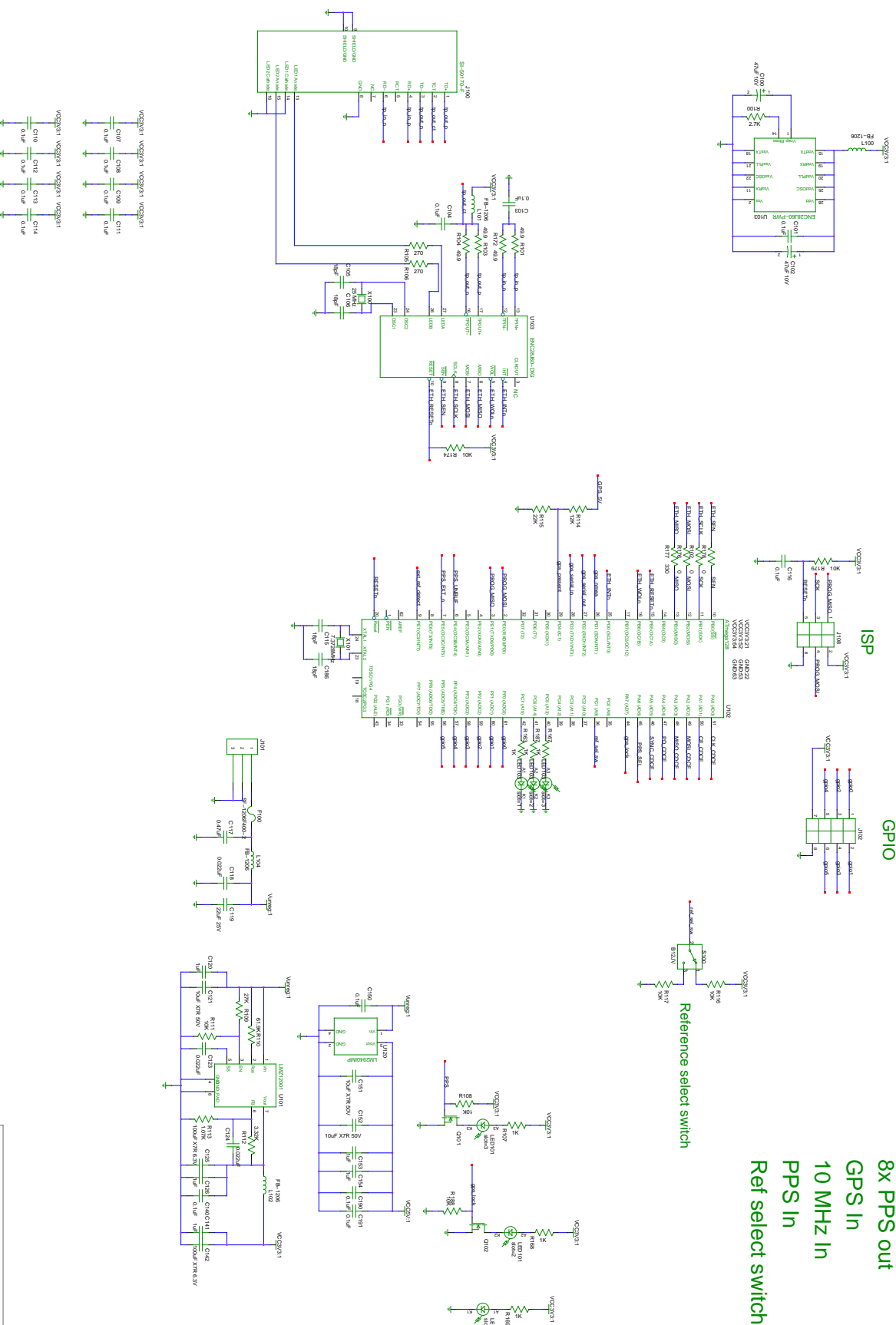
PPS In

Ref select switch

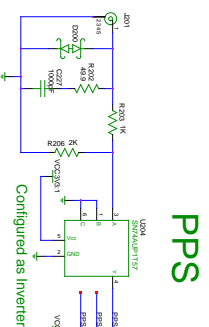
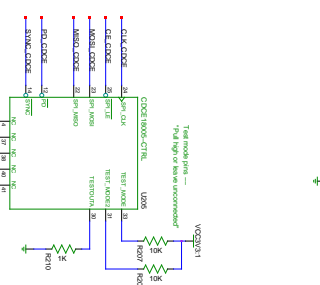
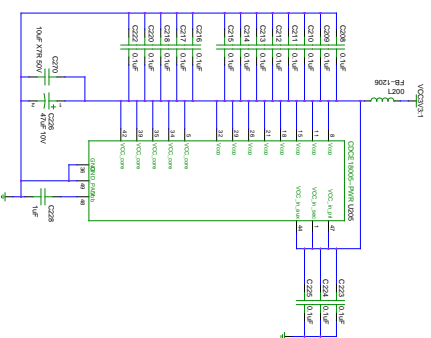
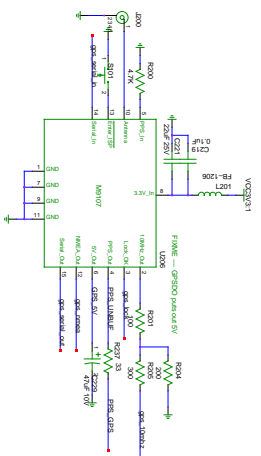
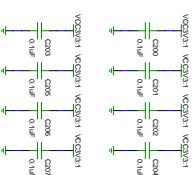
ISP

GPIO

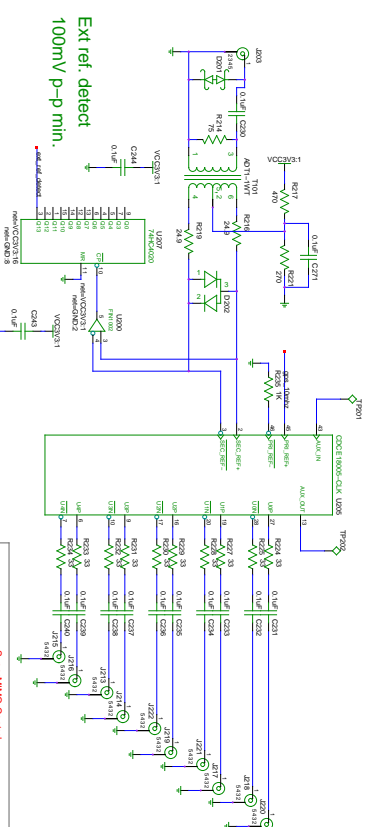
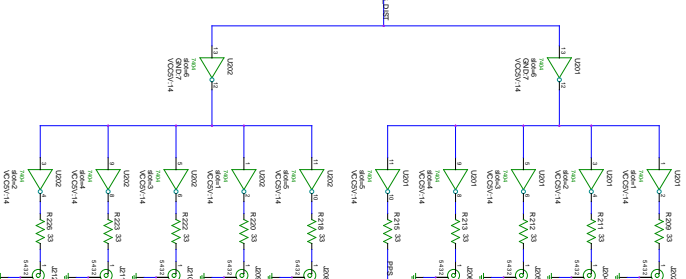
Reference select switch



Front Panel
8x 10 MHz out
8x PPS out
RS232 out
GPS In
10 MHz In
PPS In



PPS
Configured as Inverter



Ext ref. detect
100mV p-p min.

SuperMINI0 Config

| TITLE | |
|------------|------------|
| SuperMINI0 | 1.0 |
| DATE | 10/10/2010 |

Bibliography

- [1] W. Utschick, “Anwendungen in der Informationstechnik – Grundlagen der Mehrfachzugriffsverfahren I und II.”
- [2] H. Rohling, *OFDM - Concepts for Future Communication Systems*, 3rd ed. Springer, Jun. 2011.
- [3] 3GPP, “TS 36.211 Technical Specification Group Radio Access Network; Physical Channels and Modulation (Release 13), V13.2.0,” vol. 13, Jun. 2016.
- [4] K. Fazel and S. Kaiser, *Multi-Carrier and Spread Spectrum Systems*, 2nd ed. Wiley, Jun. 2008.
- [5] R. M. Gray, “Toeplitz and Circulant Matrices: A review,” Department of Electrical Engineering, Stanford University, Stanford 94305, USA, Tech. Rep.
- [6] *MIMO Prototyping System Getting Started Guide*, 2016.