U –54382

Register No. | | | | | | | | |

BE Degree Examination November 2019

Third Semester

Computer Science and Engineering

18CST32 – COMPUTER ORGANIZATION

(Regulations 2018)

Common to BTech Information Technology

Time: Three hours | Maximum: 100 marks

Answer all Questions

Part – A (10 × 2 = 20 marks)

1. Name the four commonly used condition code flags in a processor. [CO1,K1]

2. Consider a processor with an instruction of type LOAD R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Identify the addressing mode implemented by this instruction for fetching the operand in memory. [CO1,K3]

3. Mention the two attractive features of Booth algorithm. [CO2,K1]

4. Using Booth algorithm for multiplication, how the multiplier -57 is recoded? [CO2,K3]

5. Define pipelining. [CO3,K1]

6. "Hardwired control unit is slower than micro-programmed control unit". Justify this statement. [CO3,K2]

7. Define hit rate and miss rate. [CO4,K1]

8. How many 32K × 1 RAM chips are needed to provide a memory capacity of 256 K bytes? [CO4,K3]

9. List any two functions of an I/O interface. [CO5,K1]

10. Consider the following program segment [CO5,K3]

Instruction	Instruction size (in words)
Mov R1, 5000	2
Mov R2,(R1)	1
ADD R2,R3	1
Mov 6000, R2	2
HALT	1

Assume that the memory is byte addressable with 32 bits. The program has been loaded starting from memory location 1000 (decimal). If an interrupt occur while the CPU has been halted after executing HALT instruction, what is the return address saved in the stack?

Part – B (5 × 16 = 80 marks)

11. a. i) Convert the following pairs of decimal numbers to 5-bit 2's complement numbers, then perform addition and subtraction operation. Indicate whether overflow occur in each case or not. (8) [CO1,K3]

1) 9 and 8 2) -12 and 6

ii) Write a RISC-style and CISC-style program that computes the expression (8) [CO1,K3]

$x = a + b - c * (d / e) + f$

(OR)

b. Summarize the basic addressing modes found in RISC-style processors with an example. Also find the addressing mode and effective address (EA) in each case. (16) [CO1,K3]

i) 16(R1,R2)

ii) (R1)+

iii) –(R2)

iv) 12(PC) (Assume the content currently in PC is 8000)

Assume that the registers R1 and R2 contain the decimal numbers 5000 and 3000 respectively.

12. a. Multiply the following pair of signed 2's complement numbers by using booth algorithm and bit-pair recoding of multipliers. (16) [CO2,K3]

A = 110111 and B = 010011

Assume that A is the multiplicand and B is the multiplier.

(OR)

b. i) Perform A ÷ B on the 5-bit unsigned numbers A = 11011 and B = 00101 using restoring division algorithm. (8) [CO2,K3]

ii) Consider a 12-bit floating – point number with a 5-bit exponent and a 6-bit mantissa fraction which has an implied 1 to the left of the binary point. The base of the scale factor is 2 and the exponent is represented in excess 15 format. Perform subtract and multiply operations on the operands. (8) [CO2,K3]

A=	0	10001	010111

B=	1	01111	101101

Give the answer in the normalized form. Use rounding as the truncation method for producing the final mantissa.

13. a. i) At the time the instruction (8) [CO3,K3]

ADD R1, 100(R2)

is fetched, register R1 contain the decimal value 98 and register R2 contain the value 6600. Memory location 6700 contains the decimal value 118. Show the contents of the interstage registers in datapath of a processor during each of the 5 execution steps of this instruction.

ii) Elaborate with necessary block diagram how hardwired control approach generates the control signals for fetching and executing the instructions in the correct sequence and at the right time. (8) [CO3,K2]

(OR)

b. i) Consider a 5 stage pipelined processor, IF(Instruction Fetch), ID(Instruction Decode and Register read), MA(Data Memory Access-for write access, the register read at ID stage is used) and WB(Write Back). Consider the execution of the following instruction sequence. (8) [CO3,K3]

I_1 : LOAD R0, LOC1

I_2 : ADD R0, R0

I_3 : SUB R1, R0

Draw a pipeline diagram that represents the flow of the instructions through the five-stage pipeline for the given cases.

1) Allowing operand forwarding from memory stage
2) Not allowing operand forwarding from memory stage.

ii) Summarize the different methods for branch prediction and state how better prediction accuracy can be achieved by 4-state dynamic prediction algorithm compared to that of the 2-state dynamic prediction algorithm. (8) [CO3,K2]

14. a. i) Elaborate with neat sketch, how virtual addresses are translated into a physical addresses using virtual memory address translation method. Also, state the role of associative – mapped TLB in efficient address translation. (8) [CO4,K2]

ii) Design the structure of $4M \times 32$ memory module using $512\,K \times 8$ static memory chips and identify the number of address bits that are needed to select a 32-bit word in this memory. (8) [CO4,K3]

(OR)

b. i) Classify the types of ROM and highlight their features in detail. (8) [CO4,K2]

ii) A computer system has a 32 MB main memory and 64 KB cache. Block size is 256 bytes and number of blocks per set is 4. (8) [CO4,K3]

1) How many bits are there in main memory?
2) How many bits are there in each of the TAG, SET, BLOCK and WORD fields for direct mapping, associative mapping and set-associative mapping?

15. a. i) Write the sequence of events involved in handling an interrupt request from a single device. (8) [CO5,K1]

ii) Assume the numbers of devices connected to the processor are capable of initiating interrupts simultaneously. Provide the various approaches in handling the interrupts from multiple devices. (8) [CO5,K2]

(OR)

b. i) Recall the concept of handshake protocol for controlling data transfers between the master and slave in asynchronous bus with timing diagram. (8) [CO5,K1]

ii) Elaborate USB architecture with neat sketch. Write the key objectives of USB and state how the user convenience can be enhanced through a "plug-and-play" mode of operation. (8) [CO5,K2]

Bloom's Taxonomy Level	Remembering (K1)	Understanding (K2)	Applying (K3)	Analysing (K4)	Evaluating (K5)	Creating (K6)
Percentage	14.4	27.8	57.8	-	-	-