N–11662

Register No. | | | | | | | | |

BE Degree Examination November 2015

Third Semester

Computer Science and Engineering

14CST33 – COMPUTER ORGANIZATION

(Regulations 2014)

Common to BTech Information Technology

Time: Three hours Maximum: 100 marks

Answer all Questions

Part – A (10 × 2 = 20 marks)

1. Assume a program consists of 200 machine language instructions. The average number of basic steps required to execute one machine instruction is 2, where each basic step is completed in one clock cycle. Find the processor time required to execute a given program, if the clock rate is 20 cycle/sec.
2. What are condition code flags? Name the commonly used flags.
3. Mention the characteristics of Booth algorithm.
4. Write the multipliction rule for floating point numbers.
5. What is speculative execution?
6. When A=5

   A=3+A

   B=4*A

   What hazard does the above two instructions create when executed concurrently?
7. Differentiate DRAM and SRAM.
8. Define hit rate and miss penalty.
9. How does a processor handle the interrupt request?
10. What are the components of I/O interface?

Part – B (5 × 13 = 65 marks)

11. a. Calculate effective address for the following instructions (13)
    1) LOAD 20(R1), R5
    2) MOVE#3000, R5
    3) Store R5, 30 (R1, R2)
    4) Add – (R2), R5
    5) SUB (R1) + R5
    6) Store R1, 45 (R5, R2) where R1=1200 and R2=4600.

(OR)

b. i) Compare and contrast the features of RISC and CISC Processor. Which one is more preferable with respect to the performance of the processor? (5)

ii) Illustrate the methods to calculate effective address in various addressing modes. (8)

12. a. i) Apply booth algorithm to perform multiplication of the following two numbers with the flow table. (8)

Multiplicand = 110011

Multiplier = 101100.

ii) Implement the logic design for fast adders. Comment on the various approaches taken to reduce delay in adders. (5)

(OR)

b. Explain the restoring and non-restoring division algorithms. Perform the non-restoring division on the following 5-bit unsigned integers : 10101/00101. (13)

13. a. i) Consider a processor is having single bus organization of the data path. Write the sequence of control steps required for each of the following instructions : (8)

1) Add the (immediate) number NUM to register R1

2) Add the contents of the memory location whose address is at memory location NUM in register R1.

ii) Use operand forward technique to overcome data dependency problem in a pipelined processor. (5)

(OR)

b. i) Justify the statement using superscalar operation 'Out of order execution does not affect in order dispatch". (5)

ii) Illustrate delayed branching with an example. What other techniques can be used to reduce branch penalty associated with conditional branches? (8)

14. a. Suppose physical addresses are 32 bit wide. Suppose there is a cache containing 256K words of data (not including tag bits), and each cache block contains 4 words. For each of the following cache configurations,

i) direct mapped (3)

ii) 2-way set associative (3)

iii) 4-way set associative (3)

iv) fully associative (4)

specify how the 32-bit address would be partitioned. For example, for a direct mapped cache, you would need to specify which bits are used to select the cache entry and which bits are used to compare against the tag stored in the cache entry.

(OR)

b. Write about the address translation mechanism used in the virtual memory for translating virtual address into physical address. Discuss the role of TLB. (13)

15. a. i) Explain the SCSI bus interface standards. (6)

ii) Why is priority handling desired in interrupt controllers? How do the different priority schemes work? (7)

(OR)

b. i) With neat block diagram explain DMA technique for data transfer with the working of a DMA controller. Specify its advantages and disadvantages. (9)

ii) Illustrate the handshake control of data transfer in asynchronous bus. (4)

Part – C ($1 \times 15 = 15$ marks)

16. a. i) Calculate the number of bits required in each entry of a TLB that has the following characteristics : (7)

1) Virtual addresses are 32 bits wide

2) Physical addresses are 31 bits wide

3) The page size is 2K bytes

4) The TLB contains 16 entries of the page table

5) The TLB is direct-mapped.

ii) Sketch the structure of semiconductor RAM memories. Elaborate the read and write operations of RAMs. (8)

(OR)

b. Write the control sequence for the execution of Instruction Add (R3), (R1). Construct a hardwired control unit to generate control signal for the execution of above control signals. (15)