F–14392

Register No. | | | | | | | | |

BE Degree Examination November 2016

Third Semester

Computer Science and Engineering

14CST34 – DIGITAL LOGIC AND VERILOG PROGRAMMING

(Regulations 2014)

Time: Three hours Maximum: 100 marks

Answer all Questions

Part – A (10 × 2 = 20 marks)

1. Convert the decimal 255 to binary and then to hexadecimal.
2. Simplify the Boolean function $F = (x + x')y$,
3. Find the minimal SOP expression for $Y = A'C + A'B + AB'C + BC$.
4. Give the general procedure for converting a Boolean expression into multilevel NAND diagram.
5. Write the design procedure for combinational circuits.
6. Differentiate between a combinational logic circuit and sequential logic circuit.
7. Write the VHDL coding for a sequential statement (d-flip-flop) entity.
8. Which flip flop is used as a latch? Why?
9. What is programmable logic array? How it differs from ROM?
10. List the major differences between PLA and PAL.

Part – B (5 × 13 = 65 marks)

11. a. i) Prove that $ABC + ABC' + AB'C + A'BC = AB + AC + BC$ and using 10's complement subtract 72532 – 3250. (7)

ii) Convert following hexadecimal number to decimal number (6)

1) $F28_{16}$

2) $BC2_{16}$

(OR)

b. i) Find the complement of the functions $F1 = x'yz' + x'y'z$ and $F2 = x(y'z' + yz)$ by applying De-Morgan's theorem. (7)

ii) Summarize the basic properties of Boolean algebra. (6)

12. a. Reduce the Boolean function using k-map technique and implement using gates which has the don't cares condition $f(w,x,y,z) = \Sigma m(0,1,4,8,9,10)$ $d(w,x,y,z) = m(2,11)$. (13)

(OR)

b. Interpret the given Boolean function $F(A,B,C,D) = \Sigma M(0,1,2,5,8,9,10)$ into (13)

i) Sum of Products form

ii) Product of Sum form and implement it using basic gates.

13. a. i) Design a 4-bit decimal adder using 4-bit binary adders. (7)

ii) Implement the function $F = \Sigma(0,1,3,4,8,9,15)$ using multiplexer. (6)

(OR)

b. i) Conclude that the carry look ahead adder is faster than a ripple carry adder by using necessary equations. (7)

ii) Write an HDL data flow description of a 4 bit adder of unsigned numbers. (6)

14. a. i) Compare the diagram of 4-bit SISO SIPO, PIPO and PISO shift registers and draw its waveforms. (7)

ii) Realize D flip-flop using SR flip-flop. (6)

(OR)

b. i) Construct and explain the working of an 4-bit Up/Down ripple counter. (7)

ii) Model a synchronous MOD-5 counter and explain with waveforms. (6)

15. a. Design a combinational circuit using a ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. (13)

(OR)

b. i) Interpret how does programmable logic devices differ from SPLD. Give an example. (7)

ii) Formulate the implementation of the following functions with PLA having three inputs, four product terms, and two outputs. (6)

$F1(A,B,C) = (3,5,6,7)$

$F2(A,B,C) = (0,2,4,7)$.

Part – C $(1 \times 15 = 15$ marks)

16. a. Create the design of a BCD to seven segment decoder with neat diagrams. (15)

(OR)

b. Explain the functions with the state diagram and characteristics equation of T, D and JK flip flops and compare and contrast among the FFs. (15)