F–14381

Register No. | | | | | | | | |

BE Degree Examination November 2016

Third Semester

Computer Science and Engineering

14CST33 – COMPUTER ORGANIZATION

(Regulations 2014)

Common to BTech Information Technology

Time: Three hours Maximum: 100 marks

Answer all Questions

Part – A (10 × 2 = 20 marks)

1. What are the functional units of a computer system?
2. Evaluate (A+B)*(C+D) using one address instruction.
3. State the two attractive features of Booth algorithm.
4. Identify the methods for truncating guard bits in extended mantissa.
5. Outline the structure of 4-stage pipeline.
6. Assume there is single bus architecture. What is the control sequence for the execution of the instruction ADD R1, R2 including the instruction fetch phase?
7. Classify the types of ROM.
8. Differentiate write-through and write-back mechanism in cache memory.
9. When a processor is executing an interrupt service routine for one device, can other device interrupt the processor?
10. List the various types of bus standard I/O interfaces.

Part – B (5 × 13 = 65 marks)

11. a. i) Explain the block diagram of connections between the processor and memory, and explain how the following typical instructions can be executed with relevant steps. (8)
    - MOV NUM1, R2
    - ADD R3, NUM2

    ii) Write a set of instructions that can evaluate the following expression (5)
    $S = ((A + B)/(C * D)) + E$ using three address and two-address instructions types.

    (OR)

    b. i) Identify the addressing modes supported by a typical processor. With suitable examples given a brief note on any three of them. Also, identify the addressing mode and effective address of the memory opened in each of the following instruction (13)

    1) Load 40(R1), R7
    2) Move R2, 40(R1,R2)
    3) Add (R2)+ R3
    4) Sub –(R1), R3.

    Assume that resister R1, R2 and R3 contain the values 1000, 1100 and 1200 respectively.

12. a. i) List the different systems used to represent a signed number and give one example for each. Specify which number system is preferred in a computer and why? (6)

ii) Give A = 10101 and B = 00100 perform A/B using restoring division algorithm and find quotient and reminder. (7)

(OR)

b. Multiply $(A \times B)$ the following pair of numbers using Booth algorithm. (13)

$A = -15$ and $B = -7$.

Repeat the above multiplication using bit-pairing of the multiplication and verify the result.

13. a. i) How does multi-bus organization help in reducing the number of control steps needed for executing an instruction? Illustrate with a suitable sketch. Also write the control sequences for the instruction Add R1, R2, R3 with three-bus organization. (6)

ii) Draw the organization of hardwired control unit. How does hardwired control unit determine the required control signals? (7)

(OR)

b. Identify the type of hazard present in the following instruction if they are executed using pipelined processor. (13)

Add R2, R1

Sub R1, R3

Examine in detail the approaches to overcome the hazard with neat sketches.

14. a. i) Explain how the virtual address is converted into physical address using virtual-memory address translation. (8)

ii) Memory interleaving in a design technique that increase the performance without increasing the cost. Justify the statement with appropriate diagram. (5)

(OR)

b. Determine the methods for specifying where the main memory blocks are placed in the cache memory. Outline the idea behind each method. A computer system has a main memory consisting of 4096 blocks with 64 words in each block. It also has a 256 block cache with 64 words in each cache block. Apply all the mapping techniques and show how main memory address to cache memory address is mapped in all the methods. Assume that a set contains four blocks. (13)

15. a. i) Discuss the main phases involved in the operation of SCSI bus in detail with an example. (8)

ii) Enumerate the important functions of an I/O interface. (5)

(OR)

b. i) How does USB support the plugging of multiple I/O devices? Illustrate with USB the structure. (6)

ii) What is DMA? Explain the registers that are required in DMA controller chip. (7)

Part – C (1 × 15 = 15 marks)

16. a. Write the rules to add, subtract, multiply and divide two floating point members. perform addition on the following operations (15)

A=	0	10001	011011
B=	1	01111	101010

(OR)

b. i) Design a RAM chip of 16×8 organization with all necessary connection for address, data and control line. How many such RAM chips are needed to design a RAM memory of size $1MB \times 8$. (8)

ii) Why is special handling required for branch instruction in a pipelined processor? Explain with examples. (7)