N–11672

Register No. | | | | | | | | |

BE Degree Examination November 2015

Third Semester

Computer Science and Engineering

14CST34 – DIGITAL LOGIC AND VERILOG PROGRAMMING

(Regulations 2014)

Time: Three hours Maximum: 100 marks

Answer all Questions

Part – A (10 × 2 = 20 marks)

1. Determine the ones and twos complement of "11101110".
2. Simplify the expression $Y = A'B'C' + A'BC' + AB'C' + ABC'$ using Boolean laws.
3. Draw the Ex-OR gate with truth table.
4. Discover a OR gate using NAND gates.
5. Tell about data flow modeling in HDL.
6. Sketch a 4 input priority encoder.
7. Differentiate a latch and flip flop.
8. List the two keywords used in behavioural model with an appropriate example.
9. Classify the types of ROM.
10. Write the basic syntax for loop statement in HDL.

Part – B (5 × 13 = 65 marks)

11. a. i) Transform the following from one number system to the other as per the given in base. (8)

$(A3B)_{16} = (?)_{10}$, $(F3)_{16} == (?)_{10}$, $(111111011)_2 = (?)_{16}$, $(12456)_{10} = (?)_8$.

ii) Enumerate the basic properties of Boolean algebra. (5)

(OR)

b. Summarize the basic Boolean laws and theorems. (13)

12. a. Determine the Prime implicates of the following function using suitable K-map reduction technique. $F(w,x,y,z) = \sum m(0,2,3,6,7,8,10,12,13)$. (13)

(OR)

b. i) Simplify the following Boolean expression using four variable map (8)
$y = AB'C + B'CD' + BCD + ACD' + A'B'C + A'BC'D$.

ii) Which gates are called are called as "Universal gates"?Why? Tabulate the truth table for such gates. (5)

13. a. i) Explain the gate-level modeling of a full adder. (8)

ii) Using a suitable example, discuss the concept of gate level modeling in HDL. (5)

(OR)

b. Using decoder and external gates design a combinational circuit defined by the following Boolean function. (13)

$F1 = X'Y'Z' + XZ$

$F2 = XY'Z' + X'Y$

$F3 = X'Y'Z + XY$.

14. a. Using JK Flip-flop design a synchronous counter which counts in the sequence 000, 111, 101, 110, 001, 010, 000. (13)

(OR)

b. Design a sequential circuit with two D-Flip-flops A and B and one input x. (13)

i) When $x = 0$, the state of the circuit remains the same, when $x = 1$ the circuit goes through the state transitions from 00 to 01 to 11, to 10 and back to 00 and repeats.

ii) When $x = 0$, the state of the circuit remains the same, when $x = 1$ the circuit goes through the state transitions from 00 to 11, to 01, to 10 and back to 00 and repeats.

15. a. i) Interpret a verilog HDL code to perform read and write operations of memory. (8)

ii) Using suitable example, construct AND-OR PLA. (5)

(OR)

b. With an example illustrate the working principle of Hamming code. (13)

Part – C ($1 \times 15 = 15$ marks)

16. a. i) With neat diagram explain the operation of master slave flip flop configuration. (10)

ii) Compare combinational logic and sequential logic circuits. (5)

(OR)

b. i) Construct of 3 bit magnitude comparator. (10)

ii) Compare synchronous and asynchronous counters. (5)