WEEK 0 vedio Summary

SoC Development Flow

1.Specification (C Model)

Start with system requirements written in C language (functional model).

Testbench also in C to check if the algorithm works correctly.

This is the *chip modeling* stage.

2.RTL Design (Soft Copy of Hardware)

Convert the specification into RTL (Verilog/VHDL).

This design includes Processor core (control) and Peripherals/IPs (UART, SPI, GPIO, etc.). At this stage, hardware is still *virtual/soft*.

3.Synthesis

RTL is converted to gate-level netlist using libraries.

Generate macros (synthesized blocks).

Analog IPs are used directly (pre-designed, functional models).

4.SoC Integration

Combine processor, peripherals, macros, and analog Ips.

Connect via buses and GPIOs.

Verify integration through simulation.

5.Back-End (RTL → GDS)

Physical design: floorplanning, placement, clock tree synthesis, routing.

Add hardened macros and analog IPs into layout.

Processor can be soft logic or hard macro depending on design.

6.Final Steps

Perform sign-off checks: DRC (Design Rule Check), LVS (Layout vs Schematic).

Generate GDSII file → the final mask data sent for fabrication.

Microcontroller ;

It is a small SoC combining processor + peripherals.

It operates at modest frequencies 100 MHz – 130 MHz.

Testbench and programming often start in C language.

Applications of Microcontroller are

Smart wearables (iWatch, fitness bands).

Arduino boards .

TV panels (other than wifi may be display).

AC for control.