Impact of Channel Length, Oxide Layer Height, and Electrode Work Function on IV Characteristics of Organic MOSFETs

Dr. Sivasankaran K
Department of Micro and Nanoelectronicsname of organization
Vellore Institute of Technology
Vellore, Tamil Nadu, India
ksivasankaran@vit.ac.in

Mr. Vansh Jain
(student)
School of Electronics Engineering
Vellore Institute of Technology
Vellore, Tamil Nadu, India
vansh.anuj29@gmail.com

Mr. Karthik Mukund
(student)
School of Electronics Engineering
Vellore Institute of Technology
Vellore, Tamil Nadu, India
karthik.mukund2002@gmail.com

Abstract* — Organic Metal-Oxide-Semiconductor Field- Effect Transistors (MOSFETs) have emerged as a cornerstone for advancing flexible electronics, yet the interplay of design parameters on their electrical performance remains an untamed frontier. This gap limits the ability to fine-tune these transistors for real-world applications. In this study, we dive into the realm of organic MOSFETs using Silvaco TCAD simulations to unravel the impact of three critical parameters: channel length, oxide layer thickness, and electrode work function. By tweaking the channel width, we unveil its subtle yet impactful role in modulating device efficiency. Adjustments to the oxide layer thickness, reveal its undeniable influence on gate control and leakage currents. Lastly, we embark on a dual-probe exploration of the electrode work function, alternately modulating the gate, source, and drain configurations to decode their combined effect on IV characteristics. With meticulously plotted I_d vs. V_{gs} curves, derived from both simulation and Excel-assisted analysis, our findings paint a vivid picture of parameter sensitivity. This research not only enhances the understanding of MOSFET behaviour but also sets the stage for optimizing organic electronics for next-gen applications. Whether you're in it for the numbers or the nanotech marvel, this paper has something intriguing for every enthusiast.

Keywords - Organic MOSFETs, Silvaco TCAD, Channel length, Oxide layer thickness, Electrode work function, IV characteristics, Flexible electronics.

I. Introduction

A. Background

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a cornerstone of modern electronics, powering devices from microprocessors to memory units. Organic MOSFETs, with their potential for flexibility and cost-effectiveness, represent the next frontier in semiconductor technology. Key parameters such as channel length, oxide layer thickness, and electrode work function play pivotal roles in determining the electrical performance of these devices. Precise control and understanding of these parameters are crucial to optimizing MOSFETs for real-world applications.

B. Motivation

The performance and reliability of MOSFETs are intricately linked to the interplay of the design parameters when it comes to designing any application. When is comes to the case involving MOSFETs, variations in channel length influence charge transport efficiency, changes in oxide thickness affect gate control and leakage currents, and shifts in electrode work function modify the energy barriers for charge carriers. Despite their importance, these parameters are often studied in isolation, leaving gaps in understanding their collective impact. Simulation-based studies, particularly using tools like Silvaco TCAD, provide an efficient and detailed approach to analyze these effects comprehensively, paving the way for innovative designs and improved device performance.

C. Scope of Study

This study investigates the influence of three parameters—channel length, oxide layer thickness, and electrode work function—on the IV characteristics of organic MOSFETs using Silvaco TCAD simulations. The work includes:

1) Systematic alteration of these parameters to evaluate their individual and combined effects on device operation.
2) Generation of Id vs. Vgs plots to visualize and quantify the impact.

3) Analysis of results to identify trends and insights for optimizing MOSFET performance.

This approach provides a comprehensive understanding of how critical design parameters affect organic MOSFET functionality, offering valuable guidance for future advancements in flexible and organic electronics.

II. Literature Review

Tachiki et al. used a saturation drain current analysis to investigate the short-channel effects in SiC-based MOSFETs. Their results provided important insights into the behaviour of scaled MOSFETs and brought attention to the performance issues caused by shorter channel lengths [1]. The current study's emphasis on channel length fluctuations in organic MOSFETs is in line with this work.

In their overview of MOSFET scaling developments, Ratnesh et al. emphasised the trade-offs of decreasing oxide thickness, such as higher leakage currents. Their findings are especially pertinent to comprehending how oxide layer height affects device performance [2]. The performance issues in sub-45 nm MOSFET architectures were also thoroughly reviewed by Mendiratta and Tripathi, who focused on short-channel effects in particular. These issues are closely related to the current studies of channel length in organic MOSFETs [3].

In a comparative analysis of MOSFET scaling technologies, Lee and Lee concentrated on the effects of dimensional changes on device performance. Their results offer a framework for investigating how channel width affects MOSFET IV properties [4]. In support of this, Kim et al. examined electrical behaviours in gate-all-around MOSFETs made of stacked nanosheets, focussing on the impact of channel engineering, which helps with the investigation of channel variations in organic MOSFETs [5].

Numerous studies have also been conducted on the impact of the gate electrode's work function on device performance. In their analysis of the gate work function's influence on low-power MOSFET design, Gupta and Tiwari showed how important it is in influencing threshold voltage and device behaviour [6]. The current study's emphasis on work function differences in organic MOSFETs is supported by this conclusion. In a similar vein, Choi and Choi investigated how work function changes in tunnelling FETs affected current modulation [12]. In order to comprehend IV characteristics, Zhang et al. further investigated gate design and work function effects in advanced MOSFETs, offering insights into their interaction with current flow [13].

Much research has also been done on oxide layer characteristics and how they affect MOSFET performance. Chen provided important information on the function of oxide thickness in his study of threshold voltage drift brought on by changes in gate oxide characteristics [7]. The importance of oxide integrity for device performance was highlighted by Karki and Peng's analysis of gate oxide deterioration and its effects on electrical parameters [8]. Comparable to the current study of oxide layer height in organic MOSFETs, Sinha and Chaudhury offered a thorough examination of gate capacitance as a function of oxide thickness across a variety of FET topologies [9]. By demonstrating GaAs MOSFETs with oxide gate dielectrics and examining their electrical properties, Ye et al. made a contribution to this field and highlighted the significance of oxide layers [10].

Furthermore, Kubo et al. investigated how interface state density affected MOSFET performance, paying special attention to the interaction between oxide and interface characteristics. Understanding changes in oxide layer height in organic MOSFETs is made possible by this work [11]. The advantages and difficulties of scaling oxide thickness were covered in Hasan and Lee's study on high-k dielectrics, which gave crucial background information for scaling concerns [14]. Last but not least, Fischetti and Lai investigated transport mechanisms in two-dimensional materials, tackling the opportunities and difficulties of MOSFET scaling and providing a more comprehensive understanding of how material properties affect device behaviour [15].

III. Simulation Setup

A. Simulation Environment

Silvaco TCAD is a robust suite of simulation tools tailored for semiconductor device modeling and analysis. It integrates both process and device simulation capabilities, allowing for a comprehensive examination of device behavior under varying conditions. In this study, we employed the Silvaco ATLAS module to simulate the electrical characteristics of organic MOSFETs.

B. Design Parameters

The MOSFET structure was specified with the following parameters:

1) *Source/Drain Materials*: The source and drain regions were modeled using organic semiconductor materials, with doping concentrations optimized for desired conductivity.

2) *Dimensions:* The channel length was set at 10nm, while the channel width was varied to assess its impact on device performance.

3) *Gate Material:* A metal gate was utilized, with its work function adjusted to study its effect on device behavior.

These parameters served as the baseline configuration for the simulations.

C. Altered Parameters

To evaluate the functionality of the MOSFET, the following parameters were systematically varied in the Silvaco TCAD simulations:

1) *Channel Width:* The channel width was varied from 50nm to 200nm in increments of 50nm to observe its influence on current conduction and overall device performance.

2) *Oxide Thickness:* The gate oxide layer thickness was adjusted between 2.2nm and 3.0nm, in increments of 0.2nm, to evaluate its effect on gate control and leakage currents.

3) *Work Function Alterations:*

   a) *Gate Work Function:* The gate work function was varied from 4.0eV to 5.0eV in 0.5eV steps to determine its impact on threshold voltage and subthreshold swing.

   b) *Source/Drain Work Function:* The work functions of the source and drain electrodes were adjusted between 4.0eV and 5.0eV, in increments of 0.5eV, to assess their effect on contact resistance and current drive capability.

D. Data Collection

The simulation procedure to obtain the Id vs. Vgs plots involved the following steps:

1) *Device Initialization:* Defining the MOSFET structure, including materials, dimensions, and doping profiles.

2) *Parameter Variation:* Systematic variation of each parameter (channel width, oxide thickness, and work function) while keeping other parameters constant.

3) *Electrical Simulation:* Performing DC simulations for each configuration to obtain the drain current (Id) as a function of gate-source voltage (Vgs).

4) *Data Extraction:* Exporting simulation results using Silvaco's TonyPlot tool, which allows data to be exported to CSV files for further analysis. In Microsoft Excel, the data was processed to generate Id vs. Vgs plots, enabling visual comparison of the device's electrical characteristics under different parameter configurations.

IV. Research Methodology

A. Channel Width Alteration

The channel width (W) is a fundamental design parameter in MOSFETs that significantly impacts the device's current-carrying capacity. By modifying the channel width, we can analyze its effect on the MOSFET's electrical performance, especially its transfer characteristics, such as the drain current (I_d) versus gate-source voltage (V_{gs}) relationship.

The relationship between I_d and W in MOSFET operation can be expressed as follows:

For Linear Region ($V_{ds} < V_{gs} - V_{th}$):

$$I_d = \mu_n . C_{ox} . \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

where I_d is drain current, μ_n is electron mobility, C_{ox} is oxide capacitance per unit area, W is channel width, L is channel length, V_{gs} is gate-source voltage, V_{th} is threshold voltage, and V_{ds} is drain-source voltage. In the above formula used, it is clear that for the linear region, I_d is directly proportional to the W, which increases with the conduction area for charge carriers.

For Saturation Region ($V_{ds} < V_{gs} - V_{th}$):

$$I_d = \frac{1}{2} \mu_n . C_{ox} . \frac{W}{L} \left[(V_{gs} - V_{th})^2 (1 + \lambda V_{ds}) \right]$$

where λ is channel-length modulation parameter.

For V_{th}:

$$V_{th} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - 2\phi_f$$

as we can see in the above given formula, V_{th} is not depended on the W value at all, but the vice-versa is not true. So, from the above given theoretical description, we can easily tell the relation between the I_d and W as:

$$I_d \propto W$$

In this study, the channel width was varied between 2.5nm and 20nm using Silvaco TCAD to observe

how these changes impact the device's operation. Despite variations in W, Vth showed minimal deviation, confirming its dependence on gate-oxide properties and substrate doping.

B. Oxide Layer width alteration

The oxide layer in a MOSFET, in this case, SiO2, serves as the gate dielectric, playing a critical role in the electrostatic control of the channel. Its thickness (tox) directly impacts the gate capacitance, threshold voltage (V_{th}), and overall device performance. In this study, the oxide layer thickness was varied from 2.2nm to 3nm using Silvaco TCAD, and its effect on the transfer characteristics (I_d vs. V_{gs}) was analyzed.

The theoretical background of this consists of the same formulas as mentioned for the earlier case. It is just that in the previous case, we had C_{ox} value fixed, whereas in this case, its varied according to the formula:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

where the ϵ_{ox} is oxide layer permittivity and t_{ox} is the thickness of the oxide layer. Also, by changing the t_{ox} value, we basically change the Superthreshold Slope *(SS)* value, given as:

$$SS = \frac{ln10 \cdot kT}{2} \cdot (1 + \frac{C_{dep}}{C_{ox}})$$

A thinner oxide layer reduces SS, improving switching characteristics and reducing power consumption. Devices with thinner oxides exhibited higher I_d for the same V_{gs}, confirming improved gate control and channel connectivity. V_{th} decreases as t_{ox} is reduced, indicating easier channel inversion. This is evident from the steeper I_d vs. V_{gs} curves for thinner oxides, explaining the faster switching capabilities beneficial for small tech applications like microprocessors.

C. Work function alteration

The work function of the materials used in MOSFETs is a critical parameter that influences the electrostatic potential at the gate and its interaction with the semiconductor channel. Altering the work function of the gate or drain significantly affects the threshold voltage (V_{th}) and, consequently, the device's electrical performance. This study investigates the impact of work function variations, where the source and drain are kept constant while the gate's work function is altered, and vice versa. Simulations were performed using Silvaco TCAD, and the I_d vs. V_{gs} plots were analyzed.

The work function (ϕ_m) determines the energy required for electrons to move from the Fermi level of the material to the vacuum level. In MOSFETs, it influences several key parameters:

$$V_{th} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - 2\phi_f$$

and $\phi_{ms} = \phi_m - \phi_s$

where, ϕ_s is the semiconductor's work function. Modifying the gate work function changes the energy barrier for carrier injection into the channel, influencing how efficiently the device turns on or off. Rest as we have seen in the previous cases, a shift in V_{th} due to ϕ_m variations affects the gate voltage required to achieve a specific I_d.

Increasing ϕ_{gate} increases V_{th}, requiring a higher V_{gs} to turn on the MOSFET. Conversely, decreasing ϕ_{gate} reduces V_{th}, allowing easier channel inversion. A higher gate work function reduces I_d for a given V_{gs}, while a lower gate work function increases I_d. Variations in ϕ_{drain} primarily influence the output characteristics by modifying the potential barrier at the drain end. Optimizing ϕ_{gate} can enhance I_d and transconductance, while improper selection may lead to suboptimal V_{th} and off-state leakage. We can notice these changes in the Figure 4.

V. Results And Discussions

A. Effect of Channel Width

The variation in channel width significantly influenced the MOSFET's electrical performance, as depicted in the I_d vs. V_{gs} plots. Increasing the channel width from 2.5nm to 20nm led to a noticeable rise in the drain current (I_d), indicating enhanced charge carrier mobility due to reduced resistance. Wider channels provided a larger cross-sectional area for current flow, thereby improving device efficiency. However, this increase in width also resulted in higher power consumption, highlighting the need to balance performance with energy efficiency.

B. Effect of Oxide Thickness

Adjusting the oxide thickness from 2.2nm to 3.0nm revealed a critical trade-off between gate control and leakage current. Thinner oxides offered superior gate control, as evidenced by steeper I_d vs. V_{gs} curves, but were more susceptible to leakage currents due to tunneling effects. On the other hand, thicker oxides reduced leakage but weakened gate control, resulting in a flatter I_d vs. V_{gs} response. This finding underscores the importance of optimizing oxide thickness for specific applications, balancing control and stability.

C. Effect of Work Function Alteration

1) *Gate Work Function*: Altering the gate work function from 4.0eV to 5.0eV had a direct impact on the threshold voltage (V_{th}). Higher work functions led to increased V_{th}, shifting the I_d vs. V_{th} curve to the right. This adjustment improved subthreshold performance but could potentially compromise the on-state current.

2) *Source/Drain Work Function:* Changes in the source/drain work functions affected the contact resistance, influencing the saturation current (I_{dsat}). Higher work functions at the source/drain interfaces increased barrier heights, reducing current flow, while lower work functions facilitated charge injection, thus boosting current.

D. Comparison with Theoretical Insights

The observed trends are consistent with fundamental MOSFET principles. The dependence of I_d on channel width aligns with its inverse relation to resistance, as described by Ohm's law. Similarly, the impact of oxide thickness on gate control and leakage aligns with the gate capacitance equation ($C = \varepsilon/t$). Variations in work function conform to the Schottky-Mott theory, which describes the relationship between work function and barrier heights. These findings validate the simulations and provide actionable insights for optimizing organic MOSFETs.

VI. Conclusion

This study comprehensively examined the influence of channel width, oxide thickness, and electrode work function on the IV characteristics of organic MOSFETs using Silvaco TCAD simulations. Key findings include:

1) *Channel Width:* Increasing the channel width from 2.5nm to 20nm significantly boosted device performance by enhancing current flow due to reduced resistance. However, this improvement was accompanied by increased power consumption, necessitating careful optimization to balance performance and energy efficiency.

2) *Oxide Thickness:* Thinner oxide layers provided superior gate control, as evidenced by steeper I_d vs. V_{th} curves, but increased leakage currents due to tunneling effects. Thicker layers reduced leakage at the expense of weaker gate modulation, indicating that a balanced thickness is essential for achieving optimal performance.

3) *Work Function Alteration:*

   a) *Gate Work Function:* Variations in the gate work function from 4.0eV to 5.0eV had a significant impact on threshold voltage and subthreshold behavior. Higher work functions increased V_{th}, improving subthreshold performance but potentially compromising the on-state current.

   b) *Source/Drain Work Function:* Adjustments in the source/drain work functions influenced contact resistance and saturation current. Higher work functions at these interfaces increased barrier heights, reducing current flow, while lower work functions facilitated charge injection, enhancing current.

Among these parameters, oxide thickness emerged as the most critical due to its dual role in determining both gate control and leakage characteristics, which are crucial for MOSFET reliability and efficiency.

These findings have significant implications for the design of real-world devices, particularly in organic electronics. By optimizing these parameters, engineers can develop MOSFETs tailored for specific applications, such as low-power flexible electronics or high-performance sensors, thereby advancing the practical utility of organic semiconductor technology.

VII. Future Work

This research establishes a foundational understanding of the impact of channel width, oxide thickness, and work function on the performance of organic MOSFETs. However, several areas warrant further exploration:

1) *Incorporating Additional Parameters:* Future studies could examine the influence of temperature variations, doping concentrations, and different gate dielectric materials to gain a more comprehensive understanding of MOSFET behavior under various operating conditions.

2) *Three-Dimensional Simulations:* Extending simulations to a 3D model could capture spatial effects more accurately, providing detailed insights into device behavior, especially for large-scale applications.

3) *Validation with Experimental Data:* Conducting experimental studies to validate simulation results would enhance the reliability of the findings. Integrating real-world fabrication techniques and

device testing could uncover practical challenges and improve simulation accuracy.

4) *Exploring Alternative Materials:* Investigating emerging organic materials or hybrid structures could further optimize device performance for specific applications, such as flexible displays or wearable electronics.

References

[1] K. Tachiki, T. Ono, T. Kobayashi and T. Kimoto, "Short-Channel Effects in SiC MOSFETs Based on Analyses of Saturation Drain Current," IEEE Transactions on Electron Devices, vol. 68, no. 3, pp. 1382-1384, Mar. 2021, doi: 10.1109/TED.2021.3053518.

[2] R. K. Ratnesh, A. Goel, G. Kaushik, H. Garg, Chandan, M. Singh and B. Prasad, "Advancement and Challenges in MOSFET Scaling," Materials Science in Semiconductor Processing, vol. 134, 2021, Art. no. 106002, doi: 10.1016/j.mssp.2021.106002.

[3] N. Mendiratta and S. L. Tripathi, "A Review on Performance Comparison of Advanced MOSFET Structures Below 45 nm Technology Node," Journal of Semiconductors, vol. 41, no. 6, Jun. 2020, doi: 10.1088/1674-4926/41/6/061401.

[4] C. Lee and J. Lee, "Comparative Study on the Scaling of MOSFET Technologies," Journal of Electrical Engineering & Technology, vol. 16, no. 2, pp. 387-395, Apr. 2021, doi: 10.1007/s42341-021-00338-9.

[5] S. Kim et al., "Investigation of Electrical Characteristic Behavior Induced by Channel-Release Process in Stacked Nanosheet Gate-All-Around MOSFETs," IEEE Transactions on Electron Devices, vol. 67, no. 6, pp. 2648-2652, Jun. 2020, doi: 10.1109/TED.2020.2989416.

[6] B. Gupta and R. K. Tiwari, "A Comparative Analysis of Gate Work Function in MOSFETs for Low Power Design," in Advanced Nanoelectronics and Graphene Nanoribbon Technology, A. M. Vyas and K. J. Singh, Eds. Singapore: Springer, 2014, pp. 45-60, doi: 10.1007/978-81-322-3625-2_5.

[7] H. Chen, "Study on MOSFET Threshold Voltage Drift Based on SMAE Technology," MATEC Web of Conferences, vol. 61, 2016, Art. no. 06103, doi: 10.1051/matecconf/20166106103.

[8] U. Karki and F. Z. Peng, "Effect of Gate-Oxide Degradation on Electrical Parameters of Power MOSFETs," IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10764-10773, Dec. 2018, doi: 10.1109/TPEL.2018.2801848.

[9] S. K. Sinha and S. Chaudhury, "Impact of Oxide Thickness on Gate Capacitance—A Comprehensive Analysis on MOSFET, Nanowire FET, and CNTFET Devices," IEEE Transactions on Nanotechnology, vol. 12, no. 6, pp. 958-964, Nov. 2013, doi: 10.1109/TNANO.2013.2278021.

[10] P. D. Ye et al., "GaAs MOSFET with Oxide Gate Dielectric Grown by Atomic Layer Deposition," IEEE Electron Device Letters, vol. 24, no. 4, pp. 209-211, Apr. 2003, doi: 10.1109/LED.2003.812144.

[11] T. Kubo et al., "Study on Interface State Density Impact in MOSFETs," Materials Research Express, vol. 5, no. 2, 2018, doi: 10.1088/2043-6262/5/2/025002.

[12] K. M. Choi and W. Y. Choi, "Work-Function Variation Effects of Tunneling Field-Effect Transistors (TFETs)," IEEE Electron Device Letters, vol. 34, no. 8, pp. 942-944, Aug. 2013, doi: 10.1109/LED.2013.2264824.

[13] Y. Zhang et al., "Effects of Gate Design on Current Flow in Advanced MOSFETs," Physical Review Applied, vol. 19, no. 3, Art. no. 037001, Mar. 2023, doi: 10.1103/PhysRevApplied.19.037001.

[14] M. R. Hasan and S. H. Lee, "Advances in MOSFET Scaling with High-k Dielectrics," Current Opinion in Electronics Materials Science, vol. 4, no. 3, pp. 77-82, Feb. 2023, doi: 10.1016/j.cosele.2023.03.005.

[15] D. Fischetti and W. K. Lai, "Transport in Two-Dimensional Materials for MOSFET Scaling: Opportunities and Challenges," Microelectronics Journal, vol. 108, 2020, Art. no. 104893, doi: 10.1016/j.mejo.2020.104893.