

Project Portfolio

KARTHIK MUKUND

GitHub: [karthik-m-11](#) | LinkedIn: [Karthik Mukund](#) | Email: karthik.mukund2002@gmail.com | Phone: (+91) 9867174316

“Passionate about VLSI and designing performance-oriented ICs”

ABOUT ME

My Top Skills

- Functional Verification (UVM)
- Formal Verification using Assertions (SV)
- RTL Design (Verilog)
- Analog Circuit Design (SPICE)
- Programming for Automation (Python)

My Qualifications

- Industry Trained Design Verification Fresher, ChipEdge (2025)
- Research Internship in Satellite Control Systems, IIST (2024)
- B.Tech ECE, Vellore Institute of Technology - Vellore (2021 - 2025)

TABLE OF CONTENTS

About Me	ii
Internships, Research Papers, and Patents	1
1. DC Performance Analysis of MOS2FETs (Research Paper)	2
2. Reaction Wheel Attitude Control System in CubeSats (Internship)	3
3. Mono-Frequency Transmission for LEO Satellites (Patent).....	4
VLSI – RTL Design	5
1. PWM Signal Generator.....	6
2. Digital Stopwatch using FSM.....	7
3. Custom RISC-V Processor Design	8
Contact Me	9

Internships, Research Papers, and Patents

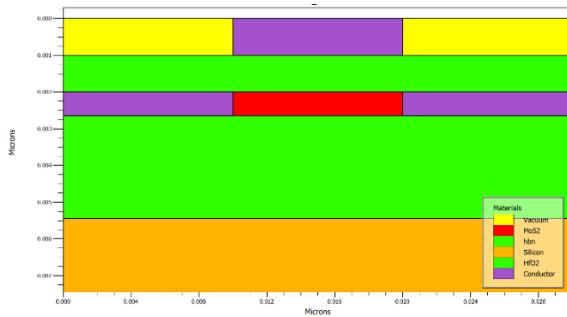
1. DC PERFORMANCE ANALYSIS OF MOS2FETs (RESEARCH PAPER)

Tool: Silvaco TCAD

Objective

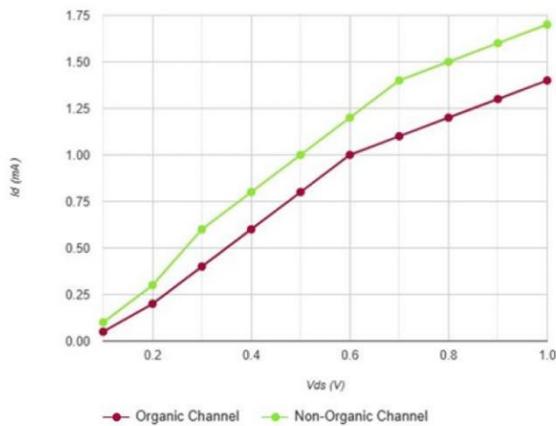
To analyze the impact of channel length, oxide height, and gate electrode work function on the I-V characteristics of MOS2FETs, and find the optimal specifications for high-speed and low-power switching applications such as wearable electronics and flexible displays.

Approach



A 2-D prototype for MOS2FET was designed in Silvaco TCAD, and each parameter was modified maintaining the others constant. The I-V curve was generated for each scenario, and the cut-off values for each noted and graphed for comparison.

Outcome



It was found that while keeping channel material constant, any changes in dimension or work function had negligible impact. However, when the channel material was changed from non-organic to organic, there was a marked increase in the voltage required to achieve the same current.

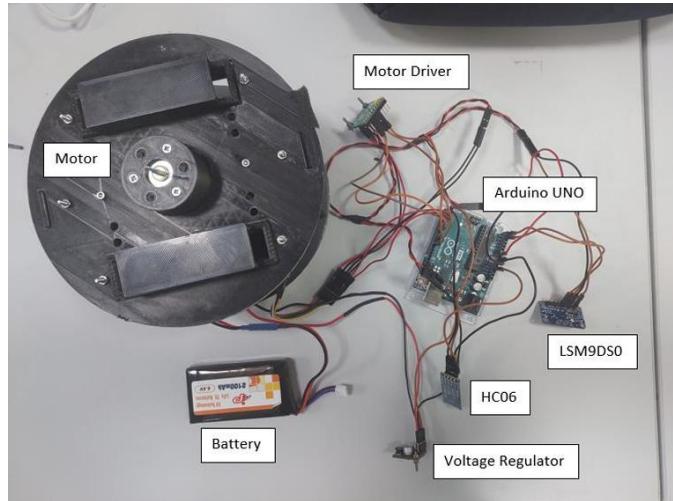
2. REACTION WHEEL ATTITUDE CONTROL SYSTEM IN CUBESATS (INTERNSHIP)

Language: C++ | Tool: Arduino IDE | Project was implemented in hardware

Objective

To design a single-axis reaction wheel control system, that will later be extended to 4-axes, for rapid recovery of attitude from disorientation during payload deployment.

Approach



A custom algorithm was developed and uploaded into an Arduino Uno microcontroller. The Arduino was then connected to a power source, sensors, and the reaction wheel motor actuator. The response times for correcting displacements in attitude were observed and noted.

Outcome



The designed prototype was tested on an air bearing floating bed test setup, and it was observed that it was successfully able to self-correct to its original attitude when externally disrupted.

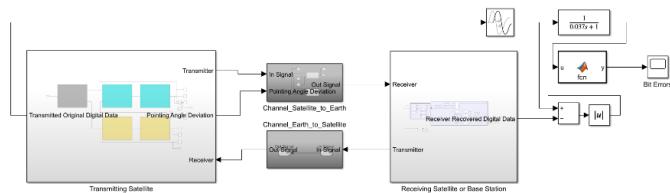
3. MONO-FREQUENCY TRANSMISSION FOR LEO SATELLITES (PATENT)

Tool: MATLAB Simulink

Objective

To explore mono-frequency transmission aided by a Lyapunov stability control system for power efficient and secure communication in autonomous satellites.

Approach



A model was designed in Simulink for the satellite's attitude stability submodule, satellite's signal transmission submodule, and the receiving station's signal recovery module. All the modules were connected and a channel was modeled to simulate noise and attenuation in the communication link. Artificial jitter was introduced to observe the satellite's attitude correction ability. The noise level was varied to observe the maximum noise the system could handle and still recover the original data.

Outcome



The designed system was observed to be able to recover the original data from a signal as noisy as -6dB, which is a 40-fold decrease from traditional optical communication systems. This allowed the transmitting laser at the satellite to use significantly less power (0.6816 W) than usually required.

VLSI – RTL Design

1. PWM SIGNAL GENERATOR

Language: Verilog | Tool: Linux, Icarus Verilog + GTKWave

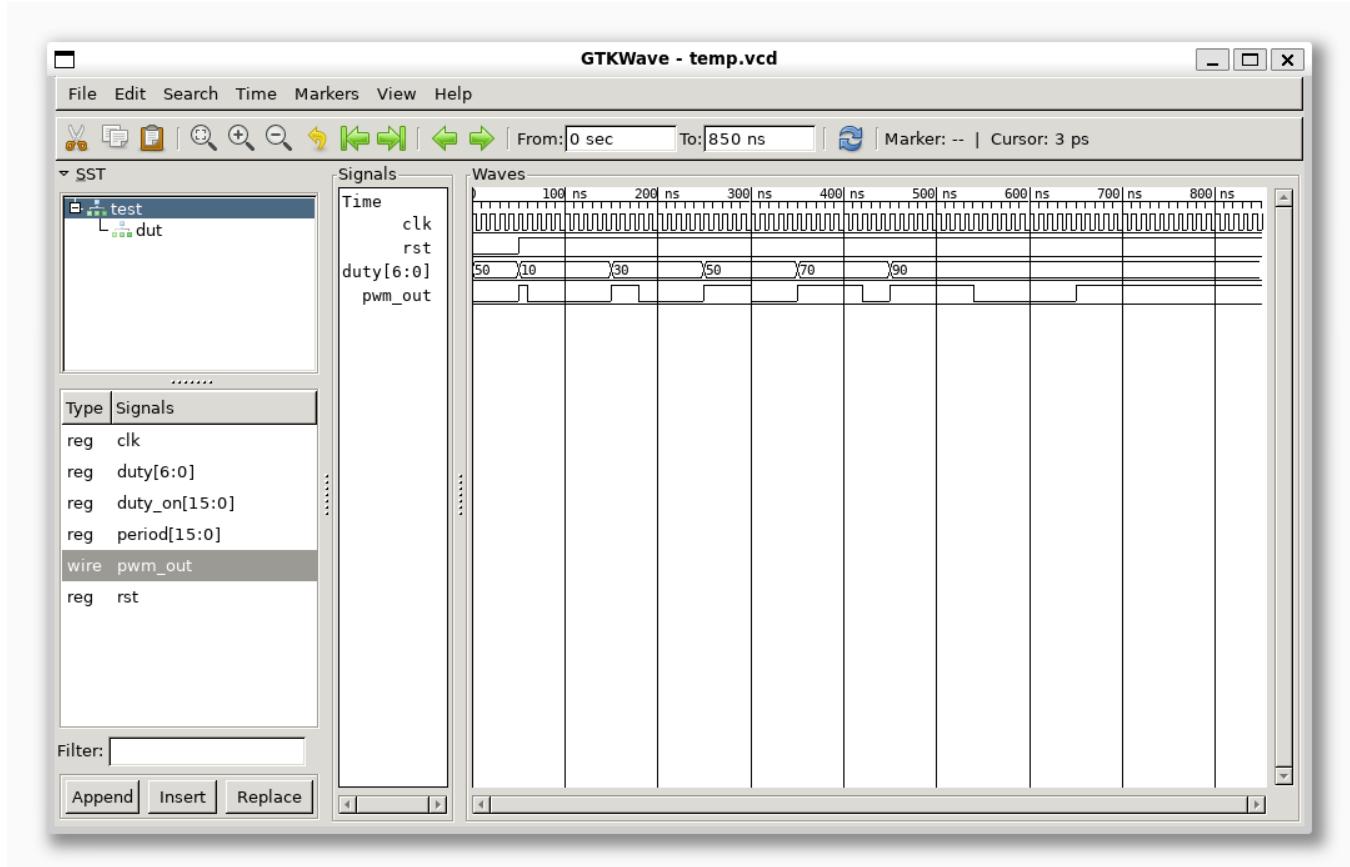
Objective

To design a PWM signal generator in Verilog.

Approach

A Verilog program was written to design a PWM signal generator modeled on an up-counter. A testbench was written to verify the design's functionality. The files were then compiled and simulated using Icarus Verilog, and the waveform was generated using GTKWave for observation and analysis.

Outcome



2. DIGITAL STOPWATCH USING FSM

Language: Verilog | Tool: Linux, Icarus Verilog + GTKWave

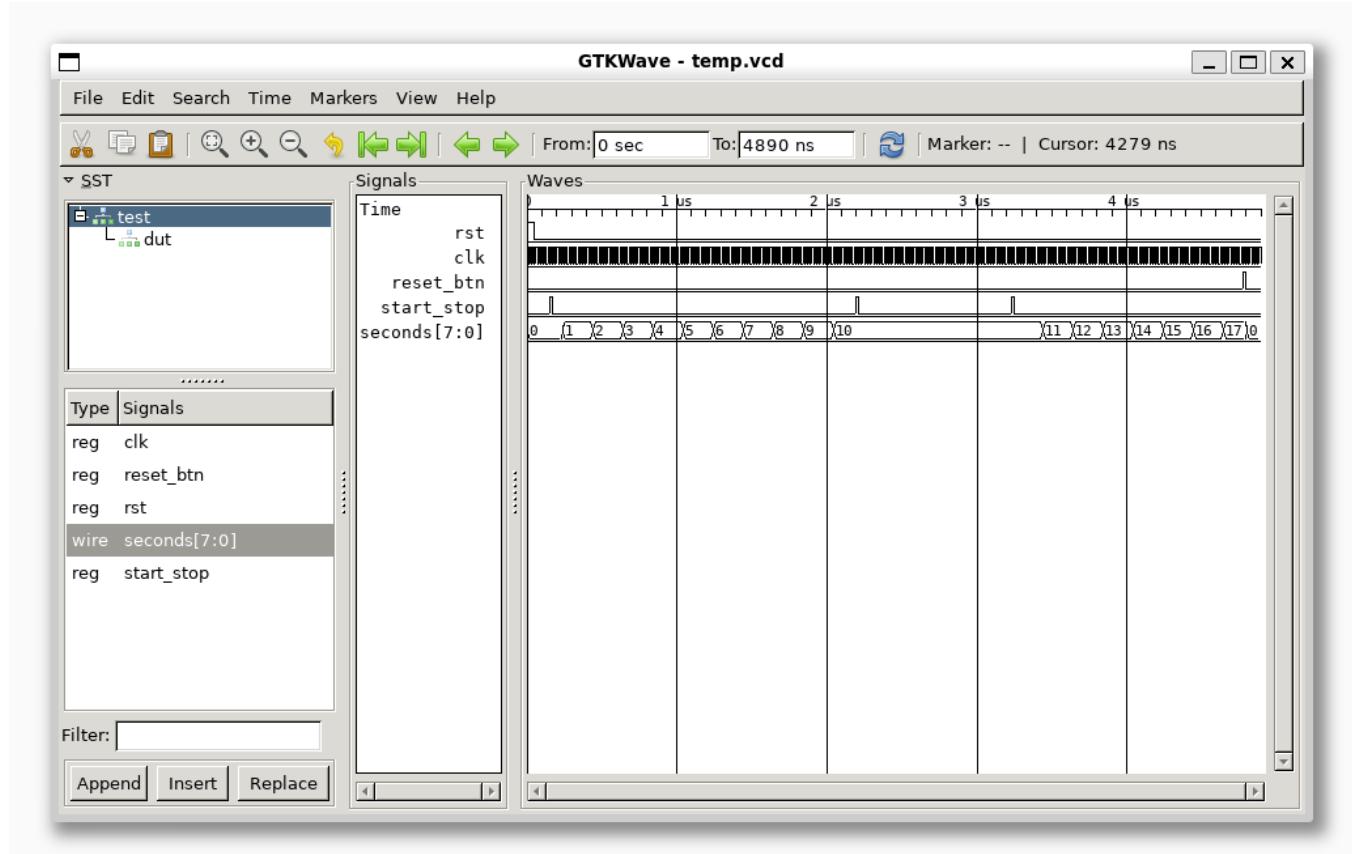
Objective

To design a digital stopwatch using FSM in Verilog.

Approach

A Verilog program was written to design a digital stopwatch modeled using an FSM. A testbench was written to verify the design's functionality. The files were then compiled and simulated using Icarus Verilog, and the waveform was generated using GTKWave for observation and analysis.

Outcome



3. CUSTOM RISC-V PROCESSOR DESIGN

Language: Verilog | Tool: Linux, Icarus Verilog + GTKWave

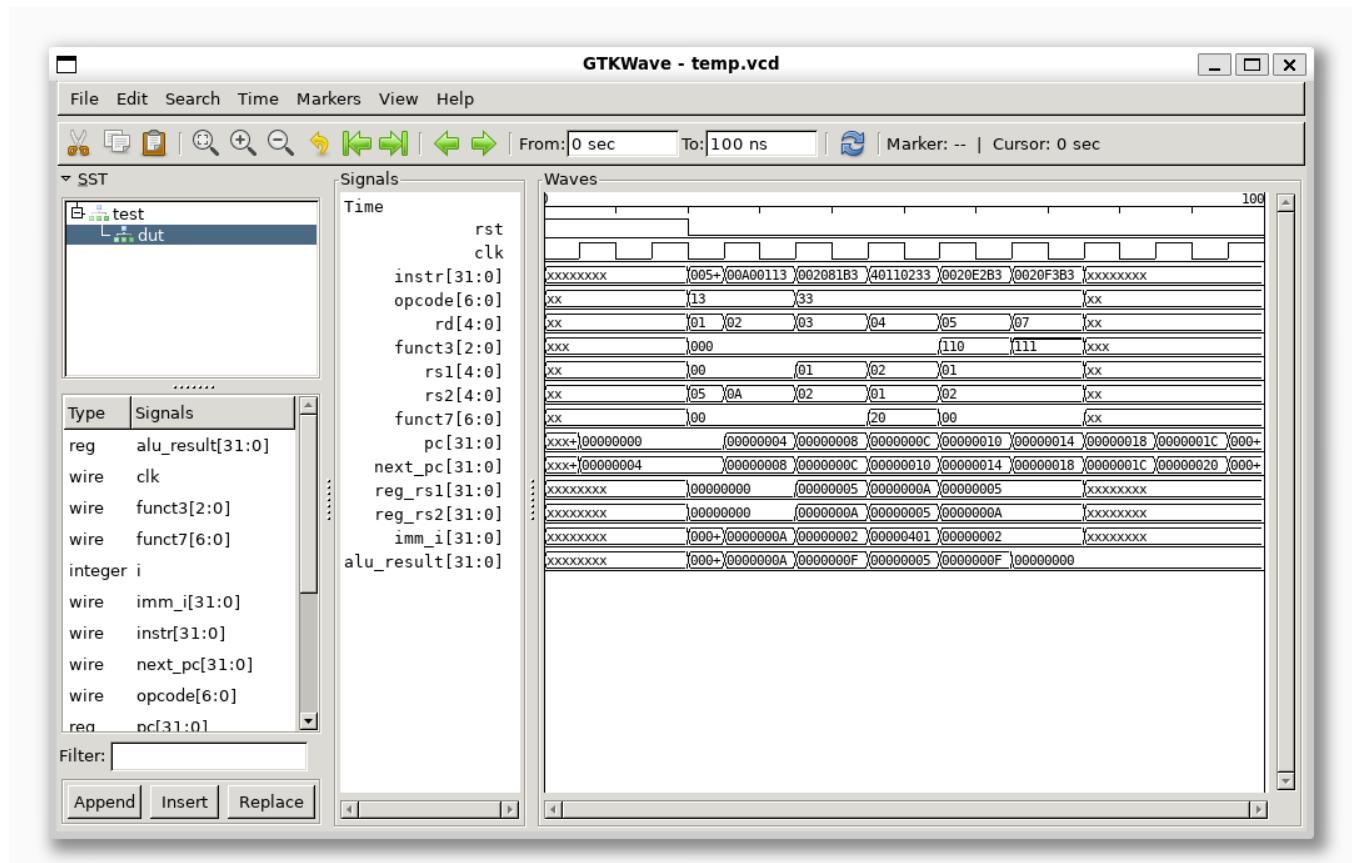
Objective

To design a basic 3 stage “decode → alu → write_back” RISC-V based 32-bit microprocessor.

Approach

A Verilog program was written to design the custom RISC-V microprocessor implementing an instruction memory, program counter, regfile, ALU, and ports. A testbench was written to verify the design’s functionality. The files were then compiled and simulated using Icarus Verilog, and the waveform was generated using GTKWave for observation and analysis.

Outcome



CONTACT ME

Phone: (+91) 9867174316

Email: karthik.mukund2002@gmail.com

LinkedIn: [Karthik Mukund](#)

GitHub: [karthik-m-11](#)