Karthik Somayaji NS

805-280-6785 karthi@ucsb.edu linkedin.com/in/karthik github.com/karthik google-scholar/karthik

Education

University of California, Santa Barbara **September 2021 – December 2026**
*Doctor of Philosophy (PhD) — CGPA - **3.8**/4.0* *Santa Barbara, CA*

University of California, Santa Barbara **September 2019 – September 2021**
*Master of Science (MS) — CGPA - **3.85**/4.0* *Santa Barbara, CA*

PES University **August 2014 – May 2018**
*Bachelor of Technology (B.Tech) — CGPA - **9.11**/10* *Bangalore, India*

Experience

University of California, Santa Barbara **September 2021 – Present**
Graduate Student Researcher — Advisor: Prof. Peng Li *Santa Barbara, CA*

- Developed theoretically grounded algorithms for uncertainty quantification in reinforcement learning and large language models (LLMs).
- Proposed machine-learning-driven optimization frameworks for analog circuit design and verification, enabling domain-adapted AI for semiconductor workflows.

Siemens EDA **June 2025 – September 2025**
Applied ML Research Intern *Fremont, CA*

- Developed symbolic modeling and symbolic sensitivity analysis for parasitic components in physical design, correlating RC variations to path delay in worst-slack nets.
- Achieved a 2× reduction in sensitivity analysis runtime while maintaining accuracy consistent with manual analysis.

Siemens EDA **June 2024 – September 2024**
Applied ML Research Intern *Fremont, CA*

- Developed physics-informed ML optimization techniques for standard-cell delay matching, achieving 100× reduction in optimization turnaround time.

Intel Corporation **June 2022 – September 2022**
Summer Research Intern *Remote*

- Incorporated reinforcement learning for wire-path suggestions in global routing.
- Developed a transformer-based net-ordering algorithm using REINFORCE for combinatorial routing optimization, achieving 2× faster runtime compared to baselines.

Projects

Safe Inference for Reasoning LLMs: An Uncertainty Perspective **December 2025**

- Formulated a step- and path-level uncertainty score for chain-of-thought LLMs by leveraging time-consistent signatures across multiple sampled reasoning traces.
- Used the proposed score to drive safe answer selection and abstention, improving best-of-N selection on math reasoning and general-knowledge benchmarks over logit- and confidence-based baselines.

GAUSS: Graph-Aligned Uncertainty for Long-Form LLM Generation **September 2025**

- Modeled each generated paragraph as a semantic graph of atomic facts and inter-fact relations, and defined uncertainty as the expected alignment cost between an anchor graph and alternative generations via an optimal-transport-based graph distance.
- Showed that GAUSS yields uncertainty scores that better track factual consistency and structural coherence than probability- and calibration-based baselines on long-form clinical, legal, and encyclopedic benchmarks.

LLM-USO: Large Language Model-Based Universal Sizing Optimizer for Analog Circuits **September 2025**

- Designed a hybrid BO–LLM framework that extracts structured design-knowledge summaries linking performance metrics, critical sub-structures, and sizing parameters, and reuses them across circuits with shared sub-topologies.
- Integrated a critique LLM and GP-based uncertainty ranking of LLM suggestions, achieving better gain/CMRR/UGF and reduced simulation budgets than GP-BO and ADO-LLM on amplifiers, comparators, LDOs, and DC–DC converters.

ADO-KT: Analog Design Optimization via Knowledge Transfer Using LLMs **June 2025**

- Built AI analog design agents that represent transistor-level netlists as multi-layer knowledge graphs and use LLMs to extract, critique, and transfer human-interpretable design rules between circuits with shared sub-structures.
- Demonstrated that graph-based knowledge transfer accelerates convergence and improves final performance trade-offs compared to per-circuit optimization baselines with no cross-task knowledge reuse.

Extreme Risk Mitigation in Reinforcement Learning Using Extreme Value Theory **January 2024**

- Introduced an EVT-based parameterization of the tail of the distributional state–action value function using generalized Pareto distributions, enabling explicit modeling of rare catastrophic events.
- Provided theoretical guarantees on tail-risk control and empirically reduced the frequency and severity of catastrophic failures versus standard risk-sensitive RL algorithms across diverse continuous-control tasks.

Representation Learning for Analog Performance Modelling **February 2024**

- Developed a semi-supervised contrastive regression framework (Learn-by-Compare) that learns latent representations of sizing solutions by comparing performance-similar and dissimilar design pairs.
- Designed transistor-level data augmentations (local-scaling and global-symmetry based) using circuit design knowledge, achieving higher analog performance prediction accuracy than conventional supervised regressors.

Pareto Optimization of Analog Circuits Using Reinforcement Learning **December 2023**

- Extended multi-objective reinforcement learning to continuous state and action spaces for analog circuit sizing, learning a single preference-conditioned policy to generate Pareto-optimal design points.
- Produced high-quality Pareto fronts and competitive or better sample efficiency compared to NSGA-II and other multi-objective baselines on multiple analog circuit benchmarks.

Optimization of Analog Circuit Design Using Prioritized Reinforcement Learning **December 2021**

- Proposed a prioritized replay RL framework that incorporates designer knowledge into the critic network, reward shaping, and prioritized experience replay to make analog circuit sizing more sample efficient.
- Achieved faster convergence to high-performance design points and reduced transistor-level simulation calls relative to vanilla deep RL baselines on op-amp sizing tasks.

Technical Skills

Python, Matlab, Verilog, LaTeX, PyTorch, OpenAI Gym, Pandas, NumPy, Scikit-Learn, Matplotlib, Seaborn

Publications

- Domain-Specific Optimization for Fast and Accurate Delay Matching in Parasitic Extraction Qualification (Under Review - ACM TODAES)
- GAUSS: Graph-Assisted Uncertainty Quantification using Structure and Semantics for Long-Form Generation in LLMs (Under Review - ICLR'26)
- AI Analog Circuit Design Agents: On Knowledge Extraction and Transfer with Knowledge Graphs (ICCAD'25)
- LLM-USO: Large Language Model-based Universal Sizing Optimizer (TCAD'25)
- Learn-by-Compare: Analog Performance Prediction using Contrastive Regression with Design Knowledge (DAC'24)
- Extreme Risk Mitigation in Reinforcement Learning using Extreme Value Theory. (TMLR'24).
- Pareto Optimization of Analog circuits using Reinforcement Learning. Accepted at (ACM TODAES'24).
- Prioritized Reinforcement Learning for Circuit Optimization with Design Knowledge. Accepted at (Design Automation Conference (DAC'21)).

Awards / Honors

- Our work on extreme-value reinforcement learning has been awarded the J2C certification and was selected for presentation at (ICLR '25).
- Our work on extreme-value reinforcement learning was featured in SIAM News (2024).
- DAC Young Fellowship 2021 — successfully completed Cadence Design System's HLS mini-project and presented a short summary of my interests.