
Report : timing

-path full

-delay max

-max_paths 1

Design : fifo

Version: I-2013.12-SP5-4

Date : Mon Apr 29 23:49:37 2019

Operating Conditions: TYPICAL Library: saed90nm_typ

Wire Load Model Mode: enclosed

Startpoint: r2w1/r2wsync_ff2_reg[3]

(rising edge-triggered flip-flop clocked by clk_in)

Endpoint: w1/wptra_reg[0]

(rising edge-triggered flip-flop clocked by clk_in)

Path Group: clk_in

Path Type: max

Des/Clust/Port	Wire Load Model	Library
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fifo	280000	saed90nm_typ
write_logic_depth7_width8	8000	saed90nm_typ

Point	Incr	Path
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clock clk_in (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
r2w1/r2wsync_ff2_reg[3]/CLK (DFFARX1)	0.00	0.00
r		
r2w1/r2wsync_ff2_reg[3]/Q (DFFARX1)	0.19	0.19
f		
r2w1/r2wsync_ff2[3] (sync_rd2wr_width8_depth7)	0.00	0.19
f		
w1/r2wsync_ff2[3] (write_logic_depth7_width8)	0.00	0.19
f		
w1/U85/Q (XNOR2X2)	0.64	0.83
f		
w1/U77/Q (AND4X1)	0.13	0.96
f		
w1/U70/Q (AND4X1)	0.11	1.07
f		
w1/U69/QN (NAND2X0)	0.07	1.14
r		
w1/U65/Q (AND2X1)	0.10	1.24
r		
w1/U67/Q (OA21X1)	0.09	1.33
r		
w1/U58/Q (AO22X1)	0.10	1.43
r		

w1/wptra_reg[0]/D (DFFARX1)	0.03	1.46
r data arrival time		1.46
clock clk_in (rise edge)	1.00	1.00
clock network delay (ideal)	0.00	1.00
w1/wptra_reg[0]/CLK (DFFARX1)	0.00	1.00
r library setup time	-0.09	0.91
data required time		0.91

data required time		0.91
data arrival time		-1.46

slack (VIOLATED)		-0.55

Startpoint: w2r1/w2rsync_ff2_reg[7]
(rising edge-triggered flip-flop clocked by clk_out)
Endpoint: r1/rptra_reg[4]
(rising edge-triggered flip-flop clocked by clk_out)
Path Group: clk_out
Path Type: max

Des/Clust/Port	Wire Load Model	Library

fifo	280000	saed90nm_typ
read_logic_depth7_width8	8000	saed90nm_typ

Point	Incr	Path

clock clk_out (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
w2r1/w2rsync_ff2_reg[7]/CLK (DFFARX1)	0.00	0.00
r w2r1/w2rsync_ff2_reg[7]/Q (DFFARX1)	0.19	0.19
f w2r1/w2rsync_ff2[7] (sync_wr2rd_width8_depth7)	0.00	0.19
f r1/w2rsync_ff2[7] (read_logic_depth7_width8)	0.00	0.19
f r1/U6/Z (NBUFFX4)	0.75	0.94
f r1/U4/Q (XNOR2X1)	0.19	1.13
r r1/U13/QN (NAND2X0)	0.07	1.20
f r1/U12/QN (NOR2X0)	0.09	1.29
r		

r1/U59/QN (NOR3X0)	0.11	1.39
f r1/U58/Q (AO21X1)	0.11	1.50
f r1/U55/QN (NOR2X0)	0.09	1.59
r r1/U53/Q (OA21X1)	0.11	1.70
r r1/U50/Q (AO22X1)	0.12	1.82
r r1/rptr_reg[4]/D (DFFARX1)	0.03	1.85
data arrival time		1.85
clock clk_out (rise edge)	2.00	2.00
clock network delay (ideal)	0.00	2.00
r1/rptr_reg[4]/CLK (DFFARX1)	0.00	2.00
r library setup time	-0.09	1.91
data required time		1.91

data required time		1.91
data arrival time		-1.85

slack (MET)		0.06