```
#Read the design in
read_file -format verilog {"seqdetector.v"}

#set the current design
set current_design seq_detect

#Link the design
link

#create clockand constrain the design
create_clock "clk" -period 4     -name  "clk"
set_input_delay -clock clk  -max -rise 0.35 "x"
set_input_delay -clock clk  -min -rise 0.1 "x"
set_output_delay -clock clk  -max -rise 0.8 "z"
set_output_delay -clock clk  -min -rise 0.2 "z"

set_dont_touch_network  "clk"
set_max_area 0

#Set operating conditions
set_operating_conditions -library "saed90nm_typ" "TYPICAL"
#Synthesize and generate report
compile  -map_effort high -boundary_optimization
report_attribute >  report1
report_area >  report2
report_constraints -all_violators > report3
report_timing -path full -delay max -max_paths 1 -nworst 1  >
report4
report_timing -path full -delay min -max_paths 1 -nworst 1  >
report5
```