```
//Declaration of Module ALU
module ALU #(parameter size = 32)  (A, B, ctrl, R, O, N, Z);

//Input Declaration
input [size - 1 : 0] A, B;
input [1:0] ctrl;

//Output Declaration
output [size - 1 : 0] R;
output O, N, Z;

//Reg Declaration
reg signed [size - 1 : 0] R;
reg O, N, Z;

//Enter Always when any of the signals change
always @ ( * )
        begin
                case(ctrl)

                        2'b00:
                                begin
                                        R = A + B;
                                        N = R[size -1];
                                        O = (((~A[size -1]) & (~B[size -1]) & R[size -1
]) | (A[size -1] & B[size -1] &(~R[size -1])));
                                end

                        2'b01:
                                begin
                                        R = A - B;
                                        N = R[size -1];
                                        O = (((~A[size -1]) & B[size -1] & R[size -1])
| (A[size -1] & (~(B[size -1]) &(~ (R[size -1])))));
                                end



                        2'b10: R = A & B;
                        2'b11: R = A | B;
                        default: $display("Invalid Test Signals");
                endcase

                if ( R == 0)
                        begin
                                O = 1'b0;
                                Z = 1'b1;
                        end

                else
                        Z = 1'b0;

        end
endmodule
```

```
‘include "ALU.v"

module ALU_fixture;
parameter size = 32;
reg signed[size -1:0] A,B;
reg [1:0] ctrl;
wire signed [size -1:0] R;
wire O, N, Z;
initial
        $vcdpluson;

initial
        $monitor($time, "A= %h B= %h Ctrl= %b ||Res= %h Zero=%b Ovf=%b Neg=%b",A,B,ctrl
,R[size -1:0],Z,O ,N);

ALU a1(A , B, ctrl, R, O, N, Z);


initial
        begin
//Test Cases for Addition and Subraction
                        A = 32’hFFFFFF00;
                        B = 32’hFFFFFFFF;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;

                #10     A = 32’hFFFFFFFF;
                        B = 32’h000F00FF;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;


                #10     A = 32’h67676767;
                        B = 32’h12341234;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;

                #10     A = 32’hAAAAAAAA;
                        B = 32’hEFABCD16;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;


                #10     A = 32’hFFFFFFFF;
                        B = 32’h00000001;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;


                #10     A = 32’hFFFFFFFF;
                        B = 32’hFFFFFFFF;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;

                #10     A = 32’hFFFFFFFC;
                        B = 32’hFFFFFFFC;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;

                #10     A = 32’hFFFF0000;
                        B = 32’h00001342;
                        ctrl = 2’b00;
                #10     ctrl = 2’b01;
```

```
                #10     A = 32'h01234567;
                        B = 32'h00080808;
                        ctrl = 2'b00;
                #10     ctrl = 2'b01;

//Test Cases for OR and AND
                #10     A = 32'hFFFFFFFF;
                        B = 32'h0A0AB0B0;
                        ctrl = 2'b10;
                #10     ctrl = 2'b11;

                #10     A = 32'hABCD4545;
                        B = 32'h12383588;
                        ctrl = 2'b10;
                #10     ctrl = 2'b11;

                #10     A = 32'hF0F0F0F0;
                        B = 32'hCFCFCFCF;
                        ctrl = 2'b10;
                #10     ctrl = 2'b11;

                #10     A = 32'h00000000;
                        B = 32'h11111111;
                        ctrl = 2'b10;
                #10     ctrl = 2'b11;



        end

initial
        begin
                #300 $finish;
        end
endmodule
```

```
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                  0A= ffffff00 B= ffffffff Ctrl= 00 ||Res= fffffeff Zero=0 Ovf=0 Neg=1
                 10A= ffffff00 B= ffffffff Ctrl= 01 ||Res= ffffff01 Zero=0 Ovf=0 Neg=1
                 20A= ffffffff B= 000f00ff Ctrl= 00 ||Res= 000f00fe Zero=0 Ovf=0 Neg=0
                 30A= ffffffff B= 000f00ff Ctrl= 01 ||Res= fff0ff00 Zero=0 Ovf=0 Neg=1
                 40A= 67676767 B= 12341234 Ctrl= 00 ||Res= 799b799b Zero=0 Ovf=0 Neg=0
                 50A= 67676767 B= 12341234 Ctrl= 01 ||Res= 55335533 Zero=0 Ovf=0 Neg=0
                 60A= aaaaaaaa B= efabcd16 Ctrl= 00 ||Res= 9a5677c0 Zero=0 Ovf=0 Neg=1
                 70A= aaaaaaaa B= efabcd16 Ctrl= 01 ||Res= bafedd94 Zero=0 Ovf=0 Neg=1
                 80A= ffffffff B= 00000001 Ctrl= 00 ||Res= 00000000 Zero=1 Ovf=0 Neg=0
                 90A= ffffffff B= 00000001 Ctrl= 01 ||Res= fffffffe Zero=0 Ovf=0 Neg=1
                100A= ffffffff B= ffffffff Ctrl= 00 ||Res= fffffffe Zero=0 Ovf=0 Neg=1
                110A= ffffffff B= ffffffff Ctrl= 01 ||Res= 00000000 Zero=1 Ovf=0 Neg=0
                120A= fffffffc B= fffffffc Ctrl= 00 ||Res= fffffff8 Zero=0 Ovf=0 Neg=1
                130A= fffffffc B= fffffffc Ctrl= 01 ||Res= 00000000 Zero=1 Ovf=0 Neg=0
                140A= ffff0000 B= 00001342 Ctrl= 00 ||Res= ffff1342 Zero=0 Ovf=0 Neg=1
                150A= ffff0000 B= 00001342 Ctrl= 01 ||Res= fffeecbe Zero=0 Ovf=0 Neg=1
                160A= 01234567 B= 00080808 Ctrl= 00 ||Res= 012b4d6f Zero=0 Ovf=0 Neg=0
                170A= 01234567 B= 00080808 Ctrl= 01 ||Res= 011b3d5f Zero=0 Ovf=0 Neg=0
                180A= ffffffff B= 0a0ab0b0 Ctrl= 10 ||Res= 0a0ab0b0 Zero=0 Ovf=0 Neg=0
                190A= ffffffff B= 0a0ab0b0 Ctrl= 11 ||Res= ffffffff Zero=0 Ovf=0 Neg=0
                200A= abcd4545 B= 12383588 Ctrl= 10 ||Res= 02080500 Zero=0 Ovf=0 Neg=0
                210A= abcd4545 B= 12383588 Ctrl= 11 ||Res= bbfd75cd Zero=0 Ovf=0 Neg=0
                220A= f0f0f0f0 B= cfcfcfcf Ctrl= 10 ||Res= c0c0c0c0 Zero=0 Ovf=0 Neg=0
                230A= f0f0f0f0 B= cfcfcfcf Ctrl= 11 ||Res= ffffffff Zero=0 Ovf=0 Neg=0
                240A= 00000000 B= 11111111 Ctrl= 10 ||Res= 00000000 Zero=1 Ovf=0 Neg=0
                250A= 00000000 B= 11111111 Ctrl= 11 ||Res= 11111111 Zero=0 Ovf=0 Neg=0
$finish called from file "ALU_fixture.v", line 96.
$finish at simulation time                  300
           V C S   S i m u l a t i o n   R e p o r t
Time: 300
CPU Time:      0.340 seconds;       Data structure size:   0.0Mb
Tue Feb 13 18:16:56 2018
```