SACRAMENTO STATE

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Course: EEE 273-Hierarchical Digital Design Methodology
Assignment Number: 5

```
module seq_detect(input x,clk,rst, output reg z);
reg[1:0] current_state, next_state;
parameter [1:0] IDLE = 2'b00, s0 = 2'b01, s1 = 2'b10;
always@(posedge clk , negedge rst)
begin
     if(!rst)   current_state <= IDLE;
     else       current_state <= next_state;
end
always@(*)
begin
next_state = IDLE;
     case(current_state)
          IDLE:
               begin
                    if(x)begin
                         next_state = s0; z = 1'b0;

                         end
                    else begin

                         next_state = IDLE; z = 1'b0;
                         end
               end
          s0:
               begin
                    if(!x)begin
                         next_state = s1; z = 1'b0;
                          end
                    else begin
                         next_state = s0; z = 1'b0;
                          end
               end
          s1:
               begin

                    if(x)begin
                         next_state = s0; z = 1'b1;
                          end
                    else begin
                         next_state = IDLE; z = 1'b0;
                          end
               end
          default: begin
                    next_state = IDLE; z = 1'b0;
                  end
     endcase
end
endmodule
```

```
#Read the design in
read_file -format verilog {"seqdetector.v"}

#set the current design
set current_design seq_detect

#Link the design
link

#create clockand constrain the design
create_clock "clk" -period 4     -name  "clk"
set_input_delay -clock clk  -max -rise 0.35 "x"
set_input_delay -clock clk  -min -rise 0.1 "x"
set_output_delay -clock clk  -max -rise 0.8 "z"
set_output_delay -clock clk  -min -rise 0.2 "z"

set_dont_touch_network  "clk"
set_max_area 0

#Set operating conditions
set_operating_conditions -library "saed90nm_typ" "TYPICAL"
#Synthesize and generate report
compile  -map_effort high -boundary_optimization
report_attribute >  report1
report_area >  report2
report_constraints -all_violators > report3
report_timing -path full -delay max -max_paths 1 -nworst 1  > report4
report_power  > report5
```

```
****************************************
Report : area
Design : seq_detect
Version: I-2013.12-SP5-4
Date   : Wed Apr  3 21:32:38 2019
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed90nm_typ (File:
/netdisk/tmp/saed/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/s
ynopsys/models/saed90nm_typ.db)

Number of ports:                            4
Number of nets:                             9
Number of cells:                            5
Number of combinational cells:              3
Number of sequential cells:                 2
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       4

Combinational area:                25.804800
Buf/Inv area:                       0.000000
Noncombinational area:             64.512001
Macro/Black Box area:               0.000000
Net Interconnect area:              1.472808

Total cell area:                   90.316801
Total area:                        91.789610
1
```

```
****************************************
Report : constraint
         -all_violators
Design : seq_detect
Version: I-2013.12-SP5-4
Date   : Wed Apr  3 21:32:38 2019
****************************************


   max_area

                              Required        Actual
   Design                       Area           Area           Slack
   -------------------------------------------------------------------
   seq_detect                   0.00           91.79         -91.79
(VIOLATED)


1
```

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : seq_detect
Version: I-2013.12-SP5-4
Date   : Wed Apr  3 21:32:38 2019
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: x (input port clocked by clk)
  Endpoint: z (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  seq_detect         ForQA                 saed90nm_typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.35       0.35 r
  x (in)                                   0.00       0.35 r
  U4/Q (AND3X1)                            0.09       0.44 r
  z (out)                                  0.00       0.44 r
  data arrival time                                   0.44

  clock clk (rise edge)                    4.00       4.00
  clock network delay (ideal)              0.00       4.00
  output external delay                   -0.80       3.20
  data required time                                  3.20
  -----------------------------------------------------------
  data required time                                  3.20
  data arrival time                                  -0.44
  -----------------------------------------------------------
  slack (MET)                                         2.76


1
```

```
Loading db file
'/netdisk/tmp/saed/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/
synopsys/models/saed90nm_typ.db'
Information: Propagating switching activity (low effort zero delay
simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : seq_detect
Version: I-2013.12-SP5-4
Date   : Wed Apr  3 21:32:39 2019
****************************************


Library(s) Used:

    saed90nm_typ (File:
/netdisk/tmp/saed/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/s
ynopsys/models/saed90nm_typ.db)


Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
seq_detect             ForQA             saed90nm_typ


Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 431.8464 nW   (66%)
  Net Switching Power  = 218.6200 nW   (34%)
                         ---------
Total Dynamic Power    = 650.4664 nW  (100%)

Cell Leakage Power     = 365.7343 nW


                 Internal         Switching           Leakage
Total
Power Group      Power            Power               Power
Power   (   %    )  Attrs
```

```
--------------------------------------------------------------------------
-------------------------
io_pad              0.0000            0.0000            0.0000
0.0000  (   0.00%)
memory              0.0000            0.0000            0.0000
0.0000  (   0.00%)
black_box           0.0000            0.0000            0.0000
0.0000  (   0.00%)
clock_network       0.0000            0.0000            0.0000
0.0000  (   0.00%)
register            0.1517            0.1712        2.4295e+05
0.5658  (  55.68%)
sequential          0.0000            0.0000            0.0000
0.0000  (   0.00%)
combinational       0.2801        4.7436e-02        1.2278e+05
0.4504  (  44.32%)
--------------------------------------------------------------------------
-------------------------
Total               0.4318 uW         0.2186 uW     3.6573e+05 pW
1.0162 uW
1
```