```
`include "ALU.v"
module ALU_Fixture;
parameter size = 32;   //Changing Parameter default size
//Declartion of input reg
reg signed[size-1 : 0]A;
reg signed[size-1 : 0]B;
reg [1:0]ctrl;
//Delcaration of Output wire
wire signed[size-1 : 0]R;
wire O,N,Z;
initial
$monitor($time," A= %h   B= %h   ctrl= %b   Result= %h   O= %b   N= %b
Z= %b\n\n",A,B,ctrl,R[size-1 : 0],O,N,Z);        //Monitor when there is
a change in time
//Dot notation of Instances
ALU  #(.size(32)) (.A(A),.B(B),.R(R),.ctrl(ctrl),.O(O),.N(N),.Z(Z));
initial
begin
A = 32'hFFFFF000;       // Input Test vectors
           B = 32'hFFFFFFFF;
           ctrl = 2'b00;          //ctrl bit operation
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFF;
           B = 32'h000F00FF;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'h67676767;
           B = 32'h12431243;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hAAAAAAAA;
           B = 32'hEFABCD19;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFF;
           B = 32'h00000001;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFF;
           B = 32'hFFFFFFFF;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFC;
           B = 32'hFFFFFFFC;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFF0000;
```

```
            B = 32'h00001342;
            ctrl = 2'b00;
      #10   ctrl = 2'b01;

      #10   A = 32'h01234567;
            B = 32'h00080808;
            ctrl = 2'b00;
      #10   ctrl = 2'b01;

      #10   A = 32'hFFFFFFFF;
            B = 32'h0A0AB0B0;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;

      #10   A = 32'hABCD4545;
            B = 32'h12383588;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;

      #10   A = 32'hF0F0F0F0;
            B = 32'hCFCFCFCF;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;

      #10   A = 32'h00000000;
            B = 32'h11000001;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;


end
initial
begin
      #500  $finish;
end
endmodule
```