```
module sync_rd2wr #(parameter width =8, depth = 7)
(input[depth:0] rptr,input clk_in,reset,flush, output reg[depth:0]
r2wsync_ff2);
reg [depth:0] r2wsync_ff1;

always @(posedge clk_in, negedge reset)
begin
      if(!reset)
      begin
            r2wsync_ff2 <= 0 ;
            r2wsync_ff1 <= 0 ;
      end
      else
      begin    //$display("b4syn r2w",rptr );
            r2wsync_ff1 <= rptr ;
            r2wsync_ff2 <= r2wsync_ff1;//$display("aftr syn
r2w",r2wsync_ff2 );
      end
end

endmodule
```