```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : seq_detect
Version: I-2013.12-SP5-4
Date   : Mon Apr  1 12:37:43 2019
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: x (input port clocked by clk)
  Endpoint: current_state_reg[1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  seq_detect         ForQA                 saed90nm_typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.10       0.10 r
  x (in)                                   0.00       0.10 r
  U5/QN (NOR3X0)                           0.10       0.20 f
  current_state_reg[1]/D (DFFARX1)         0.03       0.23 f
  data arrival time                                   0.23

  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  current_state_reg[1]/CLK (DFFARX1)       0.00       0.00 r
  library hold time                       -0.01      -0.01
  data required time                                 -0.01
  -----------------------------------------------------------
  data required time                                 -0.01
  data arrival time                                  -0.23
  -----------------------------------------------------------
  slack (MET)                                         0.25


1
```