```
module seq_detect(input x,clk,rst, output reg z);
reg[1:0] current_state, next_state;
parameter [1:0] IDLE = 2'b00, s0 = 2'b01, s1 = 2'b10;
always@(posedge clk , negedge rst)
begin
     if(!rst)   current_state <= IDLE;
     else       current_state <= next_state;
end
always@(*)
begin
next_state = IDLE;
     case(current_state)
          IDLE:
               begin
                    if(x)begin
                         next_state = s0; z = 1'b0;

                         end
                    else begin

                         next_state = IDLE; z = 1'b0;
                         end
               end
          s0:
               begin
                    if(!x)begin
                         next_state = s1; z = 1'b0;
                          end
                    else begin
                         next_state = s0; z = 1'b0;
                          end
               end
          s1:
               begin

                    if(x)begin
                         next_state = s0; z = 1'b1;
                          end
                    else begin
                         next_state = IDLE; z = 1'b0;
                          end
               end
          default: begin
                    next_state = IDLE; z = 1'b0;
                  end
     endcase
end
endmodule
```