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Report : Attribute
Design : seq_detect
Version: I-2013.12-SP5-4
Date   : Sat Mar 30 15:33:12 2019
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Design	Object	Type	Attribute Name	Value
seq_detect	seq_detect	design	compile_tot_wall_time	1.883734
seq_detect	seq_detect	design	compile_cpu_hostname	olympia
seq_detect	seq_detect	design	ice_canonical_xor2_delay	0.079115
seq_detect	seq_detect	design	ice_canonical_nand2_delay	0.029236
seq_detect	seq_detect	design	testdb_meth_sig_usage_option	98307
seq_detect	seq_detect	design	testdb_meth_sig_usage	106499
seq_detect	seq_detect	design	testdb_meth_name	multiplexed_flip_flop
seq_detect	seq_detect	design	bs_mux_cost	20.000000
seq_detect	seq_detect	design	pads_thru_hier	false
seq_detect	seq_detect	design	pads_respect_hier	false
seq_detect	seq_detect	design	map_effort_option	3
seq_detect	seq_detect	design	instance_name_suffix	
seq_detect	seq_detect	design	compile_tdrs_cpu_time	0.014000
seq_detect	seq_detect	design	compile_lib_cpu_time	0.322951
seq_detect	seq_detect	design	compile_tot_cpu_time	1.075836
seq_detect	seq_detect	design	compile_rbo_cpu_time	0.216967
seq_detect	seq_detect	design	compile_abo_cpu_time	0.110985
seq_detect	seq_detect	design	temperature_from_min_lib	25.000000
seq_detect	seq_detect	design	temperature_from_max_lib	25.000000
seq_detect	seq_detect	design	max_area	0.000000
seq_detect	seq_detect	design	design_voltage_unit	1000.000000
seq_detect	seq_detect	design	design_current_unit	0.001000
seq_detect	seq_detect	design	design_resistance_unit	999.999939
seq_detect	seq_detect	design	design_cap_unit	0.001000
seq_detect	seq_detect	design	design_time_unit	1.000000
seq_detect	seq_detect	design	ungroup_all_option	false
seq_detect	seq_detect	design	scan_state_route_serial	false

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seq_detect      seq_detect          design    scan_state_route_clocks   false
seq_detect      seq_detect          design    scan_state_route_enables  false
seq_detect      seq_detect          design    map                       true
seq_detect      seq_detect          design    exact_sequential_map      false
seq_detect      seq_detect          design    redundancy_removal        true
seq_detect      seq_detect          design    scan_state_type           1
seq_detect      seq_detect          design    min_wire_load_selection_type
                                                                        0
seq_detect      seq_detect          design    wire_load_selection_type  6
seq_detect      seq_detect          design    hdl_library               WORK
seq_detect      seq_detect          design    hdl_template              seq_detect
seq_detect      seq_detect          design    hdl_canonical_default_params
                                                                        IDLE=2'h0,s0=2'h1,s1=2'h2
seq_detect      seq_detect          design    hdl_default_parameters    IDLE => 2'h0, s0 => 2'h1, s1 =>
2'h2
seq_detect      seq_detect          design    hdl_canonical_params
seq_detect      seq_detect          design    hdl_parameters
seq_detect      seq_detect          design    link_design_libraries     WORK, DEFAULT
seq_detect      seq_detect          design    presto_gtech_count        17
seq_detect      current_state_reg[0]
                                    cell      ff_edge_sense             1
seq_detect      current_state_reg[1]
                                    cell      ff_edge_sense             1
seq_detect      clk                 net       net_original_name         clk
seq_detect      current_state[1]    net       net_original_name         current_state[1]
seq_detect      next_state[0]       net       net_original_name         next_state[0]
seq_detect      next_state[1]       net       net_original_name         next_state[1]
seq_detect      rst                 net       net_original_name         rst
seq_detect      x                   net       net_original_name         x
seq_detect      z                   net       net_original_name         z
seq_detect      current_state_reg[1]/CLK
                                    pin       pin_on_clock_network_per_scn
                                                                        true
seq_detect      current_state_reg[0]/CLK
                                    pin       pin_on_clock_network_per_scn
                                                                        true
seq_detect      clk                 port      pin_on_clock_network_per_scn
                                                                        true
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