```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : seq_detect
Version: I-2013.12-SP5-4
Date   : Sat Mar 30 15:33:12 2019
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: x (input port clocked by clk)
  Endpoint: z (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  seq_detect         ForQA                 saed90nm_typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  input external delay                     0.35       0.35 r
  x (in)                                   0.00       0.35 r
  U4/Q (AND3X1)                            0.09       0.44 r
  z (out)                                  0.00       0.44 r
  data arrival time                                   0.44

  clock clk (rise edge)                    4.00       4.00
  clock network delay (ideal)              0.00       4.00
  output external delay                   -0.80       3.20
  data required time                                  3.20
  -----------------------------------------------------------
  data required time                                  3.20
  data arrival time                                  -0.44
  -----------------------------------------------------------
  slack (MET)                                         2.76


1
```