Timing Report for clk_in=2 and clk_out-2

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****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fifo
Version: I-2013.12-SP5-4
Date   : Tue Apr 30 00:08:06 2019
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: r2w1/r2wsync_ff2_reg[3]
              (rising edge-triggered flip-flop clocked by clk_in)
  Endpoint: w1/wptr_reg[3]
            (rising edge-triggered flip-flop clocked by clk_in)
  Path Group: clk_in
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fifo               280000                saed90nm_typ
  write_logic_depth7_width8
                     8000                  saed90nm_typ

  Point                                                    Incr       Path
  ------------------------------------------------------------------------
---
  clock clk_in (rise edge)                                 0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  r2w1/r2wsync_ff2_reg[3]/CLK (DFFARX1)                    0.00       0.00
r
  r2w1/r2wsync_ff2_reg[3]/Q (DFFARX1)                      0.17       0.17
r
  r2w1/r2wsync_ff2[3] (sync_rd2wr_width8_depth7)           0.00       0.17
r
  w1/r2wsync_ff2[3] (write_logic_depth7_width8)            0.00       0.17
r
  w1/U92/Q (XOR2X1)                                        0.94       1.11
r
  w1/U96/Q (OR4X1)                                         0.15       1.26
r
  w1/U100/QN (NOR4X0)                                      0.11       1.37
f
  w1/U84/QN (NAND2X0)                                      0.09       1.46
r
  w1/U83/Q (AND3X1)                                        0.14       1.60
r
  w1/U79/Q (OA21X1)                                        0.13       1.74
r
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  w1/U55/Q (AO22X1)                                       0.12       1.85
r
  w1/wptr_reg[3]/D (DFFARX1)                              0.03       1.89
r
  data arrival time                                                  1.89

  clock clk_in (rise edge)                                2.00       2.00
  clock network delay (ideal)                             0.00       2.00
  w1/wptr_reg[3]/CLK (DFFARX1)                            0.00       2.00
r
  library setup time                                     -0.09       1.91
  data required time                                                 1.91
  ------------------------------------------------------------------------
---
  data required time                                                 1.91
  data arrival time                                                 -1.89
  ------------------------------------------------------------------------
---
  slack (MET)                                                        0.03


  Startpoint: w2r1/w2rsync_ff2_reg[3]
              (rising edge-triggered flip-flop clocked by clk_out)
  Endpoint: r1/read_addr_reg[1]
            (rising edge-triggered flip-flop clocked by clk_out)
  Path Group: clk_out
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fifo               280000                saed90nm_typ
  read_logic_depth7_width8
                     8000                  saed90nm_typ

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
---
  clock clk_out (rise edge)                               0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  w2r1/w2rsync_ff2_reg[3]/CLK (DFFARX1)                   0.00       0.00
r
  w2r1/w2rsync_ff2_reg[3]/Q (DFFARX1)                     0.17       0.17
r
  w2r1/w2rsync_ff2[3] (sync_wr2rd_width8_depth7)          0.00       0.17
r
  r1/w2rsync_ff2[3] (read_logic_depth7_width8)            0.00       0.17
r
  r1/U66/ZN (INVX0)                                       0.46       0.63
f
  r1/U4/Q (XNOR2X2)                                       0.16       0.79
f
  r1/U43/Q (AND4X1)                                       0.14       0.92
f
```

```
  r1/U92/QN (NAND4X0)                                     0.09       1.02
r
  r1/U102/QN (NOR2X0)                                     0.10       1.11
f
  r1/U28/QN (NOR2X0)                                      0.10       1.22
r
  r1/U26/Q (AO21X1)                                       0.13       1.35
r
  r1/U70/Q (AO22X1)                                       0.13       1.48
r
  r1/read_addr_reg[1]/D (DFFARX1)                         0.03       1.51
r
  data arrival time                                                  1.51

  clock clk_out (rise edge)                               1.00       1.00
  clock network delay (ideal)                             0.00       1.00
  r1/read_addr_reg[1]/CLK (DFFARX1)                       0.00       1.00
r
  library setup time                                     -0.09       0.91
  data required time                                                 0.91
  ------------------------------------------------------------------------
---
  data required time                                                 0.91
  data arrival time                                                 -1.51
  ------------------------------------------------------------------------
---
  slack (VIOLATED)                                                  -0.60


1
```