```
`include "seqdetector.v";
module seqdetector_fixture;
reg x,clk,rst;
reg [31:0]in;
wire Z;
integer i;
seq_detect U1(.x(x), .Z(Z), .clk(clk), .rst(rst));
initial
      $monitor($time," X = %b , Z = %b ,reset = %b\n",x,Z,rst);
initial
        $vcdpluson;
initial begin
in = 32'b10110101010101010010101010111011;
      for(i=0;i<32;i=i+1) begin
            @(posedge clk) x = in[i];end
end
initial
begin
        rst = 1'b1;x = 1'b1;
      #80 rst = 1'b0;
      #70 rst = 1'b1;
      #100 rst = 1'b0;
end
initial
begin
       clk = 1'b1;
       forever #5 clk = ~clk;
end

initial
begin
       #800 $finish;
end
endmodule
```