SACRAMENTO STATE

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Course: EEE 273-Hierarchical Digital Design Methodology
Assignment Number: 2
Date Submitted: 8th Feb 2019
Due Date: 11th Feb 2019 by 11:59pm

```
module ALU #(parameter size = 16) (A,B,ctrl,R,O,N,Z);    //Declaration of
default parameter size and port names
//Delclaring input ports
input [size-1 : 0]A, B;
input [1:0]ctrl;
//Delclaring output ports
output [size-1 : 0] R;
output O, N, Z;
//Delcaring registers
reg signed [size-1 : 0] R;
reg O,N,Z;
always @(*)    // * denotes a change in any variables
begin
case(ctrl)      //ctrl bit denotes the operation to be performed
      2'b00:
      begin
            R = A + B;       //Result
            N = R[size-1];         //Sign Flag
            O = (((~A[size-1]) & (~B[size-1]) & (R[size-1])) | ((A[size-
1]) & (B[size-1]) & (~R[size-1])));          // Overflow Flag
      end
      2'b01:
      begin
            R = A - B;
            N = R[size-1];
            O = (((~A[size-1]) & (B[size-1]) & (R[size-1])) | ((A[size-
1]) & (~B[size-1]) & (~R[size-1])));
      end
      2'b10:
      begin
            R = A & B;
      end
      2'b11:
      begin
            R = A | B;
      end
endcase;
if(R==0)         //Conditions for Zero Flag
begin
      O=1'b0;
      Z=1'b1;
end
else
      Z=1'b0;
end
endmodule
```

```
`include "ALU.v"
module ALU_Fixture;
parameter size = 32;  //Changing Parameter default size
//Declartion of input reg
reg signed[size-1 : 0]A;
reg signed[size-1 : 0]B;
reg [1:0]ctrl;
//Delcaration of Output wire
wire signed[size-1 : 0]R;
wire O,N,Z;
initial
$monitor($time," A= %h   B= %h   ctrl= %b   Result= %h   O= %b   N= %b
Z= %b\n\n",A,B,ctrl,R[size-1 : 0],O,N,Z);        //Monitor when there is
a change in time
//Dot notation of Instances
ALU a1(.A(A),.B(B),.R(R),.ctrl(ctrl),.O(O),.N(N),.Z(Z));
initial
begin
A = 32'hFFFFF000;       // Input Test vectors
           B = 32'hFFFFFFFF;
           ctrl = 2'b00;          //ctrl bit operation
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFF;
           B = 32'h000F00FF;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'h67676767;
           B = 32'h12431243;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hAAAAAAAA;
           B = 32'hEFABCD19;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFF;
           B = 32'h00000001;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFF;
           B = 32'hFFFFFFFF;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFFFFFC;
           B = 32'hFFFFFFFC;
           ctrl = 2'b00;
      #10  ctrl = 2'b01;

      #10  A = 32'hFFFF0000;
```

```
            B = 32'h00001342;
            ctrl = 2'b00;
      #10   ctrl = 2'b01;

      #10   A = 32'h01234567;
            B = 32'h00080808;
            ctrl = 2'b00;
      #10   ctrl = 2'b01;

      #10   A = 32'hFFFFFFFF;
            B = 32'h0A0AB0B0;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;

      #10   A = 32'hABCD4545;
            B = 32'h12383588;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;

      #10   A = 32'hF0F0F0F0;
            B = 32'hCFCFCFCF;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;

      #10   A = 32'h00000000;
            B = 32'h11000001;
            ctrl = 2'b10;
      #10   ctrl = 2'b11;


end
initial
begin
      #500  $finish;
end
endmodule
```

```
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Feb 12 15:38 2019
                   0 A= fffff000   B= ffffffff   ctrl= 00   Result= ffffefff   O= 0   N= 1   Z= 0

                  10 A= fffff000   B= ffffffff   ctrl= 01   Result= fffff001   O= 0   N= 1   Z= 0

                  20 A= ffffffff   B= 000f00ff   ctrl= 00   Result= 000000fe   O= 0   N= 0   Z= 0

                  30 A= ffffffff   B= 000f00ff   ctrl= 01   Result= ffffff00   O= 0   N= 1   Z= 0

                  40 A= 67676767   B= 12431243   ctrl= 00   Result= 000079aa   O= 0   N= 0   Z= 0

                  50 A= 67676767   B= 12431243   ctrl= 01   Result= 00005524   O= 0   N= 0   Z= 0

                  60 A= aaaaaaaa   B= efabcd19   ctrl= 00   Result= 000077c3   O= 1   N= 0   Z= 0

                  70 A= aaaaaaaa   B= efabcd19   ctrl= 01   Result= ffffdd91   O= 0   N= 1   Z= 0

                  80 A= ffffffff   B= 00000001   ctrl= 00   Result= 00000000   O= 0   N= 0   Z= 1

                  90 A= ffffffff   B= 00000001   ctrl= 01   Result= fffffffe   O= 0   N= 1   Z= 0

                 100 A= ffffffff   B= ffffffff   ctrl= 00   Result= fffffffe   O= 0   N= 1   Z= 0

                 110 A= ffffffff   B= ffffffff   ctrl= 01   Result= 00000000   O= 0   N= 0   Z= 1
```

```
120 A= fffffffc   B= fffffffc   ctrl= 00   Result= fffffff8   O= 0   N= 1   Z= 0

130 A= fffffffc   B= fffffffc   ctrl= 01   Result= 00000000   O= 0   N= 0   Z= 1

140 A= ffff0000   B= 00001342   ctrl= 00   Result= 00001342   O= 0   N= 0   Z= 0

150 A= ffff0000   B= 00001342   ctrl= 01   Result= ffffecbe   O= 0   N= 1   Z= 0

160 A= 01234567   B= 00080808   ctrl= 00   Result= 00004d6f   O= 0   N= 0   Z= 0

170 A= 01234567   B= 00080808   ctrl= 01   Result= 00003d5f   O= 0   N= 0   Z= 0

180 A= ffffffff   B= 0a0ab0b0   ctrl= 10   Result= ffffb0b0   O= 0   N= 0   Z= 0

190 A= ffffffff   B= 0a0ab0b0   ctrl= 11   Result= ffffffff   O= 0   N= 0   Z= 0

200 A= abcd4545   B= 12383588   ctrl= 10   Result= 00000500   O= 0   N= 0   Z= 0

210 A= abcd4545   B= 12383588   ctrl= 11   Result= 000075cd   O= 0   N= 0   Z= 0

220 A= f0f0f0f0   B= cfcfcfcf   ctrl= 10   Result= ffffc0c0   O= 0   N= 0   Z= 0

230 A= f0f0f0f0   B= cfcfcfcf   ctrl= 11   Result= ffffffff   O= 0   N= 0   Z= 0

240 A= 00000000   B= 11000001   ctrl= 10   Result= 00000000   O= 0   N= 0   Z= 1
```

```
                250 A= 00000000   B= 11000001   ctrl= 11   Result= 00000001   O= 0   N= 0   Z= 0


$finish called from file "ALU_fixture.v", line 87.
$finish at simulation time                  500
          V C S   S i m u l a t i o n   R e p o r t
Time: 500
CPU Time:      0.340 seconds;       Data structure size:   0.0Mb
Tue Feb 12 15:38:57 2019
```