SACRAMENTO STATE

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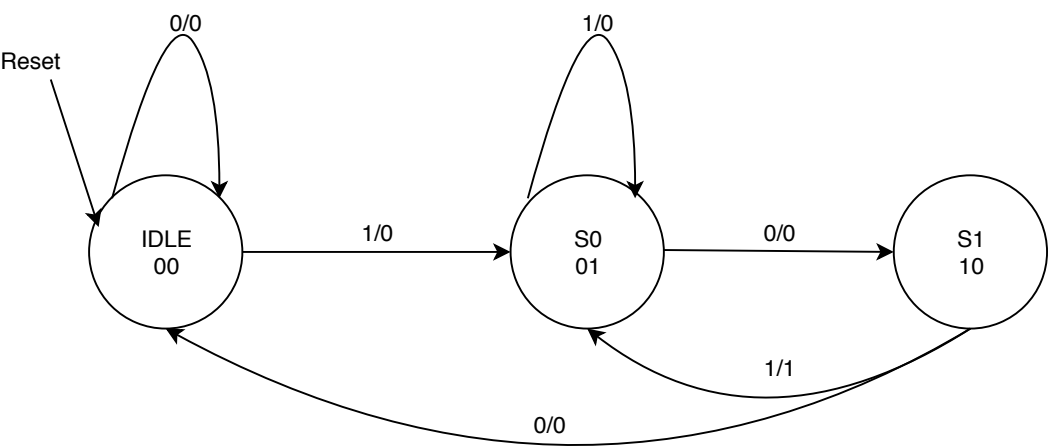
Course: EEE 273-Hierarchical Digital Design Methodology
Assignment Number: 3


Reset
0/0
IDLE
00
1/0
1/0
S0
01
0/0
S1
10
1/1
0/0

```
module seq_detect(input x,clk,rst, output reg Z);
reg[1:0] current_state, next_state;
parameter [1:0] IDLE = 2'b00, s0 = 2'b01, s1 = 2'b10;
always@(posedge clk , negedge rst)
begin
      if(!rst)    current_state <= IDLE;
      else        current_state <= next_state;
end
always@(*)
begin
next_state = IDLE;
      case(current_state)
            IDLE:
                  begin
                        if(x)begin
                              next_state = s0; Z = 1'b0;
                             end
                        else begin
                              next_state = IDLE; Z = 1'b0;
                             end
                  end
            s0:
                  begin
                        if(!x)begin
                              next_state = s1; Z = 1'b0;
                              end
                        else begin
                              next_state = s0; Z = 1'b0;
                              end
                  end
            s1:
                  begin

                        if(x)begin
                              next_state = s0; Z = 1'b1;
                              end
                        else begin
                              next_state = IDLE; Z = 1'b0;
                              end
                  end
            default: begin
                        next_state = IDLE; Z = 1'b0;
                     end
      endcase
end
endmodule
```

```
`include "seqdetector.v";
module seqdetector_fixture;
reg x,clk,rst;
reg [31:0]in;
wire Z;
integer i;
seq_detect U1(.x(x), .Z(Z), .clk(clk), .rst(rst));
initial
      $monitor($time," X = %b , Z = %b ,reset = %b\n",x,Z,rst);
initial
        $vcdpluson;
initial begin
in = 32'b10110101010101010010101010111011;
      for(i=0;i<32;i=i+1) begin
            @(posedge clk) x = in[i];end
end
initial
begin
        rst = 1'b1;x = 1'b1;
      #80 rst = 1'b0;
      #70 rst = 1'b1;
      #100 rst = 1'b0;
end
initial
begin
       clk = 1'b1;
       forever #5 clk = ~clk;
end

initial
begin
       #800 $finish;
end
endmodule
```

```
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Feb 22 18:04
2019
VCD+ Writer I-2014.03-2 Copyright (c) 1991-2014 by Synopsys Inc.
                   0 X = 1 , Z = 0 ,reset = 1

                  20 X = 0 , Z = 0 ,reset = 1

                  30 X = 1 , Z = 1 ,reset = 1

                  40 X = 1 , Z = 0 ,reset = 1

                  60 X = 0 , Z = 0 ,reset = 1

                  70 X = 1 , Z = 1 ,reset = 1

                  80 X = 0 , Z = 0 ,reset = 0

                  90 X = 1 , Z = 0 ,reset = 0

                 100 X = 0 , Z = 0 ,reset = 0

                 110 X = 1 , Z = 0 ,reset = 0

                 120 X = 0 , Z = 0 ,reset = 0

                 130 X = 1 , Z = 0 ,reset = 0

                 140 X = 0 , Z = 0 ,reset = 0

                 150 X = 0 , Z = 0 ,reset = 1

                 160 X = 1 , Z = 0 ,reset = 1

                 170 X = 0 , Z = 0 ,reset = 1

                 180 X = 1 , Z = 1 ,reset = 1

                 190 X = 0 , Z = 0 ,reset = 1

                 200 X = 1 , Z = 1 ,reset = 1

                 210 X = 0 , Z = 0 ,reset = 1

                 220 X = 1 , Z = 1 ,reset = 1

                 230 X = 0 , Z = 0 ,reset = 1

                 240 X = 1 , Z = 1 ,reset = 1

                 250 X = 0 , Z = 0 ,reset = 0

                 260 X = 1 , Z = 0 ,reset = 0
```

```
                270 X = 0 , Z = 0 ,reset = 0

                280 X = 1 , Z = 0 ,reset = 0

                300 X = 0 , Z = 0 ,reset = 0

                310 X = 1 , Z = 0 ,reset = 0

$finish called from file "seqdetector_fixture.v", line 32.
$finish at simulation time                  800
           V C S   S i m u l a t i o n   R e p o r t
Time: 800
CPU Time:      0.350 seconds;       Data structure size:   0.0Mb
Fri Feb 22 18:04:09 2019
```