```
read_file -format verilog {"fifo.v"}
analyze  -format verilog {fifo.v}
elaborate fifo -architecture verilog
set current_design fifo
link
create_clock "clk_in" -period 1 -name "clk_in"
set_input_delay -clock clk_in -max -rise 0.4 "insert"
set_input_delay -clock clk_in -min -rise 0.2 "insert"
set_input_delay -clock clk_in -max -rise 0.4 "flush"
set_input_delay -clock clk_in -min -rise 0.2 "flush"
set_input_delay -clock clk_in -max -rise 0.4 "data_in"
set_input_delay -clock clk_in -min -rise 0.2 "data_in"
set_output_delay -clock clk_in -max -rise 0.4 "full"
set_output_delay -clock clk_in -min -rise 0.2 "full"
create_clock "clk_out" -period 2 -name "clk_out"
set_input_delay -clock clk_out -max -rise 0.4 "remove"
set_input_delay -clock clk_out -min -rise 0.2 "remove"
set_output_delay -clock clk_out -max -rise 0.4 "empty"
set_output_delay -clock clk_out -min -rise 0.2 "empty"
set_output_delay -clock clk_out -max -rise 0.4 "data_out"
set_output_delay -clock clk_out -min -rise 0.2 "data_out"
set_dont_touch_network "clk_in"
set_dont_touch_network "clk_out"
set_max_area 0
set_false_path -from [get_clocks {clk_in}] -to [get_clocks {clk_out}]
set_operating_conditions -library "saed90nm_typ" "TYPICAL"
compile -map_effort high -boundary_optimization
report_attribute > report1
report_area > report2
report_constraints -all_violators > report3
report_timing -path full -delay max -max_paths 1 -nworst 1 > report4
report_timing -path full -delay min -max_paths 1 -nworst 1 > report5
```