CSc/EEE 273
Term Project Status Report
Team 10.

Names	*Signatures*	*Overall Grade*
1 Karthik Mallappahalli Shekarappa		
2 Sreelekha Mittai		
3		

Provide the required information as accurately as possible based on the status of your FIFO submitted on the due date. The completed form must appear after Table of Contents (TOC) in your report.

I. Project Report / Demo / 200 points

Table 1: (*To be filled by the instructor*)

Item in the report	Issues	points
Cover sheet		
TOC		
Project Status Report		
Block diagrams for the DUT and Testbench		
FSM diagrams		
Source code		
Test bench • DUT instant • Model • Automated validation • Simulation results (submitted as part of the softcopy only)		
Synthesis 1. Script 2. Synthesis report 3. check_design report		
Tabulated area and timing results		
Synthesis reports		
Code Coverage results		

VALIDITY OF RESULTS IN THE REPORT		

II.Design and Modeling Phase: /550 points

Table 2. Source code: Comment on the functionality of the source code you developed for each component of the FIFO as accurately as possible. The comments you provide here must be based on your simulation results. Add more rows as needed. (300 points)

Component	Name of the person who modeled and validated the component	Is this component fully functional?	State any functional issue
memory.v	Sreelekha Mittai	Yes	
Read_logic.v	Sreelekha Mittai	Yes	Does not support insert after full
Write_logic.v	Karthik MS	yes	Does not support remove after flush or reset
Syncrd2wr.v	Karthik MS	Yes	
Syncwr2rd.v	Karthik MS	Yes	
Fifo.v	Sreelekha Mittai	Yes	

Table 3 Top-level Design. Comment on the functionality of the FIFO you developed (The functionality of the top-level design). 250 points

State functional issues in DUT	Does not support insert after full and remove after flush or reset
State functional issues in the testbench	NONE

Table 4. Code Coverage: Fill the following table based on the coverage reports vcs generated for your FIFO design for applicable options.

Coverage Type	Percentage	Comments if any
Line	96.60	
Toggle	97.68	

Conditional	100	
FSM	100	

III. Synthesis: 25 % 250 points

Table 5. Fill out the following table based on your best synthesis trials: timing & area. In each case, state the sign of the timing and area parameters as provided by the Design Compiler tool. The first row is a summary your results based on given clock rates. You should use the following constrains in all synthesis attempts using high synthesis effort:

Max input/output delay based on clk_in	0.4ns
Min input/output delay based on clk_in	0.2 ns
Max input/output delay based on clk_out	0.4ns
Min input/output delay based on clk_out	0.2ns

You must provide synthesis results based on the clock frequencies listed for Trails 1and 2 listed below. You can list successful synthesis attempts at other frequencies under Trials 3 and 4. These attempts should be based on enhancements to RTL code to improve synthesis results.

Trial	Clk_in Period in ns	Clk_out Period in ns	Area slack from area report	Timing slack from timing report	data required time for max path from timing report	data arrival time for the max path from timing report path
1	**2 ns**	**1 ns**	**193710.326746**	**Clk_in = 0.02** **Clk_out = -0.53**	**Clk_in = 1.92** **Clk_out = 0.91**	**Clk_in = 1.90** **Clk_out = 1.44**
2	**1ns**	**2ns**	**247763.181569**	**Clk_in = -0.63** **Clk_out = 0.01**	**Clk_in = 0.91** **Clk_out = 1.92**	**Clk_in = 1.55** **Clk_out = 1.9**
3	**1.65ns**	**3.3ns**	**247375.501146**	**Clk_in = 0.00** **Clk_out = 0.31**	**Clk_in = 1.56** **Clk_out = 3.24**	**Clk_in = 1.56** **Clk_out = 2.94**
4	**1.6ns**	**3ns**	**247587.944318**	**Clk_in = 0.00** **Clk_out = 0.41**	**Clk_in = 1.51** **Clk_out = 3.11**	**Clk_in = 1.51** **Clk_out = 2.70**

Briefly describe any RTL changes you made to improve synthesis results.

Trial 3: Changed frequency in synthesis script for different iterations to meet slack

Trial 4: We used one hot for state representation and then used different iteration to meet Timing Slack at clk_in 1.6ns and clk_out 3.2 ns.

Tables 6: For each partner, state the contribution percentage for each task listed below: Please only provide a percentage.

Name	Design	Simulation	Synthesis	Project report
Sreelekha Mittai	49%	49%	51%	54%
Karthik M Shekarappa	51%	51%	49%	46%