

IV B.Tech I Semester Supplementary Examinations, February- 2020
SYSTEM DESIGN THROUGH VERILOG
(Electronics and Communication Engineering)

Time: 3 hours**Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any FOUR questions from Part-B************PART-A(14 Marks)**

1. a) Compare synthesis and simulation. [2]
- b) Draw the truth table of AND gate primitive. [3]
- c) Write the syntax of intra assignment delay. [2]
- d) Write the syntax of an AND gate in dataflow format and write its test bench. [2]
- e) What is continuous assignment synthesis? [2]
- f) Explain memory operators? [3]

PART-B(4x14 = 56 Marks)

2. a) Write a short notes on [14]
 (i) strengths (ii)parameters (iii) operators (iv) system tasks
3. a) Design all 4 types of tri state buffers, write its VERILOG code and test bench. [7]
 b) Explain design of Flip flops with gate primitives. [7]
4. Write the syntax of (i) for loop (ii) disable construct (iii) while loop with [14]
 suitable examples and test benches.
5. a) Design an edge triggered flip flop through continuous assignments for the gates [7]
 and write its test bench.
 b) Write VERILOG code for AOI gate and its test bench. [7]
6. a) Explain simple latch with Verilog module. [6]
 b) Design Verilog module of an edge triggered flip flop built with the latch. [8]
7. Write a Verilog description for SRAM and implement it. [14]

