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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – CAT-2

Course Code: ECE2002 | **Course Title: Computer Organization and Architecture**

Set number: 1 | **Date of Exam:** 28/03/2023 (AN) (B2)

Duration: 90 min | **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Discuss the addressing modes of 8086 with suitable examples. **(15M)**

Q2. What is RS232 protocol? Discuss the working of RS232 hardware and software handshaking process. **(10M)**

Q3. Calculate the effective address of the memory location:

a) When the data is stored at 2222 H : 0016 H

b) After the following operation MOV AX, 2000H [BX] [SI] **(10M)**

Q4. The 8 bytes of data are stored from memory location 0200H to 0207H in the segment 5000H. Write a program to transfer the block of data and store it in reverse direction to location 0400H to 0407H in the segment 5000H. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1,2,3,5	2	1	15
Q2	3	3	1,2,3,5	1,2	1	10
Q3	3	3	1,2,3,5	1,2	1	10
Q4	3	3	1,2,3,5	2	1	15

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – CAT-2

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 4 **Date of Exam:** 28/03/2023 (FN) (B1)

Duration: 90 Minutes **Total Marks:** 50 Marks

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.
3. Draw the necessary diagrams.
4. Underline the important points, titles, and subtitles.

Q1. Explain all addressing modes of 8086 with examples. **(15M)**

Q2. State and explain the different instruction formats of 8086. **(15M)**

Q3. Write a program to sort an 8-bit data array in ascending order. The array consists of 5 numbers starting from location 3000H: 4000H. **(10M)**

Q4. Explain the different types of Interrupt signals with standard format for microprocessors 8086. **(10M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1	1	1	15
Q2	3	3	2	2	2	15
Q3	3	3	3	2	2	10
Q4	3	3	3	2	2	10

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – CAT-2

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 6 **Date of Exam:** 29/03/2023 (AN) (C2)

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Write an Assembly Language Programming (ALP) to find factorial of Ten(10) for 8086. **(10M)**

Q2. What are the components of an RS232 system? How does RS232 communication work? **(10M)**

Q3. Discuss the architecture of 8086 with the proper diagram. Mention the total number of registers of 8086 and show the manner in which they are grouped. **(15M)**

Q4. What are various addressing modes? Explain with help of suitable example. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1,2,3	2	3	10
Q2	3	3	1,2	1	1	10
Q3	3	3	2	1	1	15
Q4	3	3	1	1	1	15

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QUESTION PAPER

Name of the Examination: WINTER SEMESTER (2022-2023) - CAT-2

Course Code: ECE2002 **Course Title:** Computer Organization & Architecture

Set Number: 7 **Date of Exam:** 27/03/2023 (AN) (A2)

Duration: 90 min **Total Marks:** 50 Marks

Instructions:

(1) All questions are compulsory.
(2) Assume data wherever necessary.
(3) Any assumptions made should be clearly stated.

Q1. Discuss the need of handshaking protocol in a communication process. With suitable diagram explain the handshaking involved within RS-232 protocol. **(10 Marks)**

Q2. What are Interrupts and Interrupt Service Routine in 8086 architecture?. With a suitable example, explain the procedure adopted to handle the user defined interrupts within 8086 microprocessor. **(10 Marks)**

Q3. Explain the methodology used to decode the assemble language programs within 8086 microprocessor. Give examples to support the diversity present in decoding the instructions using the above methodology. **(15 Marks)**

Q4. Write an effective 8086 assemble language program to implement the following function:

$$F(x, y) = x! + y!$$

where, {x, y} are the 8-bit binary numbers stored at memory location 1020H and 2010H, and {x!, y!} are their respective factorials. Additionally, store the resultant function value at a memory location 3020H. **(15 Marks)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1,2,3,5	1,2	1	10
Q2	3	3	1,2,3,5	1,2	1	10
Q3	3	3	1,2,3,5	1,2	1	15
Q4	3	3	1,2,3,5	1,2	1	15

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QUESTION PAPER

Name of the Examination: CAT-2 (Fall Semester 2023-2024)

Course Code: ECE2002 **Course Title:** computer architecture and organization

Slot: 01 **Date of Exam:** 17/10/2023 (AN)

Duration: 90 min **Total Marks: 50** (C2)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. The 16 data bytes are stored from memory location 1000H to 100FH. Write 8086 assembly language programming (ALP) to transfer the data byte in reverse order to the new memory location 2001H to 200FH. **(10M)**

Q2. Draw and describe the functional block diagram of 8086 microprocessor and describe instructional queue In detail **(15M)**

Q.3 What are the different addressing modes used in the 8086 microprocessor? Discuss each with a suitable example. **(15M)**

Q.4 Explain the concept of segmented memory? What are its advantages? **(10M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1	1	1	10
Q2	3	3	1	2	1	15
Q3	3	3	2	2	2	15
Q4	3	3	2	3	3	10

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QUESTION PAPER

Name of the Examination: CAT (FALL 2023-2024) – II

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set No: 05 **Date of Exam:** 17/10/2023 (FN) (C1)

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Draw the architectural representation of the 8086 microprocessor. Discuss the functions performed by the Bus interface unit and an Execution unit. Calculate the Physical address. The value of Code Segment (CS) Register is 4042H and the value of different offsets is as follows: BX: 2025H , IP: 0580H , DI: 4247H. Calculate the effective address of the memory location pointed by the CS register. **(15M)**

Q2. Explain the various addressing modes used for sequential flow control of instructions in 8086 microprocessor with suitable examples. **(15M)**

Q3. The 8 data bytes are stored from memory location E000H to E007H. Write 8086 assembly language programming (ALP) to transfer the block of data to the new location B001H to B008H. **(10M)**

Q4. Explain the instructions used in the following program and describe the result of each of the instructions. **(10M)**

```
MOV AL, 69H
MOV BH, 85H
AND AL, BH
MUL BL
MOV DI, 505BH
MOV [DI], AL
INC DI
MOV [DI], AH
XOR BH, AH
```

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Name of the Examination: Continuous Assessment Test - II (CAT –II)

Winter Semester 2023-2024

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 06 **Date of exam:** 18/10/2023 (AN) (D2)

Duration: 90 mins **Total Marks:** 50

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. What is the role of segment registers in 8086 microprocessor architecture? Explain different segment registers with neat architectural diagram. If the code segment is started with 2034H address and the offset address is F231H, what is the value of physical address. [15]

Q2. Explain the status of each register and corresponding status flags after execution of each instruction of the following program [10]

```
MOV AX, 1000H
MOV CX, 2000H
RCL AX, 4
MOV BX, CX
RCR BX, 3
ADD AX, BX
```

Q3. Write a program to sort five 8-bit numbers stored in a data array in ascending order using 8086 assembly language programming. [10]

Q4. Explain different addressing modes of 8086 microprocessors with suitable examples. [15]

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	4,5	1, 2, 3, 5	1	1	15
Q2	3	4.5	1, 2, 3, 5	1	1	10
Q3	3	4,5	1, 2, 3, 5	1	1	10
Q4	3	4,5	1, 2, 3, 5	1	1	15

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Name of the Examination: Continuous Assessment Test - II (CAT –II)

Winter Semester 2023-2024

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 07 **Date of exam:** 16/10/2023 (FN) (B1)

Duration: 90 mins **Total Marks:** 50

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1.	Explain the concept of segmented memory? What are its advantages?	[15]

Q2.	What will be the content of AX register, and which flag(s) will be set if you execute the below program?
	
	MOV AX, 5
	SUB AX, 3
	CMP AX, 0
	JZ zero_flag_set
	JS sign_flag_set
	NOP
	HLT
	zero_flag_set:
	MOV AH, 2
	HLT
	sign_flag_set:
	MOV AH, 5
	HLT
		[10]

Q3.	Write a program in 8086 assembly language to add two 8-bit numbers. The two 8-bit numbers are stored in memory locations **1000H** and **1001H**. After addition store the result in memory location **1002H.**	[10]
Q4.	What do you mean by addressing mode? What are the different addressing modes supported by 8086?	[15]

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	4,5	1, 2, 3, 5	1	1	15
Q2	3	4.5	1, 2, 3, 5	1	1	10
Q3	3	4,5	1, 2, 3, 5	1	1	10
Q4	3	4,5	1, 2, 3, 5	1	1	15

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QUESTION PAPER

Name of the Examination: CAT-2 (FALL 2023-2024)

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 08 **Date of exam:** 18/10/2023 (FN) (CO1)

Duration: 90 mins **Total Marks:** 50

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1.	Explain the purpose and types of registers in the 8086 microprocessor, and how they are used in instruction execution and data manipulation?	**[10]**
Q2.	What are addressing modes in computer architecture, and why are they important for effective programming? Provide explanations for different addressing modes commonly used in microprocessors. For each addressing mode, give a detailed example of how it is used in an assembly language instruction for the 8086 microprocessor, along with the corresponding memory or register addresses.	**[15]**
Q3.	Explain the following instructions with suitable examples. 1. MOV, 2. MOVSB, 3. CMP, 4. ROR, 5. RCR, 6. ROL, 7. RCL, 8. JGE, 9. JC, 10. LODSB	**[10]**
Q4.	Write an assembly language program for the 8086 microprocessor to find the maximum value among a set of 8-bit unsigned integers stored in memory at five consecutive addresses starting from 2000:3000.	**[15]**

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1, 2, 3			10
Q2	1	1	1, 2, 3			15
Q3	2	2	1, 2, 3			10
Q4	2	2	1, 2, 3			15

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QUESTION PAPER

Name of the Examination: Fall 2023-24 Semester – CAT-2

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 10 **Date of Exam:** 16/10/2023 (AN) (B2)

Duration: 90 mins **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Explain about all the four control transfer addressing modes with suitable examples. **(10M)**

Q2. Write a program for 8086 microprocessor to check whether the data coming from the port having address 7789h is same as the value in AL register. If both the values are same, send the value 0000h to the port having address 34EFh. If both the values are not same, send the value FFFFh to the same above port. **(15M)**

Q3. The 8086 microprocessor executes the following program. Find out the values of all the flags at the end of the program execution. Also, show the values of the registers after each instruction execution. **(10M)**

```
MOV AX,3C49H
MOV BX, 2F18H
ADD AX, BX
MUL BL
SUB AX, BX
DIV BH
ADD AX, BX
```

Q4. Explain about stack of 8086. With suitable examples and diagrams, explain the PUSH and POP instructions? **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	3	3	1, 2, 3, 5	1	1	10
Q2	3	3	1, 2, 3, 5	1	1	15
Q3	3	3	1, 2, 3, 5	1	1	10
Q4	3	3	1, 2, 3, 5	1	1	15