VIT-AP UNIVERSITY	Regular Arrear Examinations (2023-24) - July 2024	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: ECE2002	Course Title: Computer Organization and Architecture	
Set No: 1	Exam Type : **Closed Book**	School: SENSE
Date: 09/08/2024	Slot: F	Session: FN

Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice

General Instructions if any:

1. **"*fx* series" - non Programmable calculator are permitted : YES /NO**
2. **Reference tables permitted : YES / NO (if Yes, Please specify:)**

PART – A: Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

1. How to represent the signed integer numbers? Perform arithmetic addition and subtraction using 2's complement. In this how to handle overflow? **(10 M)**

2. Define computer architecture and computer organization. Explain the different buses used in the microprocessor? **(10 M)**

3. Carry out the calculation steps for the 4-bit binary division of positive numbers 1000/0011 (i.e., 8/3) using the non-restoring division algorithm. **(10 M)**

4. Demonstrate the multiplication approach using Booth's algorithm to multiply 05 into 03. **(10 M)**

5. Write an 8086 assemble language program to find the factorial of an 8-bit number stored at a memory location 1000H. Additionally, the program must send the resultant value to a device connected through a port address 6000H. **(10 M)**

6. Discuss the addressing modes of 8086 microprocessor using suitable examples. **(10 M)**

7. What is the micro-operation required for following instruction.
   (a) STC
   (b) MOV R1, [2000] **(10 M)**

8. Demonstrate the basic organization of a hardwired control unit and the generation of control signals using hardwired control. **(10 M)**

9. Explain the concept of segmented memory? What are its advantages? **(10 M)**

10. An 8-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 24 bits. The size of the physical address space is 4 GB. Calculate the number of bits require for the SET field and TAG field. **(10 M)**

11. How 4-stage pipelined, and 5-stage pipelined microprocessor works? Identify the type of hazard that can result, if following instruction in executed on a pipelined microprocessor and how it can be avoided? [12]

ADD [4000H], AL
MOV BL, [5000H]

12. A four-stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, the total time taken to execute 1000 instruction on the pipeline will be? **(10 M)**

QP MAPPING

Q. No.	E/A/T	Module Number	Marks	BL	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped
Q1	A	1	10	2	1	1	1	1
Q2	E	1	10	1	1	1	1	1
Q3	A	2	10	3	2	1	1	1
Q4	A	2	10	3	2	1	2	2
Q5	T	3	10	4	3	2	2	2
Q6	E	3	10	1	3	2	2	2
Q7	A	4	10	4	4	2	2	2
Q8	A	4	10	2	4	2	3	3
Q9	E	5	10	1	5	3	3	3
Q10	T	5	10	3	5	3	3	3
Q11	A	6	10	4	6	3	3	3
Q12	T	6	10	3	6	3	3	3

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – FAT

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 1 **Date of Exam:** 15/5/2023 (FN) (A1)

Duration: 120 Minutes **Total Marks: 60 Marks**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.
3. Draw the necessary diagrams.
4. Underline the important points, titles, and subtitles.

Q1. Mention the Rules for Grouping of micro-operations. Also, evaluate the micro-operations for the Indirect and execute cycle for instruction **MOV B, [2001H].** **(12M)**

Q2. Show how ADD M(X) instruction can be executed using Wilke's design for microprogrammed control unit with suitable diagrams. **(12M)**

Q3. A set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight-bit words.

a) How many bits are required for addressing the main memory?
b) How many bits are needed to represent the TAG, SET, BLOCK and OFFSET fields?
c) Sketch the block diagram showing the mapping. Also, show a case of cache HIT / MISS by assuming an example **(12M)**

Q4. Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-

i) Pipeline cycle time ii) Non-pipeline execution time
iii) Speed up ratio iv) Pipeline time for 1000 tasks
v) Non-pipeline time for the same 1000 tasks **(12M)**

Q5. Write down a signed decimal number with a value of -25 in 32-bit floating point presentation for the presentation of signed numbers. Do the same also with the number 33. And, perform addition of these numbers in binary form using the flow chart. **(12M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	4	4	1,3	1	1	12
Q2	4	4	1,3	2	2	12
Q3	5	5	1,3	2	2	12
Q4	6	6	1,2,3,4	2	2	12
Q5	2	2	1,3	1	1	12

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QUESTION PAPER

Name of the Examination: FAT – WINTER SEMESTER (2022-2023)

Course Code: ECE2002 **Course Title: Computer Organization & Architecture**

Set Number: 3 **Date of Exam: 15/05/2023 (AN) (A2)**

Duration: 120 min **Total Marks: 60 Marks**

Instructions:

(1) All questions are compulsory.
(2) Assume data wherever necessary.
(3) Any assumptions made should be clearly stated.

Q1. Perform the signed division $(-32) \div (-8)$ using restoring algorithm. Tabulate the step-by-step process involved herein. **(15 Marks)**

Q2. Explain with a suitable diagram how a multi-stage pipelined microprocessor works? Identify the type of hazard that can result if following instructions are executed on a pipelined microprocessor and how it can be avoided? **(15 Marks)**

CMP [6000H], BL

PUSH [6000H]

Q3. (a) Explain the execution cycle of each of the following instructions in terms of micro-operations and their associated control signals: **(15 Marks)**

SUB AX, [1000H] and POP [2000H]

(b) Assuming unique control signal for each micro-operation, design a control circuitry for both the instructions using minimum logic gates.

Q4. Design a memory mapping between a cache memory of size 512KB and a main memory having each memory location specified by a 34-bit unique address. Considering a block size of 2KB, the mapping should provide a maximum 32 search count. **(15 Marks)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1,2,3,12	1,2	1,2,3	15
Q2	6	6	1,2,3,4,5,12	1,2,3	1,2,3	15
Q3	4	4	1,2,3,5	1,2	1,2,3	15
Q4	5	5	1,2,3,4,12	1,2,3	1,2,3	15

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 - FAT

Course Code: ECE2002 **Course Title:** Computer Organization & Architecture

Set number: 4 **Date of Exam:** 17/5/2023 (AN) (C2)

Duration: 120 **Total Marks:** 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Explain the flow chart of Booth's multiplication in detail. Also perform the signed multiplication of two numbers with multiplicand, B = 110111 and multiplier, A = 100011 using Booth's algorithm. **(15M)**

Q2. Consider any 16 instructions from IAS computer's instruction set. Identify the control signals required for one instruction out of 16. Design a micro-programmed control unit using Wilkes' design method with suitable diagrams. **(15M)**

Q3. Assume an Intel processor has the following memory configuration:

Size of main memory	2 GB
Size of cache memory	8 KB
Size of a cache block	128 Bytes

Determine the number of bits in main memory address, Tag size, block number, set number and offset. Assuming the cache is already filled, draw the memory mapping structure required for a 8-way set associative mapping of cache memory. **(15M)**

Q4. In the below program, I_1, I_2, I_3 .. BI_1 is the sequence of instructions and 100, 101, 102..250 corresponds to the memory location for each instructions.

100:I_1
101:I_2 (JMP250)
102:I_3

.

250: BI_1

Identify and explain the type of hazard that will arise when the above instructions are executed on a pipelined microprocessor. Discuss how this type of hazard can be avoided? **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1,2,3,4,12	1,2,3	1,2,3	15
Q2	4	4	1,2,3,5	1,2	1,2,3	15
Q3	5	5	1,2,3,4,12	1,2,3	1,2,3	15
Q4	6	6	1,2,3,4,5,12	1,2,3	1,2,3	15

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QUESTION PAPER

Name of the Examination: FAT (WIN 2022-2023)

Course Code: ECE2002 **Course Title:Computer Organization and Architecture**

Slot: 5 **Date of Exam:** 16/5/2023 (AN) (B_2)

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. A simple processor has four major phases to its instruction cycle: Fetch, indirect, execute and interrupt. Two 1-bit flags designate the current phase in a hardwired implementation. Why are these flags needed? Why are they not needed in a microprogrammed control unit? Also, show how Load M(500) can be implemented using Wilke's microprogrammed control unit? **(15M)**

Q2. a) A 4-way Set Associative cache consists of 64 lines. The main memory contains 4096 blocks of 128 bytes each. Show the mapping with suitable diagrams.

b) A fully associative cache has lines of 16 bytes and a total size of 8kB. The 64-Mbyte main memory is byte addressable. Show the format of Main memory addresses, tag, block number and offset. **(15M)**

Q3. How the pipelining stages be implemented in the processor using 8086? Identify the type of hazard that can result, if the following instruction is executed on a pipelined microprocessor and how it can be avoided? **(15M)**

```
MOV AL,42H
ADD [6000H],AL
MOV BL,[6000H]
```

Q4. Draw the flow chart and demonstrate the division approach using the non-restoring algorithm to divide 11 by 3. **(15M)**

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QUESTION PAPER

Name of the Examination: FAT (Win Semester 2022-2023)

Course Code: ECE2002 **Course Title:** computer architecture and organization

Slot: 7 **Date of Exam:** 16/5/2023 (FN) (B1)

Duration: 120 min **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

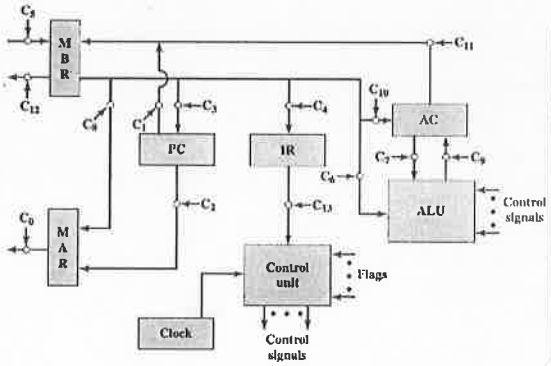
Q1. Write an 8086 program to convert Gray numbers into Binary. where 8-bit number stored at memory location 3000 and store result into 6000 memory address. [12]

Q2. Referring to the figures below,

(a) depict the control signals required for the execution cycle of LOAD 100 and ADD 400 using conventional hardwired method.

(b) Express the Boolean expression for each of the control signals.

(c) Implement the Boolean expressions for each of the control signals using minimum number of gates.



	Micro-operations	Active Control Signals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← (PC) + 1	C_5, C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	C_5, C_R
	t_3: IR(Address) ← (MBR(Address))	C_4
Interrupt:	t_1: MBR ← (PC)	C_1
	t_2: MAR ← Save-address PC ← Routine-address	
	t_3: Memory ← (MBR)	C_{12}, C_W

Q3. Why is multi-level cache memory required? What is cache hit ratio? If you have 44 cache hits (requests) and 11 misses, then what is the cache hit ratio? [12]

Q4. Design the memory mapping between the Cache memory of 8 MB to the main memory of 4 GB using 8 way set associative method where the block or page or frame size is of 4 KB. Consider each memory location is byte addressable. Write the number of bits required for memory address, tag address, block address and block location. [12]

Q5. How 4-stage pipelined, and 5-stage pipelined microprocessor works? Identify the type of hazards that can result, if following instruction in executed on a Von –Neumann based pipelined microprocessor and how it can be avoided? [12]

```
next1:  MUL [5000H]
        MOV BL, [5000H]
        JMP next1
```

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Name of the Examination: ~~WINTER~~ Short Summer-I **2022-2023 – FAT**

Course Code: ECE2092 **Course Title:** Computer Architecture

Set number: 1 **Date of Exam:** 21/06/2023 (FN)(A1)

Duration: 120 Min **Total Marks:** 60

Instructions: All questions are compulsory

Q1	Discuss the basic elements and functions of a computer.	**(15 M)**
Q2	Perform 9*3 using the unsigned multiplication algorithm.	**(15 M)**
Q3	Discuss the hardwired control unit design methods in detail.	**(15 M)**
Q4	Perform memory mapping between the Cache memory of 16 kB to the main memory of 4 GB using 2-way set associative mapping. Where the block size is 64 bytes and each memory location is byte addressable.	**(15 M)**

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	CO1	PO1, PO2, PO3			15
Q2	2	CO2	PO1, PO2, PO3, PO5			15
Q3	3	CO3	PO1, PO2, PO3, PO5			15
Q4	4	CO4	PO1, PO2, PO3, PO5			15

VIT-AP UNIVERSITY	Final Assessment Test – Long Summer (2023-24) - July 2024	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: ECE2002	Course Title: Computer Organization & Architecture	
Set No: 2	Exam Type : **Closed Book**	School: SENSE
Date: 20-07-2024	Slot: C	Session: AN

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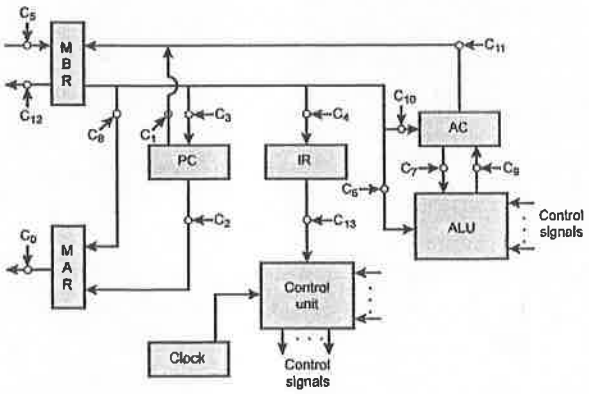
General Instructions if any:

1. **"*fx* series" - non Programmable calculator are permitted: NO**
2. **Reference tables permitted : NO**

Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

1. What are basic functions of a computer? Discuss with some real-life example. **(10 M)**
2. Discuss Moor's Law and its significance. **(10 M)**
3. Depict the restoring division Algorithm flowchart and perform binary operation to perform 9/3. **(10 M)**
4. Discuss IEEE 32-bit Floating point representation and present 123.55 in this format. **(10 M)**
5. Develop an 8086 Assembly Language Program (ALP) to find a number in an array of 50 numbers located at 3000H: 7000H. An optimum ALP is expected. **(10 M)**
6. Draw and discuss the flag register of 8086 microprocessor. **(10 M)**
7. What is pipelining in microprocessors and what are its hazards? **(10 M)**
8. **(10 M)**



For the IAS computer instructions, LOAD 350; SUB 300; derive the hardwire control unit using state table method. Use the above diagram to identify the control signals.

9. Draw the microprogrammed control unit. **(10 M)**
10. Discuss the memory hierarchy in computer. What is the need for this hierarchy? **(10 M)**
11. Perform the memory mapping between the Cache memory of 64 kB to the main memory of 8 GB using 4 way set associative method where the block or page or frame size is of 8 KB. **(10 M)**
12. **(10 M)**

A computer has the following memory capacity:Ram: 4 GB

Cache: 8 kB

Block size: 32 Bytes

Perform the One-way Set Associative Mapping and discuss the searching process with suitable diagrams.

VIT-AP UNIVERSITY	Final Assessment Test – Short Summer-II (2023-24) - July 2024	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: ECE2002	Course Title: Computer Organization and Architecture	
Set No: 2	Exam Type : **Close Book**	School: SENSE
Date: 20-07-2024	Slot: C	Session: FN
Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice		
General Instructions if any: 1. **"*fx* series" - non Programmable calculator are permitted: NO** 2. **Reference tables permitted: NO (if Yes, Please specify: NA)**		

PART – A: Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

Q1. Explain how to represent the number -41.125 using the IEEE 32-bit floating-point format? **(10M)**

Q2. Perform -9 by 6 using Booth's Algorithm step by step? **(10M)**

Q3. Describe the different instruction sets used in the 8086 processor with examples for each to illustrate how they work? **(10M)**

Q4. Explain microprogrammed control unit. What are the limitations of microprogrammed control unit? **(10M)**

Q5. Describe the levels of memory hierarchy in terms of speed, size, and cost. Explain the role of primary memory in this context? **(10M)**

Q6. Define pipelining in computer architecture. Discuss its hazards with examples and outline its drawbacks and limitations? **(10M)**

Q7. Show how to represent the numbers -8 and +21 using 8-bit 2's Complement notation? **(10M)**

Q8. Perform the division of -7 by -2 using the restoring division algorithm with clear steps. **(10M)**

Q9. Discuss the various flags used in 8086 microprocessors, provide the examples to illustrate how each flag is set or cleared during program execution? **(10M)**

Q10. Describe IAS memory machine. **(10M)**

Q11. What do you mean by Interrupt Vector Table (IVT) in an 8086 microprocessor, What is vectored interrupt and non-vectored interrupt? **(10M)**

Q12. What is the key difference between 2nd and 3rd generations of computer, Describe Von-Neumann Computer architecture? **(10M)**

QP MAPPING

Q. No.	E/A/T	Module Number	Marks	BL	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped
Q1	E	1	10	2	1	1,2,3	1,2	1
Q2	A	2	10	3	2	1,2,3	1,2	1
Q3	T	3	10	3	3	1,2,3	1,2	1
Q4	E	4	10	2	4	1,2,3	1,2	1
Q5	A	5	10	2	5	1,2,3	1,2	1
Q6	T	6	10	3	6	1,2,3	1,2	1
Q7	E	1	10	3	1	1,2,3	1,2	1
Q8	A	2	10	2	2	1,2,3	1,2	1
Q9	T	3	10	2	3	1,2,3	1,2	1
Q10	E	1	10	3	1	1,2,3	1,2	1
Q11	A	5	10	3	5	1,2,3	1,2	1
Q12	T	1	10	2	1	1,2,3	1,2	1

VIT-AP UNIVERSITY	Final Assessment Test – Long Summer (2023-24) - July 2024	
	Maximum Marks: 100	Duration: 3 Hours
Course Code: ECE2002	Course Title: Computer Organization & Architecture	
Set No: 2	Exam Type : **Closed Book**	School: SENSE
Date: 20-07-2024	Slot: C	Session: AN

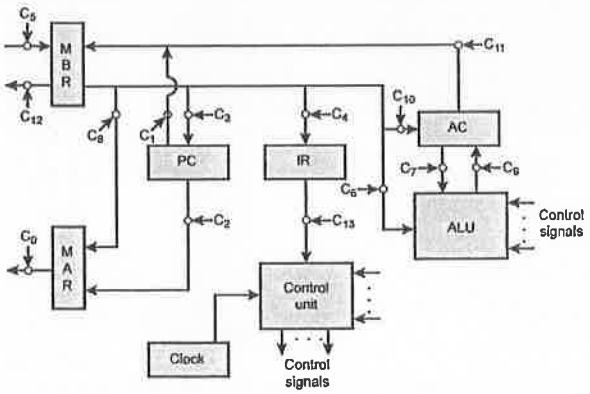
Keeping mobile phone/smart watch, even in 'off' position is treated as exam malpractice

General Instructions if any:

1. **"*fx* series" - non Programmable calculator are permitted: NO**
2. **Reference tables permitted : NO**

Answer any TEN Questions, Each Question Carries 10 Marks (10×10=100 Marks)

1. What are basic functions of a computer? Discuss with some real-life example. **(10 M)**
2. Discuss Moor's Law and its significance. **(10 M)**
3. Depict the restoring division Algorithm flowchart and perform binary operation to perform 9/3. **(10 M)**
4. Discuss IEEE 32-bit Floating point representation and present 123.55 in this format. **(10 M)**
5. Develop an 8086 Assembly Language Program (ALP) to find a number in an array of 50 numbers located at 3000H: 7000H. An optimum ALP is expected. **(10 M)**
6. Draw and discuss the flag register of 8086 microprocessor. **(10 M)**
7. What is pipelining in microprocessors and what are its hazards? **(10 M)**
8. **(10 M)**



For the IAS computer instructions, LOAD 350; SUB 300; derive the hardwire control unit using state table method. Use the above diagram to identify the control signals.

9. Draw the microprogrammed control unit. **(10 M)**
10. Discuss the memory hierarchy in computer. What is the need for this hierarchy? **(10 M)**
11. Perform the memory mapping between the Cache memory of 64 kB to the main memory of 8 GB using 4 way set associative method where the block or page or frame size is of 8 KB. **(10 M)**
12. **(10 M)**

A computer has the following memory capacity:Ram: 4 GB

Cache: 8 kB

Block size: 32 Bytes

Perform the One-way Set Associative Mapping and discuss the searching process with suitable diagrams.

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QUESTION PAPER

Name of the Examination: FAT (Fall 2023-2024)-FAT

Course Code: ECE2002 **Course Title:** COA

Slot: 01 **Date of Exam:** 01/12/2023 (AN)

Duration: 120 min **Total Marks: 60** (B_2)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

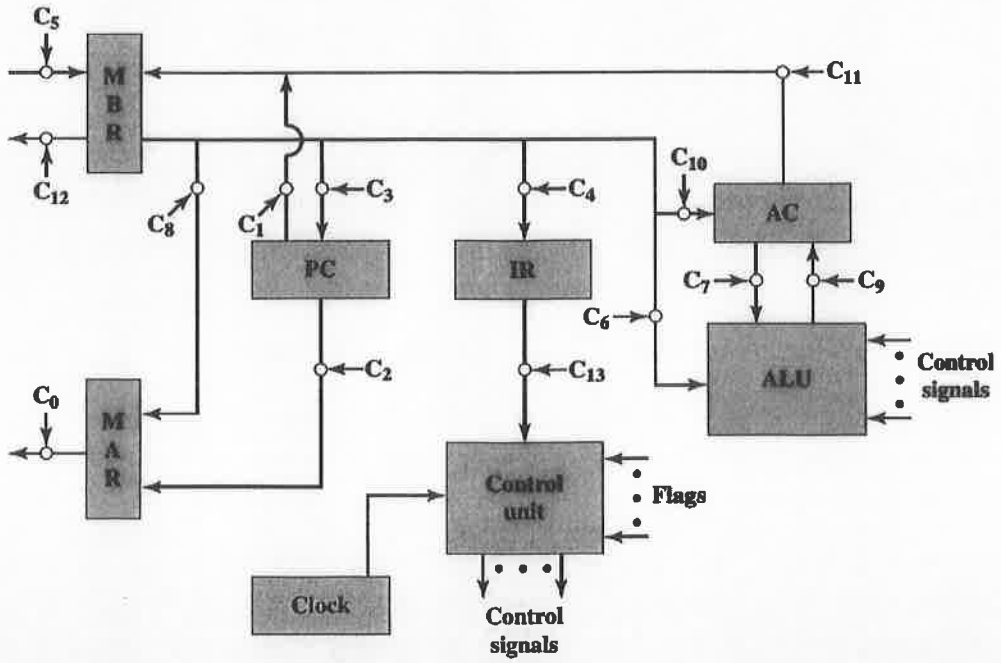
Q1. Demonstrate the multiplication approach using Booth's algorithm to multiply 09 by 08. **(12M)**

Q2. What is the micro-operation required for following instruction?

(a) STC
(b) MOV [R1], R2
(c) ADD R1, [BX] **(12M)**

Q.3. Referring to the figures below,

(a) Depict the control signals required for the fetch and execution cycle of ADD 200.
(b) Express the Boolean expression for each of the control signals.
(c) Implement the Boolean expressions for each of the control signals using a minimum number of gates. **(12M)**



Q4. An 8-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 24 bits. The size of the physical address space is 4 GB. Calculate the number of bits required for the SET field and TAG field. **(12M)**

Q5. A four-stage pipeline has stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, the total time taken to execute 1000 instructions on the pipeline will be? **(12M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1	1	2	12
Q2	3	3	1	2	1	12
Q3	4	4	1	3	1	12
Q4	5	5	2	4	3	12
Q5	6	6	2	3	3	12

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QUESTION PAPER

Name of the Examination: Fall 2023-24 Semester – FAT

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 02 **Date of Exam:** 02/12/2023 (AN) (G1)

Duration: 120 min **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Compute the product -5 × -7 using 4-bit twos complement notation based on Booth's algorithm? **(12M)**

Q2. Explain the concept of interrupts and the role of the Interrupt Vector Table (IVT) in managing interrupts in the context of 8086 microprocessor architecture. Provide examples of non-maskable and maskable interrupts? **(12M)**

Q3. A 5-stage pipelined processor has the stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Operand (WO). The IF, ID, OF, and WO stages take 1 clock cycle each for any instruction. The execution stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. **(8 + 4 = 12M)**

a. How many clock cycles are required to execute the following sequence of instructions with pipelining? Prepare the pipeline diagram.

MUL R2, R10, R1

DIV R5, R3, R4

ADD R2, R5, R2

SUB R5, R2, R6

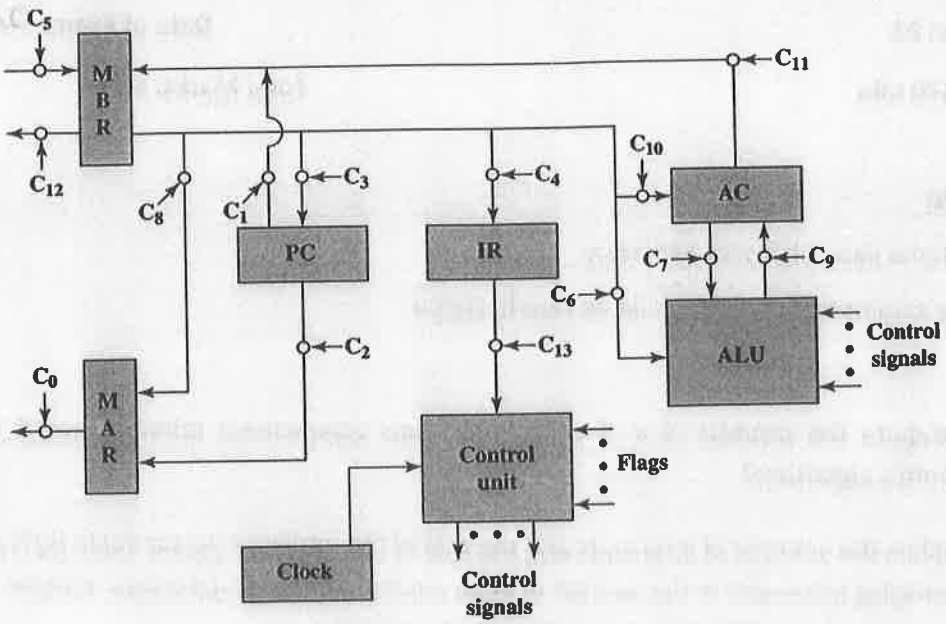
b. If the Microcontroller frequency is 2MHz, what is the operating frequency? Also calculate the number of clock cycles without pipelining.

Q4. List the sequence of micro-operations and corresponding active control signals of the following instructions in a tabular form for the processor shown in the below figure. **(3 + 3 + 3 = 12M)**

a) ADD R1, [5000H]
(Meaning: Add the contents of memory location 5000H with register R1)

b) MOV R1, [R2]
(Meaning: R1 register gets the data from memory location pointed by R2)

c) Jump if AC = 0



Q5. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. **(3 + 4 + 3 + 2 = 12M)**

a. How is a 16-bit memory address divided into set number, block number, and location number?

b. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1100 0011 0011 0100

c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

d. How many total bytes of memory can be stored in the cache?

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1, 2, 3	1	1	12
Q2	3	2	1, 2, 3	1	1	12
Q3	6	6	1, 2, 3	1	1	12
Q4	5	3	1, 2, 3	1	1	12
Q5	4	4	1, 2, 3	1	1	12

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Name of the Examination: Final Assessment Test (FAT)

Fall Semester 2023-2024

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 06 **Date of exam:** 04/12/2023 (AN) (D2)

Duration: 120 mins **Total Marks:** 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Perform the -14/11 using restoring signed division algorithm. [12]

Q2. Explain the micro operations of the following instructions of 8086 and IAS computer [4+4+4]

a. MOV AX, BX
b. AND AX, [1000H]
c. STOR M(200)

Q3. The alphabet "B" of a keyboard is pressed which is connected to the INTR pin of an 8086 processor. Explain the steps associated to execute the interrupt requested through the keyboard. Write a program to initialize the keyboard interrupt in vector table with interrupt vector 52H. The ISR of the keyboard interrupt is stored in offset address 4032H in data segment with segment address 2000H. [12]

Q4. A processor has 64 GB of RAM and 2MB of cache memory. If the size of the cache block is 128 bytes, then explain the mapping structure using 32-way associative mapping with a suitable diagram. Besides, find the following parameters [12]

a. Number of searches
b. Number of blocks in a set
c. Number of blocks in the RAM
d. Number of sets in the RAM
e. Tag size
f. Memory address structure

Q5. Design a microcontroller instruction pipeline to execute a program which has 6 instructions. Each instruction has 4 pipeline stages in the following order – Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex), and Register Write Back (WB). The fetch operation takes 1 clock cycle, decode operation takes 1 clock cycles, and register write back takes 2 cycles. The execution operation takes various clock cycles in each instruction whose values are (in the order of each instruction) 2, 5, 7, 6, 4, 2 clock cycles. [6+6]

a. With necessary diagrams, calculate the total number of clock cycles that will take to execute the program using pipeline. If the microcontroller is given a

clock with input clock frequency 1.5 GHz, what is the maximum clock frequency with which the microcontroller can operate?

b. If the instruction pipeline is flushed after every 2 instructions, calculate the total number of clock cycles taken.

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1,2,3	1,2	1	12
Q2	3	4,5	1,2,3,5	1,2	1	12
Q3	4	4	1,2,3,5	1,2	1	12
Q4	5	3	1,2,3,5	1,2	1	12
Q5	6	6	1,2,3,5	1,2	1	12

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QUESTION PAPER

Name of the Examination: FAT (FALL 2023-2024)

Course Code:	ECE2002	**Course Title:**	Computer Organization and Architecture
Set number:	08	**Date of exam:**	30/11/2023 (AN)(A2)
Duration:	120 mins	**Total Marks:**	60

Instructions:

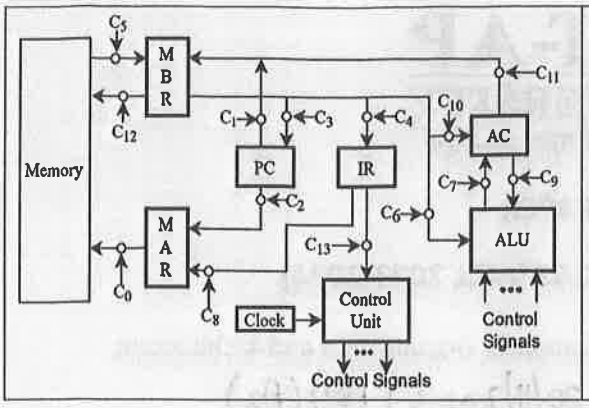
1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Consider the division of two signed numbers, -24 (dividend) and 5 (divisor), using the restoring algorithm. **[10]**

Q2. Give a detailed description about Interrupt Vectors. Draw a circuit diagram to show how a device with interrupt vector 45H can be connected on an 8088 microprocessor system. Using the Interrupt Vector Table shown below, determine the address of the ISR of a device with interrupt vector 45H **[15]**

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00000	3C	22	10	38	6F	13	2C	2A	33	22	21	67	EE	F1	32	25
00010	11	3C	32	88	90	16	44	32	14	30	42	58	30	36	34	66
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
00100	4A	33	3C	4A	AA	1A	1B	A2	2A	33	3C	4A	AA	1A	3E	77
00110	C1	58	4E	C1	4F	11	66	F4	C5	58	4E	20	4F	11	F0	F4
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
00250	00	10	10	20	3F	26	33	3C	20	26	20	C1	3F	10	28	32
00260	20	4E	00	10	50	88	22	38	10	5A	38	10	4C	55	14	54
.....	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
003E0	3A	10	45	2F	4E	33	6F	90	3A	44	37	43	3A	54	54	7F
003F0	22	3C	80	01	3C	4F	4E	88	22	3C	50	21	49	3F	F4	65

Q3. In the following diagram and Table different control signals are given with respect to the different microinstructions occurred during different cycles. Find out the equations and gate level circuits for all the control signals generated during fetch and execution of LOAD 600 instruction. **[15]**



	Microoperations	Active control singals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← PC+1	C_5 , C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	$C_5 C_R$
	t_3: IR(Address) ← MBR(Address)	C_4
Interrupt :	t_1: MAR ← (PC)	C_1
	t_2: MAR ← Save-Address PC ← Routine-Address	
	t_3: Memory ← (MBR)	C_{12} , C_W

Q4 Given a Pentium processor with the following configuration **[10]**

Size of Main Memory	8GB
Size of Cache Memory	16KB
Size of Cache Block	128 Bytes

A Fully Associative mapping is employed. Explain the mapping technique with suitable diagrams. Then find the following

1. Tag Size
2. Number of Search's
3. Method of Searching

Q5 Design a microcontroller instruction pipeline to execute a program which has 6 instructions. **[10]**
Each instruction has 5 pipeline stages in the following order – Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex), Memory Access (MEM) and Register Write Back (WB). The fetch operation takes 1 clock cycles, decode operation takes 1 clock cycles, memory access takes 2 cycles and register write back takes 1 cycle. The execution operation takes various clock cycles in each instruction whose values are (in the order of each instruction) 2, 3, 1, 3, 2, 1 clock cycles.

a) With necessary diagrams, calculate the total number of clock cycles that will take to execute the program in pipeline method. (8marks)
b) If the microcontroller is given a clock with input clock frequency 1.5 GHz, what is the maximum clock frequency with which the microcontroller can operate? (2marks)

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1,2	1, 2, 3			10
Q2	3	3	1, 2, 3			15
Q3	4	4	1, 2, 3, 5			15
Q4	5	5	1, 2, 3			10
Q5	6	6	1, 2, 3,5			10

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QUESTION PAPER

Name of the Examination: Fall 2023-24 Semester – FAT

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 10 **Date of Exam:** 30/11/2023 (FN) (AN)

Duration: 120 mins **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Convert the following decimal number into 64-bit IEEE 754 format 62597.57719781 x 2^{-11}. Also convert the given binary number into decimal 1 10010101011 10101111011000000.....0.

(12M)

Q2. For a processor requiring 60 micro-operations for all the instructions, show how this will be implemented using Wilke's design with suitable diagrams. Show how the control signals are generated of any two instructions of your choosing. **(12M)**

Q3. Design the memory mapping between the Cache memory of 16KB to the main memory of 512KB using a 2-way set associative method where the block size is of 2KB. Consider each memory location is byte addressable. Assume the cache is having the below given values from the respective sets of main memory. For example, "S61 B3" represents Block 3 from Set 61 of the main memory. Now, let the CPU is trying to access the memory location 5612. Determine whether you will have a cache HIT or a MISS? **(12M)**

S57 B0
S1 B1
S8 B2
S44 B3
S0 B0
S37 B1
S29 B2
S61 B3

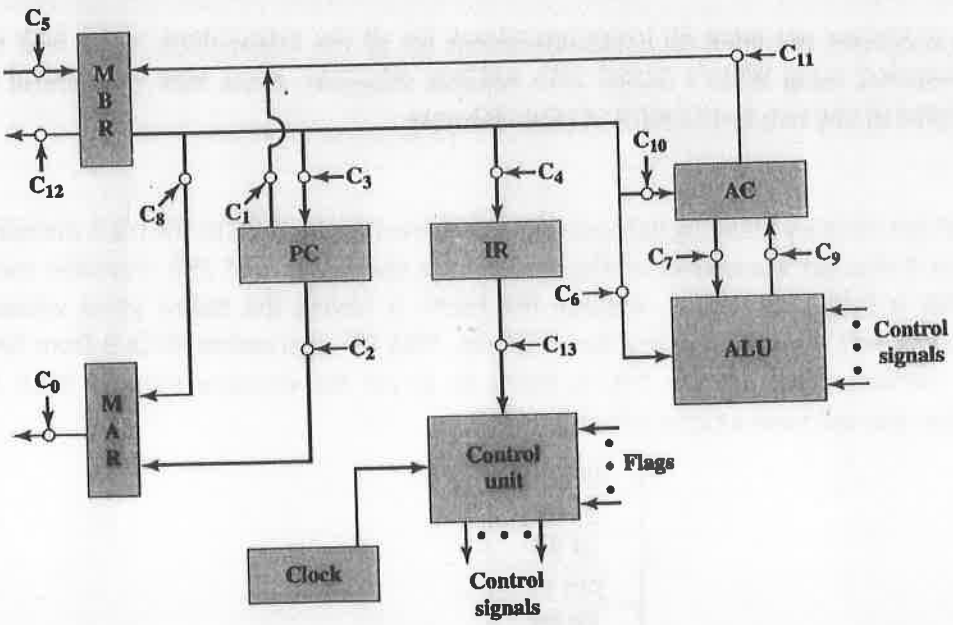
Q5. Explain how the 3-stage and 4-stage pipelined microprocessors work with the help of diagrams and derive the expressions for finding the time required for executing 'n' instructions? Identify the type of hazard that can result, if the following instructions are executed on a pipelined microprocessor and how they can be avoided? **(12M)**

SUB [5000H], AL

MOV BL, [5000H]

Q4. Explain the execution cycle of each of the following instructions in terms of micro-operations and their associated control signals: JMP 200 and CMP R1. JMP 200 will start executing from the address given in the instruction and CMP R1 will compare the registers R1 and AC and if both are equal the next two instructions are skipped. Design a control circuitry for all the control signals for both the instructions using minimum logic gates. **(12M)**

	Micro-operations	Active Control Signals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← (PC) + 1	C_5, C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	C_5, C_R
	t_3: IR(Address) ← (MBR(Address))	C_4
Interrupt:	t_1: MBR ← (PC)	C_1
	t_2: MAR ← Save-address PC ← Routine-address	
	t_3: Memory ← (MBR)	C_{12}, C_W



QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	2	1, 2, 3	1	1	12
Q2	4	4	1, 2, 3, 5	1	1	12
Q3	5	5	1, 2, 3	1	1	12
Q4	6	6	1, 2, 3, 5	1	1	12
Q5	4	4	1, 2, 3, 5	1	1	12

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QUESTION PAPER

Name of the Examination: Intra 2023-24 Semester – FAT

Course Code: ECE2002 | **Course Title: Computer Organization & Architecture**

Set number: II | **Date of Exam:** 11/1/24 (D)

Duration: 120 mins | **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Discuss the key technological developments in different generations of computers. **(15M)**

Q2. Represent the -125.0625 in IEEE 32-bit floating point representation. Also, discuss regenerating the decimal number from the IEEE 32-bit floating point representation to the decimal number. **(15M)**

Q3. Draw and discuss the flag register of 8086 microprocessor. **(15M)**

Q4. Discuss the memory hierarchy in the latest computers. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	2	1	15
Q2	2	2	1	2	1	15
Q3	3	3	1	2	1	15
Q4	5	5	4	-	1	15

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QUESTION PAPER

Name of the Examination: Intra 2023-24 Semester – FAT

Course Code: ECE2002 | **Course Title: Computer Organization & Architecture**

Set number: IV | **Date of Exam:** 12/1/24 (E)

Duration: 120 mins | **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Draw the architecture of the IAS computer and discuss register transfer operation for the following.

Memory Location	Instructions
00A H	LOAD M(00C H), ADD M(00D H)

(15M)

Q2. Perform -9*3=-27 using Booth's algorithm. **(15M)**

Q3. Draw and discuss the flag register of 8086 microprocessor. **(15M)**

Q4. What do you understand by cache memory mapping? Using suitable diagrams discuss different cache memory mapping. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	2	1	15
Q2	2	2	1	2	1	15
Q3	3	3	1	2	1	15
Q4	5	5	4	-	1	15

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QUESTION PAPER

Name of the Examination: Fall 2023-2024 Semester- FAT

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 04 **Date of Exam:** 04/12/2023 (FN)

Duration: 120 min **Total Marks: 60** (01)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Represent the decimal number 45.75 in single-precision floating-point format using the IEEE 754 standard. Show the binary representation for the sign, exponent, and mantissa. **(12M)**

Q2. Provide a definition of micro-operations and specify the micro-operations necessary during the execute cycle for the following instructions: (a) LOAD R3, 4000H, (b) MOV R2, [2000H], and (c) ADD R1, [R2] **(12M)**

Q3. Explain the procedure of hardware handshaking in RS232. Given a 4-bit binary encoding for 9 numbers (e.g., '0': 0000, '1': 0001 to '9': 1001), calculate the potential binary sequence received at DCE corresponding to the message "2023" sent by DTE. Each frame consists of 01 start bit, 4 data bits, 01 parity bit, and 02 stop bits. **(12M)**

Q4. In a scenario where a 4-way set-associative mapped cache with a block size of 4 KB is employed, and the main memory has a capacity of 16 GB with a 10-bit tag, determine the following: (a) Size of cache memory (b) Tag directory size (c) Number of Bits in Set Number **(12M)**

Q5. Design and evaluate a microcontroller instruction cycle pipeline for the execution of an embedded program comprising 500 instructions. Each instruction undergoes four pipeline stages in the following sequence: Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex), and Memory Access (MEM). The fetch operation requires 1 clock cycle, the decode operation takes 1 clock cycle, execute takes 4 clock cycles, and memory access takes 3 cycles. **(12M)**

(a) Utilizing essential diagrams, compute the total number of clock cycles required to execute the program.

(b) If the microcontroller is provided with a clock period of 20ns, determine the maximum clock frequency at which the microcontroller can operate.

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Name of the Examination: Final Assessment Test (FAT)

FALL Semester 2023-2024

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 05 **Date of exam:** 02/12/2023 (AN) (C2)

Duration: 120 mins **Total Marks:** 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1.	Consider the division of two signed numbers -21 (dividend) and 16 (divisor) using the restoring algorithm.	[12]
Q2.	Describe in detail the different forms of interrupts. How does the vector table work? Describe the instructions INT nn related to interrupt programming.	[12]
Q3.	Explain the vertical and horizontal microinstruction formats. Describe how they can be used for nano program control unit. Consider a control unit that generates 28 control signals. Then, show the microinstructions for both vertical and horizontal format.	[12]
Q4.	Develop a microcontroller instruction pipeline for the execution of a 5-instruction program. Each instruction progresses through 4 pipeline stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex), and Register Write Back (WB). The time requirements for each operation are as follows: fetch (1 cycle), decode (1 cycle), execute (2 cycles), and register write back (1 cycle). The execution operation for each instruction demands varying clock cycles (3, 5, 2, 2, 1). Using diagrams where applicable, determine the total number of clock cycles necessary for executing the entire program employing the pipeline method. If the microcontroller operates with a clock having an input frequency of 3 GHz, compute the maximum clock frequency achievable for the microcontroller.	[12]
Q5.	Consider a main memory of size 4MB that needs to be mapped with a cache memory of 64KB with a block size of 64 bytes. For the given hardware specifications, design the memory mapping using an 8-way set associative method. Compute the tag size, number of searches and main memory address format. Also, comment on the hit ratio of the mapping technique.	[12]

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Name of the Examination: Final Assessment Test (FAT)

Fall Semester 2023-2024

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 07 **Date of exam:** 01/12/2023 (FN) (B1)

Duration: 120 mins **Total Marks:** 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Perform the arithmetic operation below with binary numbers and with negative numbers in signed-2's complement representation. Use seven bits to accommodate each number together with its sign. In each case, determine if there is an overflow by checking the carries into and out of the sign bit position. [12]

(a) (+ 35) + (+ 40) (b) (- 35) + (- 40)

Q2. Describe the micro operations involved in the execution of the following instructions in the 8086 microprocessor: [12]

a. AND AX, 0400H
b. SUB AX, [200H]
c. LOAD M(300)

Q3. Imagine a scenario where the 'Tab' key on a keyboard triggers an interrupt connected to the INTR pin of an 8086 processor. Outline the step-by-step process of handling this keyboard interrupt. Additionally, create a program to set up the keyboard interrupt in the vector table, specifying a custom interrupt vector (e.g., 60H), and storing the Interrupt Service Routine (ISR) at a specific offset address (e.g., 4096H) within a data segment (e.g., with a segment address of 3000H). [12]

Q4. In a communication setup using the RS232 protocol, information is transmitted from Data Terminal Equipment (DTE) to Data Communication Equipment (DCE). Each frame consists of 01 start bit, 05 data bits, 01 parity bit, and 03 stop bits. Given a 5-bit binary encoding for 26 alphabets (e.g., 'A': 00001, 'B': 00010 to 'Z': 11010), calculate the potential binary sequence received at DCE corresponding to the message VITAP sent by DTE. [12]

Q5. Develop a microcontroller instruction pipeline for the execution of a 10-instruction program. Each instruction progresses through 4 pipeline stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex), and Register Write Back (WB). The time requirements for each operation are as follows: fetch (1 cycle), decode (1 cycle), execute (2 cycles), and register write back (1 cycle). [12]

a. Using diagrams where applicable, determine the total number of clock cycles necessary for executing the entire program employing the pipeline method.
b. If the microcontroller operates with a clock having an input frequency of 3 GHz, compute the maximum clock frequency achievable for the microcontroller.

QP Mapping

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1,2,3	1,2	1	12
Q2	4	4,5	1,2,3,5	1,2	1	12
Q3	3	2,3	1,2,3,5	1,2	1	12
Q4	3	3	1,2,3,5	1,2	1	12
Q5	6	6	1,2,3,5	1,2	1	12