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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – CAT-1

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 2 **Date of Exam:** 14-02-2023 (AN)

Duration: 90min **Total Marks: 50** (B2)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Discuss about the various components of a computer system with neat diagram. **(10M)**

Q2. What are Harvard and Von Neumann architectures. Which architecture is generally preferred among them? **(10M)**

Q3. In the following assembly code written for the IAS computer, each word contains either a 40-bit constant or two 20-bit (left-L and right-R) instructions. The data contains three 100-word integer arrays, A(I), B(I) and C(I), starting at memory locations 101, 201 and 301, respectively. **(10M)**

Memory address	Instruction	Comment
0	99	Constant N, initialized to 99
1	1	Constant, set to 1
2	100	Constant, set to 100
3L	LOAD M(200)	Transfer A(100) from Memory address 200 to AC
3R	ADD M(300)	Place A(100) + [B(100) from Memory address 300] in AC
4L	STOR M(400)	Transfer AC to C(100) at Memory address 40
4R	LOAD M(0)	Load N in AC
5L	SUB M(1)	Decrement N in AC by 1
5R	JUMP + M(6, 20:39)	Test N, if N ≥ 0, jump to 6R to continue
6L	HALT	Halt otherwise
6R	STOR M(0)	Update N in Memory address 0
7L	ADD M(1)	Increment AC by 1
7R	ADD M(2)	
8L	STOR M(3, 8:19)	Modify memory address in 3L
8R	ADD M(2)	
9L	STOR M(3, 28:39)	Modify memory address in 3R
9R	ADD M(2)	
10L	STOR M(4, 8:19)	Modify memory address in 4L
10R	JUMP M(3, 0:19)	

Examine the assembly code and determine what result it produces.

Q4. Using flowchart depict the procedure to perform -9 into 3 using Booth's Algorithm **(10M)**

Q5. Perform division of the following numbers using Restoring algorithm as Dividend =17 and Divisor=3. **(10M)**

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – CAT-1

Course Code: ECE2002 **Course Title:** Computer Organization and Architecture

Set number: 3 **Date of Exam:** 15-02-2023 (C2)

Duration: 90 Mins **Total Marks:** 50 (AN)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Given that a program has 4 Million instructions with percentages of 40, 30, 30 for ALU related (Category I_1), load/store (Category I_2), and branching instructions (Category I_3), respectively. Compare the performance of two personal computers (PC) using MIPS with processors configurations as follows:

PC1:- clock freq: 500 MHz; CPI I_1: 2; CPI I_2: 4; CPI I_3: 4.

PC2:- clock freq: 700MHz; CPI I_1: 1; CPI I_2: 5; CPI I_3: 5.

(CPI = Clock per instructions) **(10M)**

Q2. Represent 300.5625 in the IEEE 32 bit-floating point representation format. Describe the each step of conversion. **(10M)**

Q3. Find out quotient and remainder of the division -21/8 by applying signed binary division using restoring algorithm. **(15M)**

Q4. Explain the memory format of IAS computer for data representation and instructions. Draw the architecture of the IAS Computer and briefly describe the importance of MAR, MBR, PC, and IBR register. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	2	1	10
Q2	2	2	1	2	1	10
Q3	2	2	1	2	1	15
Q4	1	2	1	2	1	15

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QUESTION PAPER

Name of the Examination: CAT (WIN 2022-2023)

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Slot: 4 **Date of Exam:** 13-02-2023 (AN)

Duration: 90 min **Total Marks: 50** (A2)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. a) Discuss different functional units of a digital computer system with its block diagram. **(5M)**

b) Justify whether present day computers are the combination of both Harvard and Von-Neumann concepts or not. **(5M)**

Q2. Draw the flow chart and demonstrate the division approach using the non-restoring algorithm to divide 11 by 3 **(10M)**

Q3. How to represent the signed integer numbers? Perform arithmetic operation in binary using **sign magnitude and 2's** complement representation

(i) (+34) + (-15)

(ii) (-34) – (-15) **(10M)**

Q4. Use the Booth algorithm to multiply 25(multiplicand) by 15(multiplier), where each number is represented by 6 bits. **(10M)**

Q5. The IAS operates by repetitively performing an instruction cycle, which consists of two sub-cycles: a fetch cycle and an execute cycle. On the IAS, describe the tasks accomplished during the fetch cycle and execute cycle. **(10M)**

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – CAT-1

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: 5 **Date of Exam:** 14-02-2023 (FN)

Duration: 90 min **Total Marks: 50** (B1)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. What is the distinction between computer organization and computer architecture. List and briefly define the main structural components of a computer. **(10M)**

Q2. Define and explain IAS computer and its memory format. Write an IAS program to compute the results of the following equation.

$$Y=(B+C)/D$$

Assume that *B*, *C*, and *D* are stored in memory location 1001, 1002, and 1003 respectively. **(10M)**

Q3. Explain the IEEE single and double precision standard of floating point representation. Convert -14.25D in single and double precision format. **(10M)**

Q4. Represent -73 and +65 in twos complement form using eight bits. Perform (+70) + (+80) and (-70) + (-80) with binary numbers in twos complement representation. Use eight bits to accommodate each number together with its sign. **(10M)**

Q5. Use the Booth algorithm to multiply 25 by 15. Represent each number using 6 bits. **(10M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	1	10
Q2	1	2	1	2	1	10
Q3	2	2	2	2	2	10
Q4	2	2	1	2	1	10
Q5	2	2	2	2	1	10

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QUESTION PAPER

Name of the Examination: WINTER 2022-2023 – CAT-1

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Set number: ~~1~~ **Date of Exam:** 13-02-2023 (FN)

Duration: 90 min **Total Marks: 50** (A1)

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. With a suitable diagram explain how the instructions are executed within IAS machine. **(10M)**

Q2. Convert the following numbers into the floating-point repartition using IEEE 754: 32-bit format.

(a) 2B3AH (b) 16.125

(10M)

Q3. How to represent the signed integer numbers? Perform arithmetic addition and subtraction using 2's compliment with suitable examples. Explain the process of identifying overflow condition during binary addition?

(15M)

Q4. Draw the flowchart of the restoring algorithm and perform the calculations for 15/5. Discuss each step-in detail.

(15M)

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	2	3	10
Q2	1	1	1,2	1	1	10
Q3	2	2	2	1	1	15
Q4	2	2	1	1	1	15

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QUESTION PAPER

Name of the Examination: CAT (FALL 2022-2023)

Course Code: ECE2002 **Course Title: Computer Organization and Architecture**

Slot: SB1+STB1 **Date of Exam: 01-11-2022**

Duration: 90 min **Total Marks: 50**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. What are the different buses used in the Microprocessor? Draw the single bus structure. **(10M)**

Q2. Draw the flow chart and demonstrate the division approach using the restoring algorithm to divide 11 by 3. **(15M)**

Q3. How to represent the signed integer numbers? Perform arithmetic operation in binary using sign-magnitude and 2's complement representation.

(i) (+34) + (-15)

(ii) (-34) – (-15) **(10M)**

Q4. What are the different addressing modes used in the 8086 microprocessor? Discuss each with a suitable example. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	1	10
Q2	2	1	2	2	1	15
Q3	2	2	3	2	3	10
Q4	3	2	4	2	3	15

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QUESTION PAPER

Name of the Examination: FAT 2022-2023

Course Code: ECE2002 **Course Title:** COA

SET number: 1 **Date of Exam:** 20-12-2022-FN (B1)

Duration: 120 min **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. How to represent the signed integer numbers? Perform arithmetic operation in binary using 1's and 2's complement representation

(i) (+42) + (-13)

(ii) (-42) – (-13) **(10M)**

Q2. Demonstrate and explain how control signals are generated using Micro-Programmed control unit. **(10M)**

Q3. What are the different phases of a basic computer instruction cycle ? Explain instruction cycle with flowchart. **(10M)**

Q4. Explain a function of the memory management unit in a typical computer. Demonstrate Direct and Set associative map technique in cache memory. **(15M)**

Q5. What is instruction pipelining? Discuss the conflicts that occurred during instruction Pipelining? **(15M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1	1	2	10
Q2	4	2	1	2	1	10
Q3	4	2	1	3	1	10
Q4	5	1	2	4	3	15
Q5	6	3	2	3	3	15

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QUESTION PAPER

Name of the Examination: FALL 2022-2023

Course Code: ECE2002 **Course Title:** COA

Set number: 3 **Date of Exam:** 20-12-2022- AN (B2)

Duration: 120 mins **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. Explain the algorithm for performing the multiplication of two numbers with multiplicand, B=10111 and multiplier, A= 10011. **(10M)**

Q2. Describe the Wilkes' micro programmed control unit. Also highlight its advantages and dis-advantages. **(10M)**

Q3. Explain any one type of hardwired control unit and with suitable diagram. **(10M)**

Q4. Consider a main memory of size 4MB that needs to be mapped with a cache memory of 64KB with a frame size of 8KB. For the given hardware specifications, design the memory mapping using an 8-way set associative method. **(15M)**

Q5. What are the limitations of a scalar pipelined processor? Explain pipelined superscalar processor of degree m=3 for four stages of instruction execution. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1	1	2	10
Q2	4	2	1	2	1	10
Q3	4	2	1	3	1	10
Q4	5	1	2	4	3	15
Q5	6	3	2	3	3	15

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QUESTION PAPER

Name of the Examination: FALL 2022-2023 - FAT

Course Code: ECE2002 **Course Title:** COA

Set number: 4 **Date of Exam:** 21-12-2022- FN (C1)

Duration: 120 mins **Total Marks: 60**

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. How to represent the signed integer numbers? Perform arithmetic addition and subtraction operation of 31 and 12 using two's complement. In this example, explain how to handle the overflow? **(10M)**

Q2. Compare hardware and micro programmed control units? Also compare horizontal and vertical micro-instructions. **(10M)**

Q3. Discuss how micro operations are organized to control a processor. **(10M)**

Q4. Consider a main memory associated with 22-bit physical address and a cache memory having 8KB space. For the given hardware, design the memory map using fully associative method considering frame size equal to 2KB. **(15M)**

Q5 What are the pipeline hazards that can cause a slowdown in the pipeline process? Briefly explain all of them with possible remedies. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1	1	2	10
Q2	4	2	1	2	1	10
Q3	4	2	1	3	1	10
Q4	5	1	2	4	3	15
Q5	6	3	2	3	3	15