KARTHIK C G

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Aim is to pursue challenging assignments in Product Development with a reputed organization in the semiconductor industry.

PRÉCIS

- ✓ An astute performer with more than **9.5 years** of experience in Physical Design in Qualcomm andIntel.
- ✓ Aneffectivecommunicatorwithexcellentrelationshipandstronganalytically,challengeoriented,problemsolving& organizational abilities.

EMPLOYMENT FORTES

Intel Technology India	SOC Design Engineer (Grade7)	Since 24th April 2017
Qualcomm India	Senior Design Engineer	From Oct 2014 to Apr 2017
Tata Elxsi(client Qualcomm)	Senior Design Engineer	From May 2012 to Oct 2014
Nano chip solutions	Physical design Engineer	From July 2011 to May 2012

TECHNICAL EXPERTISE

Synthysis	DC, DCT, Genesis
Place and Route	ICC2 , IC Compiler, SOC encounter, Innovus
Signoff	StarRC, PT, Calibre, Redhawk, Conformal, Joules, Tempus
Scripting	TCL, Python

- ❖ Comprehensive understanding of Synopsys/Cadence RM design FLOW for ICC,ICC2 and Innovus.
- ❖ Good Experience in freezing multi-voltage floorplans for complex designs with multiplememories.

ACADEMIC CREDENTIALS

2011	Bachelor of EngineeringinTelecommunication	VTU

CAREER PROFILE

- ***Responsibility*** **:** **Subsystem PD LEAD along with block implementation**

Technology **:** 7nm(TSMC)

Challenge faced **:** Learning new flow along with new tool set. Training engineers on the new flow and tools along with implementing blocks and leading cluster level power checks for signoff. Accepting new IPs for closure and distributing the new responsibilities among the team for a smooth execution in the last month of project time cycle without affecting our block implementation is a tough and challenging decision we as a team took. Along with the above responsibilities I help in running Chip level joules runs for power analysis.

- ***Responsibility*** **:** **LEAD for 10 partitions along with block implementation**

Technology **:** 14nm(Intel)

Challenge faced **:** Leading a team of 13 members towards closure of 10 partitions.Continuous interaction with the cross-site teams, training RCGs, analysis,debug and tracking the UPF and timing issues of all the partitions in parallel with implementation of a UPF critical block with multiple voltage areas was very challenging.

- ***Responsibility*** **:** **Subsystem LEAD**

Technology **:** 14nm(Intel)

Challenge faced **:** I pitched into the project after the final release of the netlist for a subsystem with 5 blocks. The partition was not converging with more than 40K shorts and ~1 lakh timing issues. Re-floorplanning with proper feedthrough punching and block rearrangement without disturbing the sub-system level interface ports and Continuous interaction with Synopsys AEs, motivating and guiding the team of 6 engineers with multiple experiments and closing all timing and layout issues was very challenging.

- ***Responsibility*** **:** **Block implementation**

Technology **:** 10nm, 14nm, 22nm(Intel).

Challenge faced **:** A timing critical block was implemented first time in Intel. I did multiple experiments from Synthesis to route and had continuous interaction with the designer in Israel to get many design issues fixed in theRTL.
I was also recognized for supporting another block for getting congestion in control and reducing the number of shorts form 1.7lkhs to closure.

- ***Responsibility*** **:** **DDRsub-system**

Technology **:** 7nm(TSMC)

Challenge faced **:** This was my first time I worked on partitioning flow. pin placement challenges, block area challenges, congestion due to pin placement, clock and data synchronous paths and budgeting were some of the interesting challenges that I faced.

- ***Responsibility*** **:** **Memory controller**

Technology **:** 10nm(TSMC)

Challenge faced **:** This block has more than 1.2M instance in a single hierarchy, timing fixes for this needed alot of manual effort, used standard cell grouping and created bounds based on data flow analysis to control spreading for the standardcells.

- ***Responsibility*** **:** **Interface communication block**

Technology **:** 14nm / 20nm /28nm(TSMC)

Challenge faced **:** Handling 2 projects in parallel and helping 2 teams with a strength of 5. Analyzing all issues and guiding teammates to fix the same with proper settings and delivering quality data on time is a challenge I havefaced.