DIGITAL FUNDAMENTALS

Part A:3 marks each Part B: 6 marks each

MODULE 1

PART A

1. Represent +45, -45 in 1's complement and 2's complement form. (2 times)
2. Implement a full adder using 8:1 MUX
3. Convert decimal number 3.248 x 10^4 to a single precision floating point binary number
4. Express the number -173 as a 12-bit number in Sign Magnitude, 1's Complement and 2's Complement notation.
5. Convert decimal no 4.248 * 104 to a single precision floating point binary number
6. Express the decimal number -23 as an8 bit number in the 1's and 2's complement form. (2 times)
7. Design a 4:1 MUX with the help of a truth table and logic diagram. (2times)
8. Represent +35,-35 in 8 bit 1's complement and 2's complement representation
9. Implement a half adder with a multiplexer
10. Implement a full adder by deriving expressions from its truth table.

PART B

1. Explain about single precision floating point representation with an example
2. Minimize the Boolean expression f(A,B,C,D)=Σm(1,5,6,7,9,15)+d(2,3,11,13) using Karnaugh map and realize it using NAND gates. (2 times)
3. Minimize the Boolean expression f(A,B,C,D)=Σm(0,1,3,5,7,8,9,11,13,15) using Karnaugh map and realize it using NAND gates.
4. Using Boolean algebra techniques simplify the expression
   a) AB+A(B+C)+B(B+C)
   b) Express +19 and -19 in 2's complement form
5. Optimize the Boolean function, F (A, B, C, D) =m0+m1+m7+m13+m15 with don't care conditions d(A, B, C, D) = m2+m6+m8+m9+m10 using K-Map.
6. What is a multiplexer? Using an 8-to-1 MUX, implement the Boolean function F(A,B,C,D)=∑ (1,3,4,11,12,13,14,15).
7. Design an Octal to Binary encoder with the help of a truth table and logic diagram.
8. Reduce the Boolean function specified in the truth table to its minimum SOP form by using a K-Map.
9. Minimize the Boolean expression f(A,B,C,D)=Σm(1,3,5,8,9,11,15)+d(2,13) using Karnaugh map and realize it using NAND gates.
10. Distinguish between decoders and demultiplexers. Implement a function F(A,B,C)=∑m(0,3,5,7) using decoder.

11. Convert decimal number 3.257×10^4 into IEEE-754 single precision floating point binary representation
12.

Inputs			Output
X	Y	Z	S
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

MODULE 2

PART A

1. How could you convert RS flip flop to D flip flop?
2. What is meant by modulus of a counter? Realize a mod-8 synchronous counter.
3. Explain Serial In Serial Out shift register with the help of circuit diagram.
4. How can you convert JK Flip Flop to D flip flop?
5. What is a D Flip-flop? Derive a D flip-flop from RS flip-flop.
6. Design a mod-6 asynchronous Up counter using T flip-flops
7. Distinguish between Combinational and Sequential circuits.
8. With the help of logic and timing diagram, design an Asynchronous Two bit Upcounter using positive edge triggered JK Flip-Flops.
9. What is a flipflop. list its 2 applications
10. Explain serial in parallel out shift register. Give its one application.
11. Implement a JK flip flop and explain its working
12. Construct a Mod-5 Asynchronous counter.

PART B

1. Demonstrate the working of a JK flip flop. How does it eliminate the invalid condition in SR flip flop? List out its applications.
2. Design a mod-12 asynchronous counter
3. Explain working of an edge triggered SR flip flop in detail. (2times)
4. Design 3 bit UP/DOWN synchronous counter (3 times)
5. A) Mention any four applications of shift registers.
   B) Describe the working of a Parallel in Serial Out register
6. What are the basic functions of a shift register? Explain 4 bit PISO shift register with a neat diagram.
7. A) Design a mod 9 Asynchronous counter and explain its working B) Why asynchronous counters are known as Ripple counters?
8. A) Compare synchronous counters and asynchronous counters. (b) Explain the working of a 3 bit synchronous counter with a timing diagram.
9. Implement and explain the working of a 4-bit Parallel In Serial Out (PISO) shift register

MODULE 3

PART A

1. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much? (2 times)
2. Describe about little endian and big endian byte ordering (3 times)
3. A program runs in 10 seconds on computer A, which has a 2 Ghz clock. we are trying to help a computer designer build a computer B which will runs this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. what clock rate should we tell the designer to target?
4. Describe code sequence C=A+B in single Accumulator Organization and Stack Organization of instruction set architecture. (2 times)
5. Differentiate between fixed length encoding and variable length encoding
6. What is an addressing mode? Mention the addressing modes used for the branch and jump instructions
   Hint: Immediate, register indirect, PC Relative, Absolute, Indirect addressing modes
7. Consider 2 processors P1and P2 executing the same instruction set. P1 has 3 GHZ clock rate and CPI of 1.5 and P2 has 1.5GHZ clock rate and a CPI of 1.0. Which processor has the highest performance expressed in instructions/second
8. Briefly describe 5 key components of a computer system

PART B

1. Explain the five classic components of a computer with diagram. (4 times)
2. Describe the code sequence of C=A+B in different types of instruction set architecture.
3. What do you mean by Addressing Modes? Explain any three addressing modes that have been used in recent computers
   Hint: Immediate, Register, Direct(absolute) addressing modes
4. Explain the five classic components of a computer with figure
5. Calculate and Compare the average execution time between instructions of a nonpipelined implementation to a pipelined implementation. The operation times for the major functional units are 200ps for memory access, 200ps for ALU operation, and 100ps for register file read or write. Consider the 3 consecutive load instructions. (Eg: lw $t1,100($t2))
6. What is Addressing Mode? Describe any three Addressing Modes with examples.

7. Explain the different classes of instruction set architectures with an example
8. List down and briefly explain the 8 great ideas in Computer Architecture
9. Define addressing mode. Explain 5 addressing modes with examples.

MODULE 4

PART A

1. Explain 4 stage pipelining with a diagram.
2. Differentiate between memory mapped I/O and Isolated I/O
3. Explain ay one of the bus arbitration schemes in DMA
4. How to calculate branch target address in branch on equal (beq) instruction?
5. Diagrammatically explain the Daisy Chain arrangement for handling simultaneous arrivals of interrupt requests
6. What are the datapath elements used for Load/Store instructions?
7. Explain the use of Vectored Interrupts.
8. What is Bus Arbitration? List out and explain two approaches to Bus Arbitration
9. Draw the data path for R-format instructions and explain it.
10. Explain two methods of mapping I/O devices
11. What are the MIPS data path components required to construct a Branch (beq) Datapath? Represent their symbols and the control signals associated with them
12. Briefly explain different types of pipeline hazards

PART B

1. Draw a single data path representation for memory instructions and R-type instructions (3 times)
2. What is Direct Memory Access? Explain two types of bus arbitration schemes (2 times)
3. How two or more simultaneous interrupt requests be handled? Explain with figure.
4. List different types of pipeline hazards with examples. (3 times)
5. With a neat diagram, explain the operation of DMA controllers in a computer system
6. What is Direct Memory Access? Explain the data transfer operation using Direct Memory Access.
7. Write notes on: Direct Memory Access and Interrupt Handling

MODULE 5

PART A

1. What is static RAM?
2. Define temporal locality and spatial locality. (2 times)
3. Write a short note on memory operation: a) Write back b) Write through
4. Explain different types of ROM
5. Draw a SRAM Cell and explain how the read and write operations are performed?
6. Sketch the internal organization of a 2M x 8 dynamic memory chip.
7. Explain the operation of a static RAM cell with the help of a diagram
8. Differentiate between PROM and EPROM?
9. Explain about memory hierarchy.
10. If a CPU has 16-bit address bus and 8-bit words, how much memory can it address?
11. What is semi-conductor memory?

PART B

1. Elaborate the various cache memory mapping techniques with an example for each. (5 times)
2. Explain the internal organization of memory chips and design a 1K*1 memory chip using decoder.
3. How the virtual address is converted into real address in a paged virtual memory system? Explain (2 times)
4. A computer system uses 16-bit memory addresses. It has a 2K bye cache organized I a direct mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits I each of the Tag, Block and word fields of the memory address.
5. What is virtual memory? Explain the process of address translation.
6. Explain the organization of 4M*32 memory module with 512k*8 static memory chips with a diagram
7. A) construct a 1 KB memory IC using 1024 x 4 Memory Chips
   B) What do you understand by virtual memory?