Karthikeya Mandava

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Education

DVR & Dr. HS MIC College of Technology Kanchikacherla, Andhra Pradesh, India

Bachelor of Technology, Electronics & Communication Engineering, **Percentage: 66.11/100** 2016-2019

Coursework: Switching Theory and Logic Design, Digital System Design & DICA, Microprocessors & Microcontrollers, VLSI Design, Computer Architecture & Organization, Low Power VLSI Design.

Work Experience

Sankalp Semiconductor Pvt. Ltd. (HCLTech) Bangalore, India

Design Verification Engineer Nov 2021 – Preset

- Managed verification item lists, coordinated various IPs within the SoC, and conducted coverage analysis to ensure a comprehensive verification process.
- Collaborated with cross-functional teams to analyze and resolve design issues, ensuring timely project delivery.
- Led low-power verification efforts, verifying power management features and validating various power modes for SoC designs, resulting in optimized power consumption.
- Mentored junior team members, providing technical guidance and fostering skill development to build a high-performing verification team.

Qsocs Technologies Bangalore, India

Design Verification Engineer Oct 2019 – Nov 2021

- Assisted in creating comprehensive verification plans and test cases for thorough design coverage.
- Conducted systematic regressions, actively debugged to validate functionality, and resolve bugs in collaboration with the design team.
- Prepared detailed documentation, including detailed verification reports, to maintain clear records of progress and results.

Projects

UWB SoC Verification (Client: Renesas)

- Developed C-based test cases for simulation and validation of design behavior, focusing on modules like IOTOP, RIIC, ADC, RLIN, CAC, WDTB, etc.
- Created Low Power Mode scenarios for all IPs in the project, incorporating written assertions to ensure comprehensive verification coverage.

NVMe Over Fabrics IP Verification (Client: Intel)

- Developed test cases based on the verification item list and efficiently debugged errors during the verification process.
- Conducted coverage analysis and utilized scripting to enhance verification efficiency and completeness.

AHB Interconnect Functional Verification

- Designed and implemented test benches, sequences, and monitors to simulate AHB interconnect transactions, enabling thorough functional testing and identifying potential issues
- Conducted regression testing to ensure new changes did not adversely impact previously verified functionality, maintaining a stable and reliable AHB interconnect verification environment.

VIP Development and Verification

- Significantly contributed to the team's success by developing functional coverage points and creating exhaustive test cases, leading to successful verification of various IPs, including APB, AHB, AXI, and UART, with achieved high coverage levels.
- Implemented error injection mechanisms to validate the AXI VIP's response to exceptional scenarios. Developed a robust scoreboard to cross-check the design's responses against expected results, ensuring the AXI interface's correctness and reliability.

Skills and Interests

Technical Skills: Verilog HDL, System Verilog HDVL, UVM Methodology, Perl, Python, TCL, and Shell scripting.
Protocols: AMBA (APB, AHB, AXI), PCIe, UART, SPI, IIC, LIN
Tools Known: ModelSim, VCS, NCSim, vManager, Questa, Incisive, Verdi, DVe