Karthikeya Mandava

10 Paul Robeson Blvd, New Brunswick, NJ 08901
732-207-5185 karthikeyamandava.2@gmail.com linkedin.com/in/karthikeya2 github.com/karthikeya-2

Education

Rutgers University – New Brunswick **Sep. 2024 – May 2026**
Master of Science in Electrical and Computer Engineering *New Brunswick, NJ*

DVR and Dr. HS MIC College of Technology **Jun. 2016 – May 2019**
Bachelor of Technology in Electronics and Communication Engineering *Andhra Pradesh, India*

Relevant Coursework

- Computer Architecture
- Security Engineering
- Deep Submicron VLSI Design
- Hardware and System Security
- Digital System Design and DICA
- Low-Power VLSI Design
- Computer-Aided Digital VLSI Design
- High-Performance and Distributed Computing

Experience

Sankalp Semiconductor Pvt. Ltd. (HCLTech) **Nov. 2021 – July 2024**
Member Technical Staff (Design Verification) *Bangalore, India*

- Managed verification item lists, coordinated various IPs within the SoC, and conducted coverage analysis to ensure a comprehensive verification process.
- Collaborated with cross-functional teams to analyze and resolve design issues, ensuring timely project delivery.
- Led low-power verification efforts, verifying power management features and validating various power modes for SoC design, resulting in optimized power consumption.
- Mentored junior team members, providing technical guidance and fostering skill development to build a high-performing verification team.

Qsocs Technologies **Oct 2019 – Sep 2021**
Jr. Verification Engineer *Bangalore, India*

- Assisted in creating comprehensive verification plans and test cases for thorough design coverage.
- Conducted systematic regressions, actively debugged to validate functionality, and resolved bugs in collaboration with the design team.
- Prepared detailed documentation, including detailed verification reports, to maintain clear records of progress and results.

Projects

UWB SoC Verification (Client: Renesas) | *Embedded C, SV, Python, Perl* **Jan. 2023 - Jul. 2024**

- Developed C-based test cases for simulation and validation of design behavior, focusing on modules like IOTOP, RIIC, ADC, RLIN, CAC, WDTB, etc.
- Created Low-Power mode test cases for all IPs in the SoC, incorporating written assertions to ensure comprehensive verification coverage.

NVMe Over Fabrics IP Verification (Client: Intel) | *Verilog, SV, UVM, Python, Shell* **Nov. 2021 - Dec. 2022**

- Developed test cases based on the verification item list and efficiently debugged errors during the verification process.
- Conducted coverage analysis and utilized scripting to enhance verification efficiency and completeness.

AHB Interconnect Functional Verification | *Verilog, SV, UVM, Perl* **Jan. 2020 - Oct. 2021**

- Designed and implemented test benches, sequences, and monitors to simulate AHB interconnect transactions, enabling thorough functional testing and identifying potential issues.
- Conducted regression testing to ensure new changes did not adversely impact previously verified functionality, maintaining a stable and reliable AHB interconnect verification environment.

VIP Development and Verification | *Verilog, System Verilog, UVM, Python* **Oct. 2019 - Jan. 2020**

- Significantly contributed to the team's success by developing functional coverage points and creating exhaustive test cases, leading to successful verification of various IPs, including APB, AHB, AXI, and UART, which achieved high coverage levels.
- Implemented error injection mechanisms to validate the AXI VIP's response to exceptional scenarios. Developed a robust scoreboard to cross-check the design's responses against expected results, ensuring the AXI interface's correctness and reliability.

Technical Skills

Languages: Verilog HDL, System Verilog, UVM Methodology, Embedded C, Perl, Python, TCL, Shell scripting.
Protocols: AMBA (APB, AHB, AXI), NVMe-oF, UART, SPI, IIC, CAN FD, LIN.
Tools Known: ModelSim, VCS, NCSim, vManager, Questa, Incisive, Verdi, DVe, IFV.