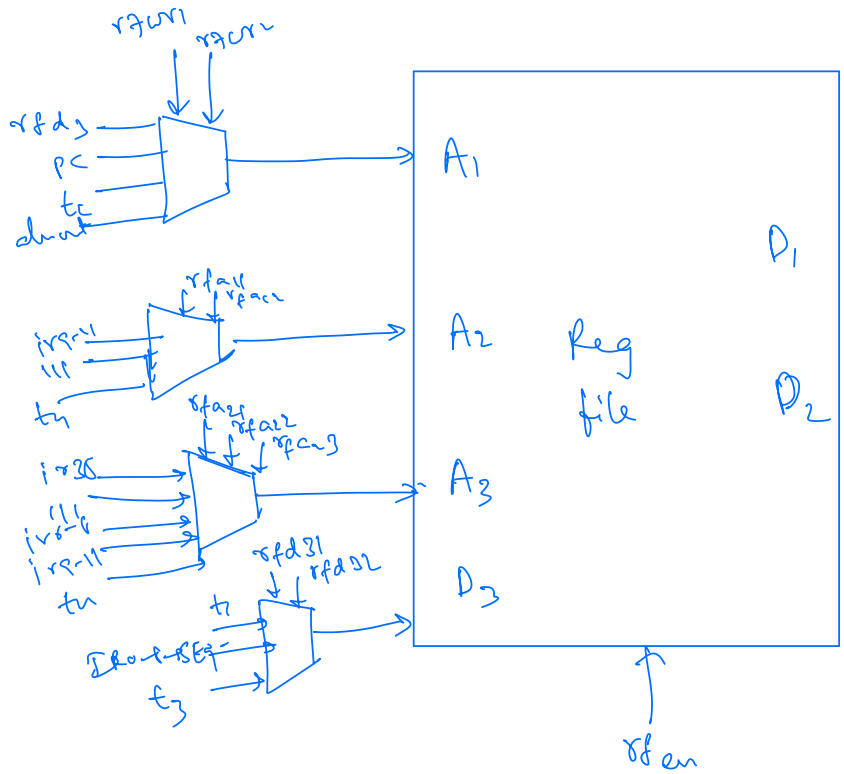
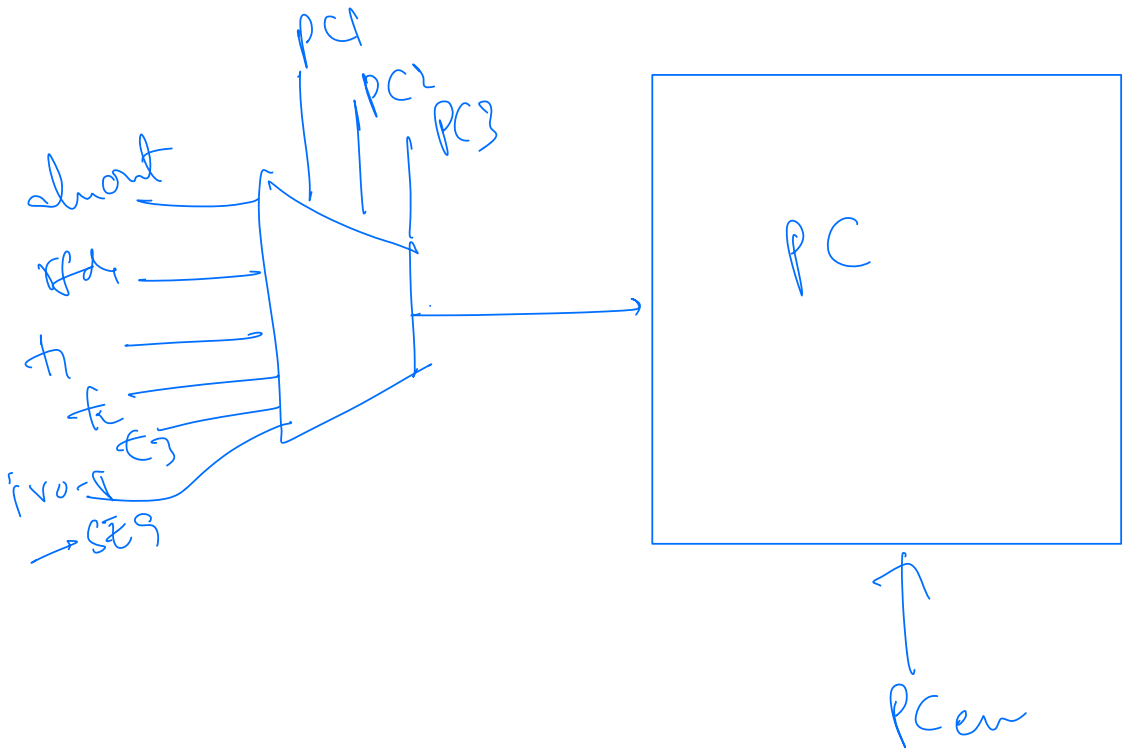
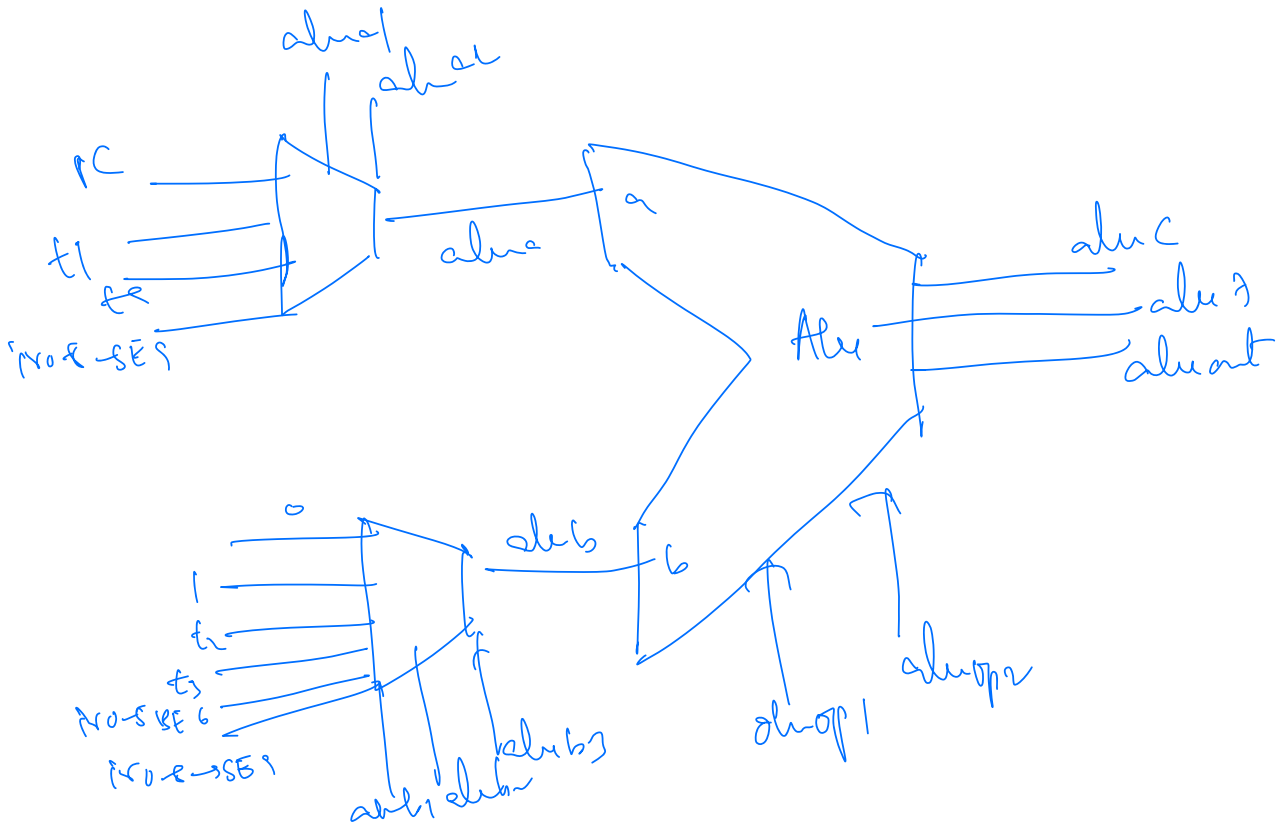
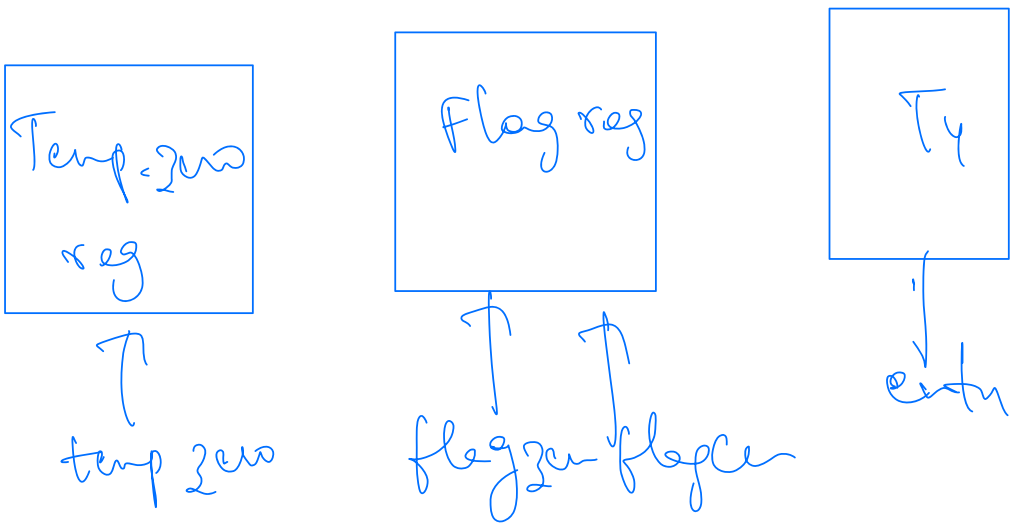
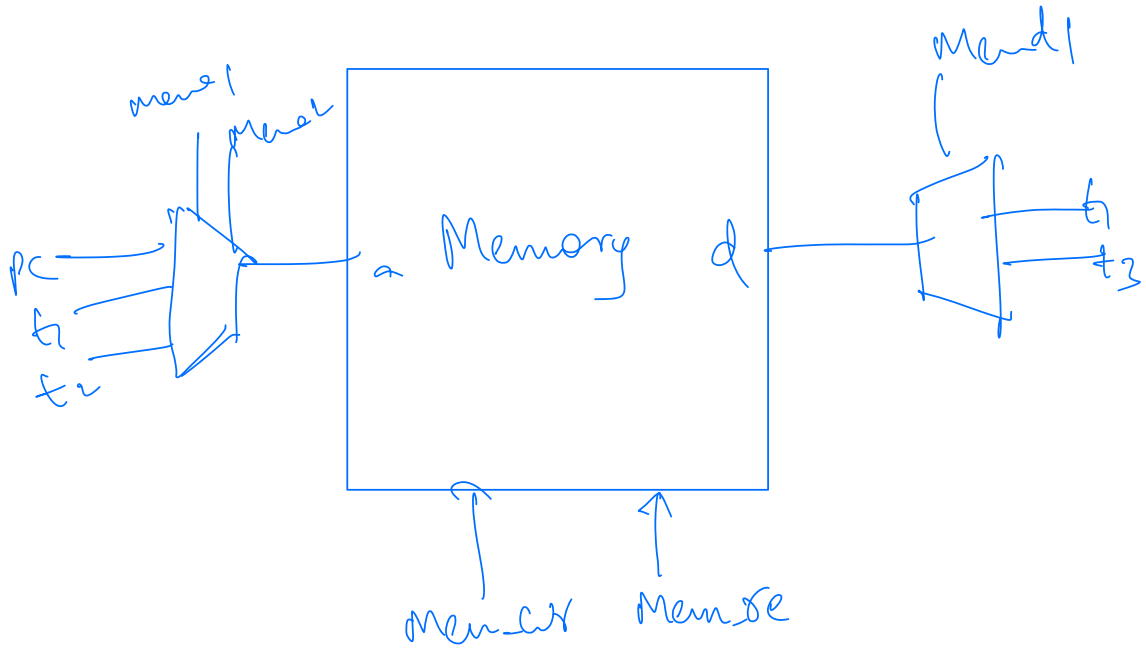
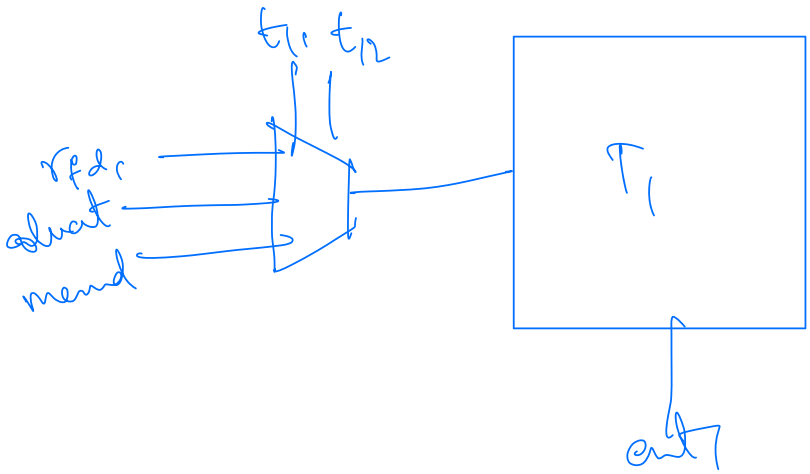

A1
D1
A2
Reg file
D2
A3
D3
rf en

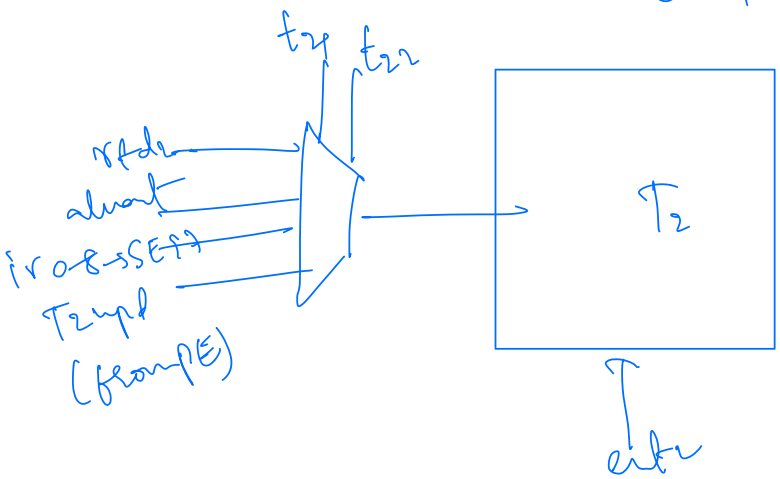

PC1
PC2
PC3
PC
PC en

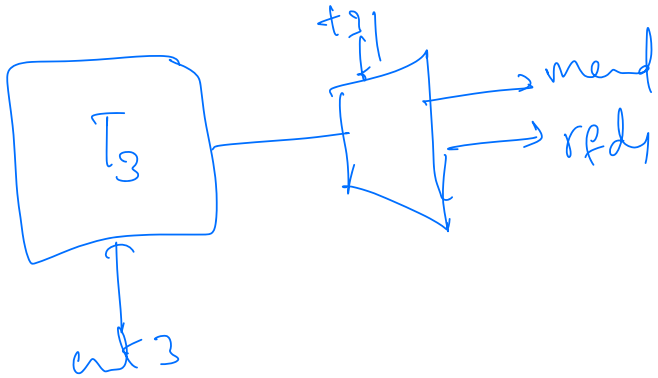

alu a1
alu a2
PC
t1
t2
IR0-5 SE 5
alu a
a
Alu
alu c
alu z
alu ovf
0
1
t2
t3
IR0-5 SE 6
IR0-8 SE 9
alu b
b
alu b1
alu b2
alu b3
alu op1
alu op2

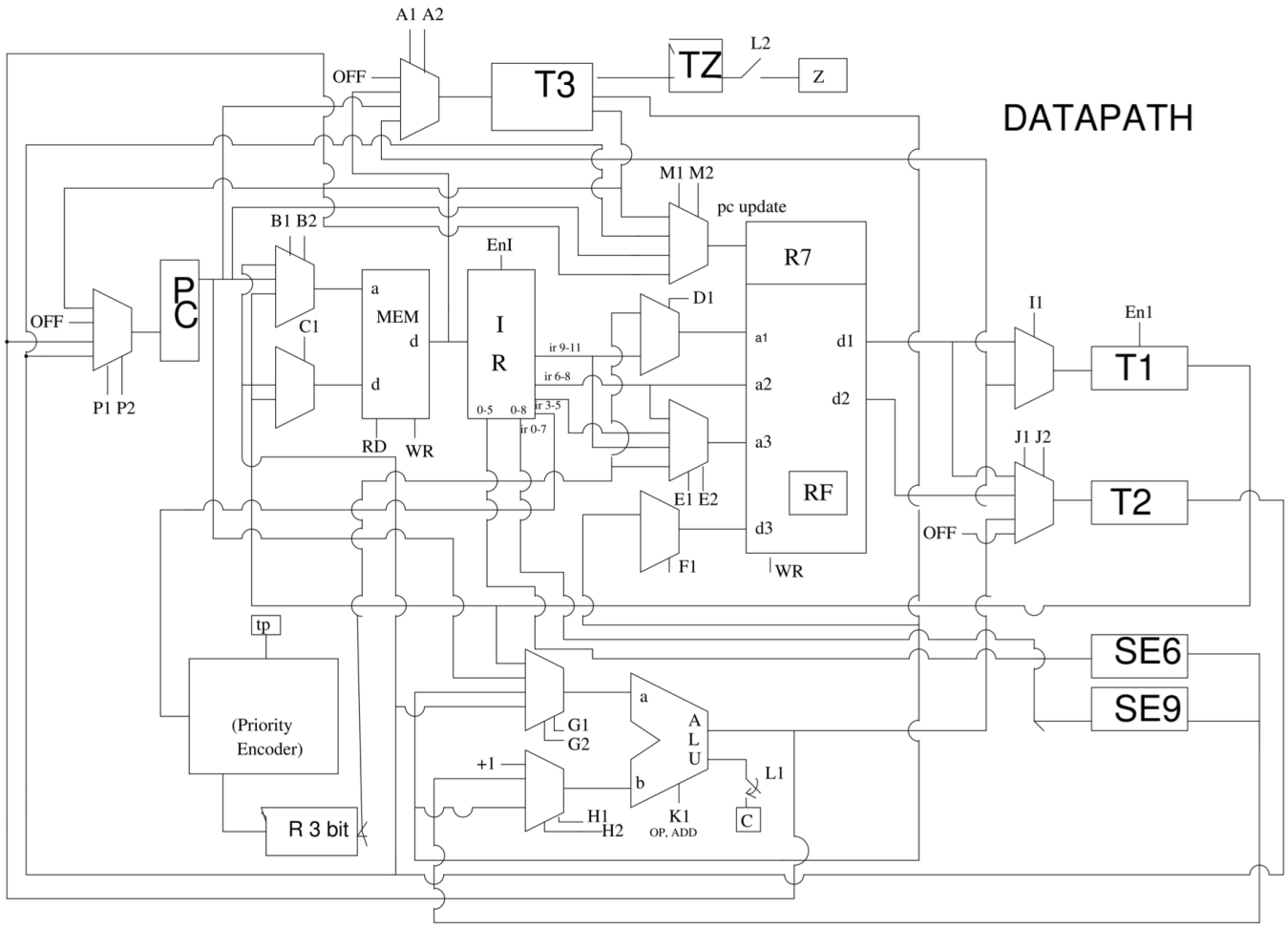

Temp zero reg
Flag reg
T4
temp zero
flag zero
flag cy
ex t4


mem1
mem2
PC
t1
t2
a
Memory
d
Mem1
t1
t3
Mem_cs
Mem_oe


t11
t12
rfdr
alwat
mem1
T1
out1


t21
t22
rfdr
alwat
irq-8-SEF7
T2upl
(from PE)
T2
out2


T3
mem
rdy
wt 3


DATAPATH
A1 A2
OFF
T3
TZ
L2
Z
M1 M2
pc update
B1 B2
EnI
R7
PC
OFF
P1 P2
C1
a
MEM
d
d
I
R
ir 9-11
ir 6-8
ir 3-5
ir 0-7
0-5
0-8
RD
WR
D1
a1
d1
a2
d2
a3
RF
d3
WR
E1 E2
F1
I1
En1
T1
J1 J2
T2
OFF
SE6
SE9
tp
(Priority
Encoder)
R 3 bit
G1
G2
+1
H1
H2
a
b
A
L
U
K1
OP, ADD
L1
C