# Control Signal Syntax

## ① ALU

Using 7 control bits

Input:

alu_a, alu_b

i) alu_a_mux:

| alu_a_1 | alu_a_2 | input |
|---|---|---|
| 0 | 0 | PC |
| 0 | 1 | T1 |
| 1 | 0 | T2 |
| 1 | 1 | ir_0-8 → SE9 |

ii) alu_b_mux:

| alu_b_1 | alu_b_2 | alu_b_3 | input |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | $t_2$ |
| 0 | 1 | 1 | $t_3$ |
| 1 | 0 | 0 | ir_0-5 → SE6 |
| 1 | 0 | 1 | ir_0-8 → SE9 |

operation

| aluop-1 | aluop-2 | operation |
|---|---|---|
| 0 | 0 | Add |
| 0 | 1 | Subtract |
| 1 | 0 | NAND |

2 + 3 + 2 = 7 bits

② Register File

Using 10 control bits

i/p : rf_a1 , rf_a2 , rf_a3 , rf_d3

rf_en (activate high)

| rf_wr_1 | rf_wr_2 | mux_rf_7 o/p |
|---|---|---|
| 0 | 0 | rf_d3 |
| 0 | 1 | PC |
| 1 | 0 | t2 |
| 1 | 1 | alu_out |

rf_a1 input :

| rf_a11 | rf_a12 | mux_rf_a1 o/p |
|---|---|---|
| 0 | 0 | ir_9-11 |
| 0 | 1 | 111 |
| 1 | 0 | t4 |
| 1 | 1 | X |

rf_a3 input :

| rf_a31 | rf_a32 | rf_a33 | mux_rf_a3 o/p |
|---|---|---|---|
| 0 | 0 | 1 | ir_3-5 |
| 0 | 1 | 0 | 111 |
| 0 | 1 | 1 | ir_6-8 |
| 1 | 0 | 0 | ir_9-11 |
| 1 | 0 | 1 | t4 |

rf_d3 input

| rf_d31 | rf_d32 | mux_rf_a1 o/p |
|---|---|---|
| 0 | 0 | t1 |
| 0 | 1 | ir_0-8 → Lshift 7 |
| 1 | 0 | t3 |
| 1 | 1 | X |

③ Memory

Using 5 contol bits

mem_write_bar

mem_read_bar

mem_a_mux:

| mem_a1 | mem_a2 | mem_a_mux o/p |
|---|---|---|
| 0 | 0 | PC |
| 0 | 1 | t1 |
| 1 | 0 | t2 |
| 1 | 1 | X |

mem_d (when write bar is 0)

mem_d1 : 0 → t1

1 → t3

④ Reg T1 : 3 control bits

en_t1 : Active High

| t1_1 | t1_2 | t1_mux (o/p) |
|---|---|---|
| 0 | 0 | rf_d1 |
| 0 | 1 | alu_out |
| 1 | 0 | mem_d |
| 1 | 1 | X |

⑤ Reg_T2

Using 4 control bits

en_t2 : Active High

| t2_1 | t2_2 | rf_t2_mux o/p |
|---|---|---|
| 0 | 0 | rf_d2 |
| 0 | 1 | alu_out |
| 1 | 0 | ir_08 → SEQ |
| 1 | 1 | T2_update (from PE) |

⑥ Reg T3

Using 2 control bits

en_t3 : Active High

t3_1 : 0 → mem_d
1 → rf_d1

⑦ Reg T4 :

Using 1 control bit

en_t4 : Active High

⑧ Flag Register

Using 2 bits

flag z_en : Active High

flag c_en : Active High

⑨ PC :

Using 4 control bits

PC_en : Active High

| pc_1 | pc_2 | pc_3 | mux-pc o/p |
|---|---|---|---|
| 0 | 0 | 0 | alu_out |
| 0 | 0 | 1 | rf_d1 |
| 0 | 1 | 0 | t1 |
| 0 | 1 | 1 | t2 |
| 1 | 0 | 0 | t3 |
| 1 | 0 | 1 | ir_0-8 → LSHIFT 2 |

⑩ IR : 1 control bit

ir_en : Active High