**VLSI SYSTEM DESIGN**

**TERM ASSIGNMENT**

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**ABSTRACT**

As part of our term assignment we are going to implement a digital clock with alarm function using Verilog HDL. The digital clock basically consists of a clock unit, time counter unit and a display unit. The clock unit generates the clock pulse of one second period. The FPGA kit has frequency oscillator which generates 50-MHz, 27 MHz and 24 MHz clock pulses. A frequency divider is used to reduce either of these clocks to a frequency of 1 Hz. The time counter unit counts the one second clock pulses and save them as seconds, minutes and hours in the memory. The display unit takes the data from the memory and displays them in the seven segment display. The alarm function is implemented as a separate block. The alarm unit asserts an output when the setup time is attained. The time of the digital clock has to be initially set by the user. So, the digital clock as a whole has user input and control unit. The input unit involves functions such as time reset, change of time, change of alarm time and stopping alarm. While, the control unit controls the blocks such as clock unit, time counter unit, display unit and alarm unit.