Computer Architecture Lab

Assignment 6 Report

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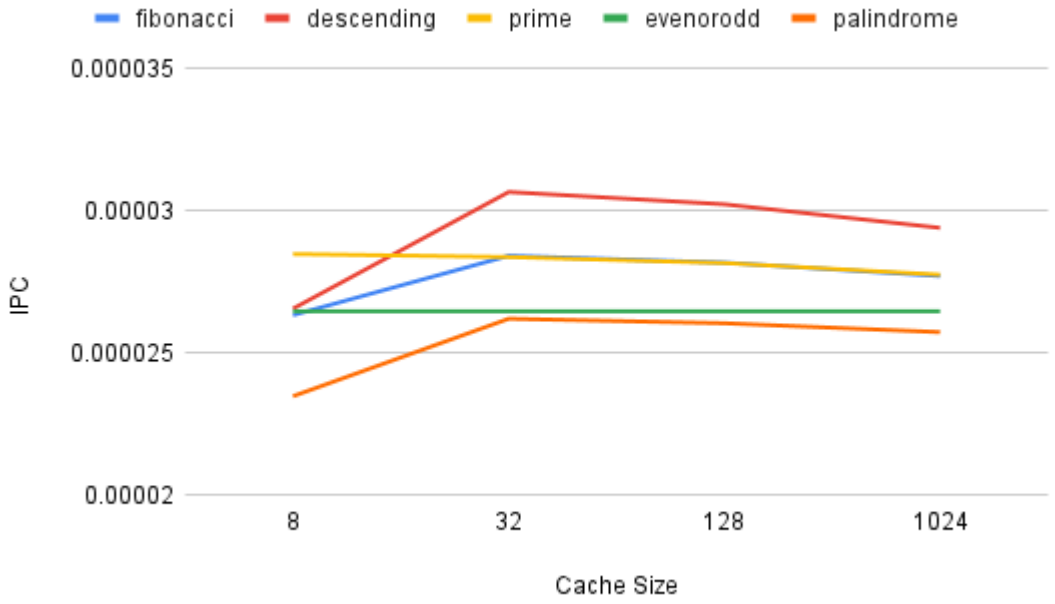
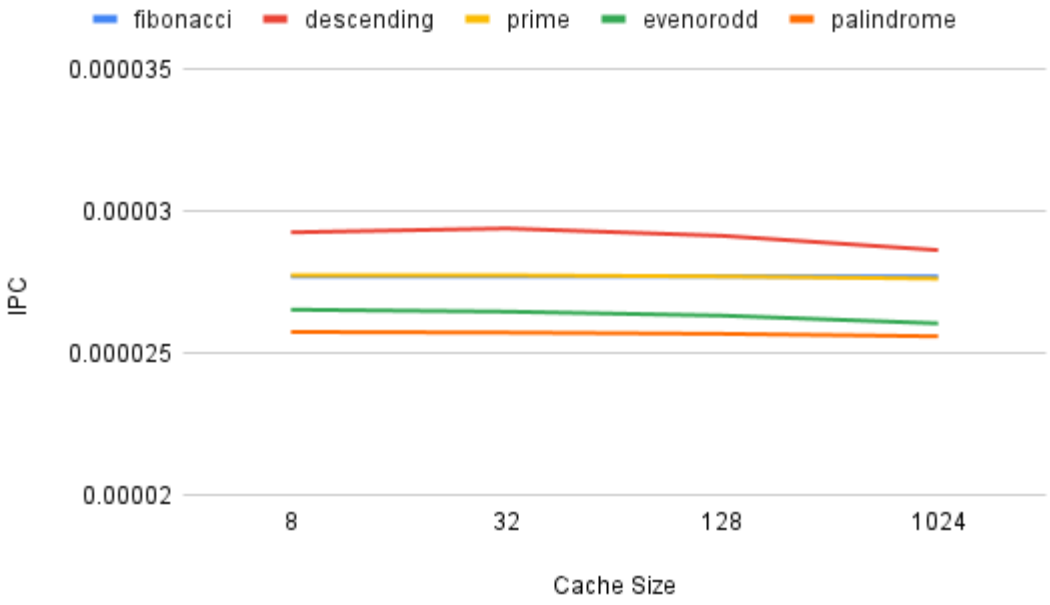
1) When L1i-cache is changed:

L1d=1024		8	32	128	1024
	evenorodd	0.0265252	0.026455026	0.02631579	0.026041666
	prime	0.027737226	0.027737226	0.027696794	0.02761628
	palindrome	0.025740026	0.025717959	0.02567394	0.025586354
	fibonacci	0.0276907	0.0276907	0.0276907	0.0276907
	descending	0.02924748	0.029384255	0.029125463	0.028621318



2) When L1d-cache is changed:

L1i=1024		8	32	128	1024
	evenorodd	0.0265252	0.026455026	0.02631579	0.026041666
	prime	0.027737226	0.027737226	0.027696794	0.02761628
	palindrome	0.025740026	0.025717959	0.02567394	0.025586354
	fibonacci	0.0276907	0.0276907	0.0276907	0.0276907
	descending	0.02924748	0.029384255	0.029125463	0.028621318



3) As the size of Cache size increases initially, IPC increases because cache is used instead of memory and latency is less than memory, after that we keep increasing cache size, then IPC decreases because max required cache is already reached at the peak, and after that we are again increasing the cache size, so the latency increases and IPC decreases.
4) We have chosen descending.asm as the benchmark. When L1-i cache is changed from 8B to 32B to 128B, the hit rate goes from 0.7082228 to 0.9811321 and then to 1.
   As cache size increases, hit rate increases as expected and then becomes constant as enough cache is present for the program.
5) We have chosen descending.asm as the benchmark. When L1-d cache is changed from 8B to 32B to 128B, the hit rate goes from 1 to 1 and then to 1.
   As the cache size increases, here the hit rate remains constant as the number of memory accesses are less.