CS 311: Computer Architecture Lab Report

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Our Normal Pipeline we are getting the values as shown below.

Program Name	No of Instructions	No of Cycles	CPI
descending.asm	377	467	1.2387
prime.asm	38	45	1.1842
evenorodd.asm	10	14	1.4
fibonacci.asm	106	128	1.2075
palindrome.asm	60	93	1.55

After modelling the latency for Memory access and ALU Execution we got these values

Program Name	No of Instructions	No of Cycles	CPI
descending.asm	377	17812	47.2466
prime.asm	38	1568	33.3684
evenorodd.asm	10	461	46.1
fibonacci.asm	106	4340	40.9433
palindrome.asm	60	2633	43.8833

We can see that the CPI for the latency model is a lot more than the normal pipelining. This is because the Instruction fetch stage needs to get the instructions every time form the memory which involves a lot of cycles. So that's the reason for the no of cycles to be more in the latency modelling scenario and the CPI is also almost 30-40 times the normal pipelining.