**SAMPLE QUESTIONS**

1. Assuming all number are in 2’s complement representation, which of the following numbers is divisible by 11111011?

(A) 11100111 (B) 11100100

(C) 11010111 (D) 11011011

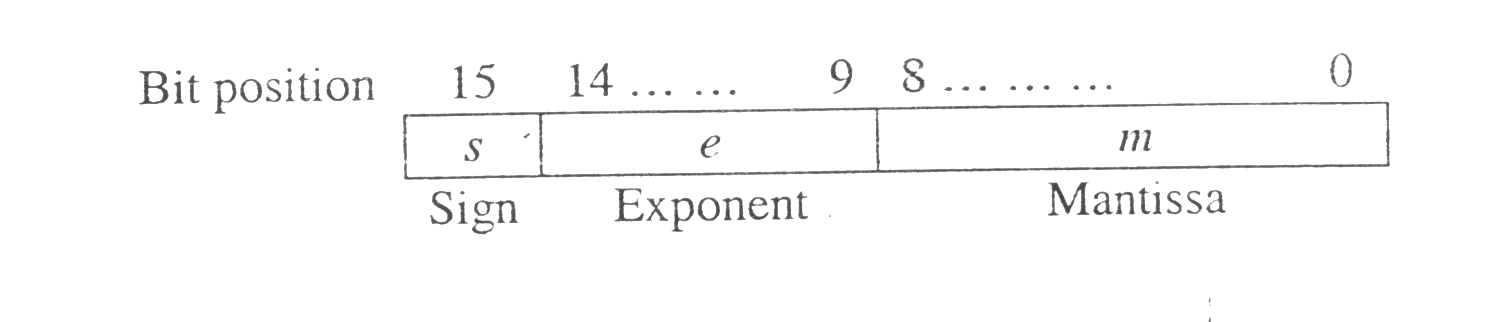
2. Let (S, ) be a partial order with two *minimal* elements a and b, and a maximum element c. Let P: S {**True, False**} be a predict defined on S. Suppose that P(a) = **True**, P(b) = **False** and P(x) P(y) for all x, y S satisfying x  y, y, where stands for logical implication. Which of the following statements CANNOT be true?

(A) P(x) = **True** for all x **S** such that x b

(B) P(x) = **False** for all x **S** such that xa and x c

(C) P(x) = **False** for all x **S** such that b x and x c

(D) P(x) = **False** for all x **S** such that a  x and b x

3. The following is a scheme for floating point number representation using 16 bits.

Let s, e, and m be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is:



What is the maximum difference between two successive real numbers representable in this system?

(A) 2−40 (B) 2−9 (C) 222 (D) 231

4. A 1−input, 2−output synchronous sequential circuit behaves as follows:

Let zk, nk denote the number of 0's and 1's respectively in initial k bits of the input (zk +nk = k). The circuit outputs 00 until one of the following conditions holds.

* zk –nk = 2. In this case, the output at the k–th and all subsequent clock ticks is 10.
* nk –zk = 2. In this case, the output at the k–th and all subsequent clock ticks is 01.

What is the minimum number of states required in the state transition graph of the above circuit?

(A) 5 (B) 6 (C) 7 (D) 8

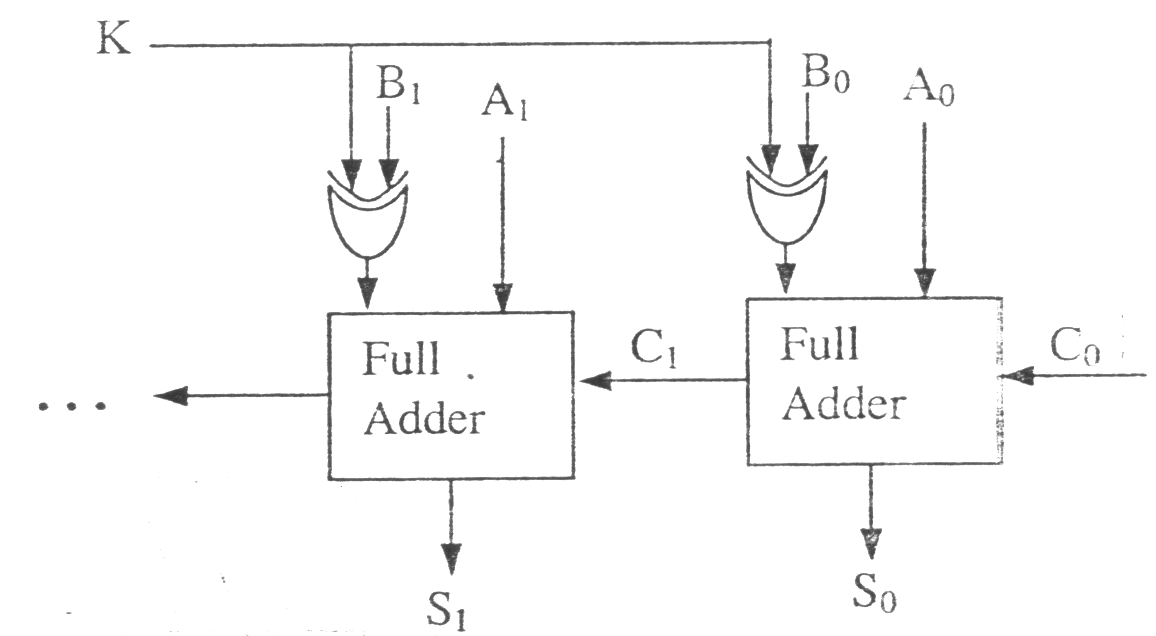
5. The literal count of a boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of (xy + xz’) is 4. What are the minimum possible literal counts of the product–of sum and sum–of–product representations respectively of the function given by the following Karnaugh map? Here, X denotes “don’t care”

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| zw  xy | **00** | **01** | **11** | **10** |
| **00** | X | 1 | 0 | 1 |
| **01** | 0 | 1 | X | 0 |
| **11** | 1 | X | X | 0 |
| **10** | X | 0 | 0 | X |

(A) (11, 9) (B) (9, 13)

(C) (9, 10) (D) (11, 11)

6. Consider the ALU shown below.



If the operands are in 2’s complement representation, which of the following operations can be performed by suitably setting the control lines K and C0 only (+ and – denote addition and subtraction respectively)?

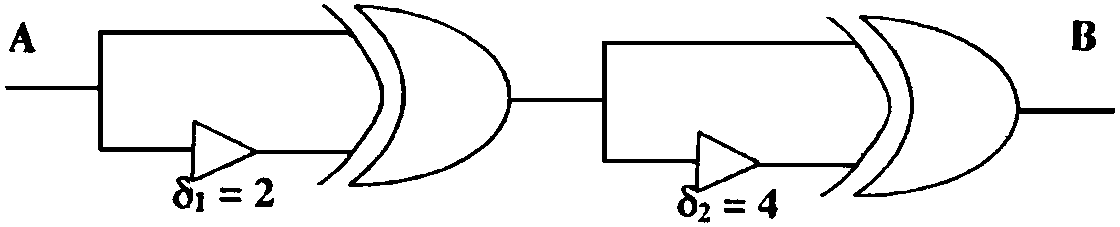
(A) A + B, and A – B, but not A + 1

(B) A + B, and A +1, but not A – B

(C) A + B, but not A – B or A + 1

(D) A + B, and A – B, and A + 1

7. Consider the following circuit composed of XOR gates and non–inverting buffers.



The non–inverting buffers have delays 1 = 2 ns and 2 = 4 ns as shown in the figure. Both XOR gates and all wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?

(a)  I1 + 4I2 + 11 I3 = 0

(b) I1 + 4I2 + 11 I3 = 0

(c) I1  4I2 + 11 I3 = 0

(d) I1 + 4I2 + 6 I3 = 0

8. Consider the following logic program P

A(x)  B(x, y), C(y)

B(x, x)

Which of the following first order sentences is equivalent to P?

(A) 

(B) 

(C) 

(D) 

9. The following resolution rule is used in logic programming

Derive clause (P  Q) from clauses (P  R), (Q  R).

Which of the following statements related to this rule is FALSE?

(A) ((PR)  is logically valid

(B)  is logically valid

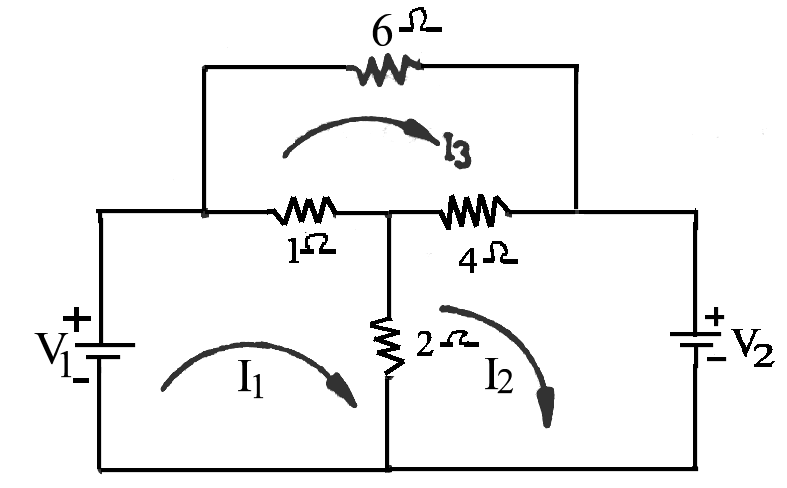
(C) (P Q) is satisfiable if and only if (P R) (Q R) is satisfiable

(D) (P  Q)  FALSE if and only if both P and Q are unsatisfiable

10. The Boolean function + xy +  is equivalent to

(A)  (B) x + y (C) x +  (D)  + y

11. A network is shown in the given figure. Which one of the following equation would represent the equation for loop 3?



(a) − I1  + 4I2 + 11 I3 = 0

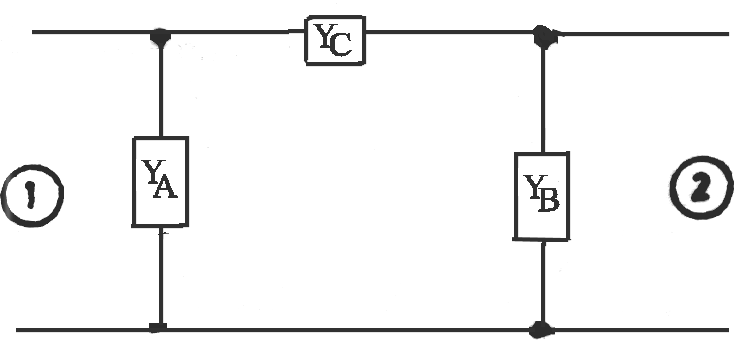
(b) I1  + 4I2 + 11 I3 = 0

(c) −I1 − 4I2 + 11 I3 = 0

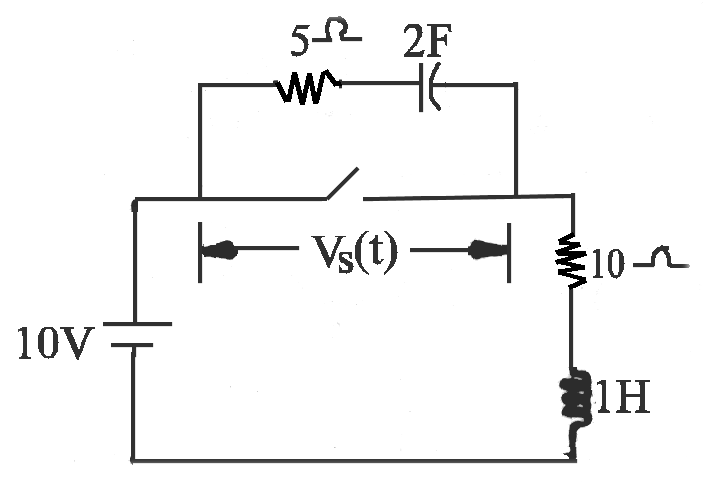
(d) I1  + 4I2 + 6 I3 = 0

12. In respect of the 2−port network shown in the figure, the admittance parameters are :

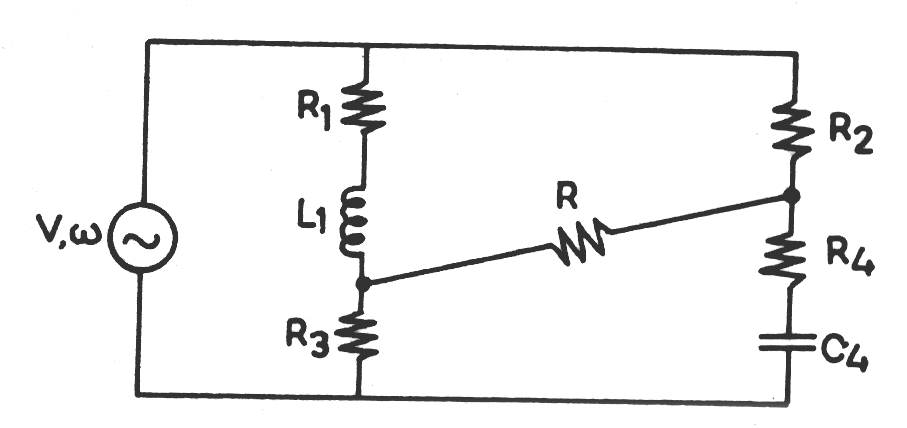
Y11 = 8 mho, Y12 = Y21 = −6 mho and Y22 = 6 mho.

 The values of YA, Y­B and YC ( in units of mho) will be respectively

(a) 2,6 and −6 (b) 2,6 and 0 (c) 2,0 and 6 (d) 2,6 and 8

13. In the network shown, the switch is opened at t = 0. Prior to that, the network was in the steady−state, VS(t) at t = 0 is

(a) 0 (b) 5 V (c) 10 V (d) 15 V

14. In the circuit shown in the figure, if the current in resistance ‘R’ is nil, then

(a)  (b) 

(c)  (d) 

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