Basic logic gates code:

```
module allgates(A, B, not1, or2, and3, nor4, nand5, xor6, xnor7);
        input A;
        input B;
        output not1;
        output or2;
        output and3;
        output nor4;
        output nand5;
        output xor6;
        output xnor7;

        reg not1;
        reg or2;
        reg and3;
        reg nor4;
        reg nand5;
        reg xor6;
        reg xnor7;

        always@(A or B)
        begin
                not1 = ~ A;
                or2 = A | B;
                and3 = A & B;
                nor4 = ~ (A | B);
                nand5 = ~ (A & B);
                xor6 = (A ^ B);
                xnor7 = ~ (A ^ B);
        end

endmodule
```

8*1 mux code:

```
module mux(d, sel, z);
   input [8:0] d;
   input [2:0] sel;
   output z;
reg  z ;
always @( d or sel)
begin
case(sel)
3'b000 : z=d[0];
3'b001 : z=d[1];
3'b010 : z=d[2];
3'b011 : z=d[3];
3'b100 : z=d[4];
3'b101 : z=d[5];
3'b110 : z=d[6];
3'b111 : z=d[7];
endcase
end
endmodule
```