Computer System Design Lab
Design Experiment 5a:
Processor Design

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1 Objective and Problem Statement:

The final outcome of this experiment is the working processor consisting of registers, buses, control signals etc. This experiment **excludes** the connection of RAM, ROM, and I/O devices.

In order to design the complete processor, the control and data path for instruction fetch (IF), instruction decode (ID), operand fetch (OF), execution (EX) and write back (WB) need to be designed. The design of CPU system is of *single cycle path*. To check the correctness of the design, the design need to be verified using the test benches.

2 Design and Verification

The following steps are involved in design and verification of the computer system. These steps need to be followed to get the final working computer system.

1. Processor Design: A single cycle data/control path need to be designed for the given Hack ISA. In this step all the paths designed for five different stages need to be connected. The design process could be very similar to the one discussed during lectures. (Note that in this experiment the connection of memory and I/O devices could be avoided.)
2. Processor Verification 1: Once the design is completed, carry out a verification process. A test bench (.tst) file need to be written and cross checked it against the compare file. To generate the test bench file automatically you can write a python program. The test bench file should consists of all the possible instruction of A-typ as well as C-type to test the working of processor.
3. Processor Verification 2: In this step the programs which are written as part of the Experiment 4 need to be executed. This needs to be done be incorporating the programs in .tst file. To make the process of writing the .tst file you may make use of python script.

3 Experimental Flow

1. Write the BHDL code and simulate it using the Hardware simulator.
2. The machine code for all the assembly instructions can be generated using Assembler tool.
3. Prepare the test bench (the .tst file) using the generated machine code. Similarly prepare the compare file for each machine instruction.
4. Prepare compare file for program counter (PC), D and A registers as well to check whether the intermediate values are correct.
5. All the address and data bus will be the primary input and output of the processor. (These buses will be connected to memory and I/O devices when the full computer system will be designed in subsequent experiments.)

4 Tools:

- Language: The Nand2Tetris HDL and TSL (test scripting language)
  Refer: Appendix A and B of text book.
- Tools: Hardware Simulator of Nand2Tetris.
  `https://www.nand2tetris.org/software`
- Machine and OS: x86_64 machines with any distribution of Linux (Ubuntu or CentOS).

5 Reporting and Evaluation

The evaluation will be carried out based on the efficient designing and correctness of the processor. All the test bench should pass to verification. Update the shared report with the learing from this experiment.

The experiment will be evaluated on 29^{th} Oct, 2020 along with viva-voce.