Text Books:

1. Sanjay Gupta, "**Virtual Instrumentation, LABVIEW"**, TMH, New Delhi, 2003
2. S. Gupta and J P Gupta,"**PC Interfacing for Data Acquisition and Process Control"**, Instrument Society of America, 1994

Reference Books:

3. Peter W Gofton , "**Understanding Serial Communication**", Sybes International, 2000
4. Robert H. Bishop, "**Learning with Lab-View**" Preticee Hall, 2009
5. Ernest O. Doeblin and Dhanesh N Manik, " **Measrement Systems – Application and Design"**, 5th Edn, TMH, 2007.

VII SEMESTER
COMPUTER COMMUNICATION NETWORKS

Subject Code	: **10EC71**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Layered tasks, OSI Model, Layers in OSI model, TCP?IP Suite, Addressing, Telephone and cable networks for data transmission, Telephone networks, Dial up modem, DSL, Cable TV for data transmission. 7 **Hrs**

UNIT - 2

DATA LINK CONTROL: Framing, Flow and error control, Protocols, Noiseless channels and noisy channels, HDLC. **6 Hrs**

UNIT - 3

MULTIPLE ACCESSES: Random access, Controlled access, Channelisation. **6 Hrs**

UNIT - 4

Wired LAN, Ethernet, IEEE standards, Standard Ethernet. Changes in the standards, Fast Ethernet, Gigabit Ethernet, Wireless LAN IEEE 802.11 **7 Hrs**

UNIT - 5

Connecting LANs, Backbone and Virtual LANs, Connecting devices, Back bone Networks, Virtual LANs **7 Hrs**

UNIT - 6
Network Layer, Logical addressing, Ipv4 addresses, Ipv6 addresses, Ipv4 and Ipv6 Transition from Ipv4 to Ipv6. **6 Hrs**

UNIT - 7
Delivery, Forwarding, Unicast Routing Protocols, Multicast Routing protocols. **6 Hrs**

UNIT - 8
Transport layer Process to process Delivery, UDP, TCP, Domain name system, Resolution. **7 Hrs**

TEXT BOOK:

1. **Data Communication and Networking**, B Forouzan**,** 4th Ed, TMH 2006

REFERENCE BOOKS:

4. **Computer Networks**, James F. Kurose, Keith W. Ross: Pearson education, 2nd Edition, 2003
5. **Introduction to Data communication and Networking**, Wayne Tomasi: Pearson education 2007

OPTICAL FIBER COMMUNICATION

Subject Code	: **10EC72**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1
OVERVIEW OF OPTICAL FIBER COMMUNICATION: Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, Ray theory, cylindrical fiber (no derivations in article 2.4.4), single mode fiber, cutoff wave length, mode filed diameter. Optical Fibers: fiber materials, photonic crystal, fiber optic cables specialty fibers. **7 Hrs**

UNIT - 2
TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS: Introduction, **A**ttenuation, absorption, scattering losses, bending loss, dispersion, Intra model dispersion, Inter model dispersion. **6 Hrs**

UNIT - 3

OPTICAL SOURCES AND DETECTORS: Introduction, LED's, LASER diodes, Photo detectors, Photo detector noise, Response time, double hetero junction structure, Photo diodes, comparison of photo detectors. **6 Hrs**

UNIT - 4

FIBER COUPLERS AND CONNECTORS: Introduction, fiber alignment and joint loss, single mode fiber joints, fiber splices, fiber connectors and fiber couplers. **6 Hrs**

UNIT - 5

OPTICAL RECEIVER: Introduction, Optical Receiver Operation, receiver sensitivity, quantum limit, eye diagrams, coherent detection, burst mode receiver, operation, Analog receivers. **6 Hrs**

UNIT - 6

ANALOG AND DIGITAL LINKS: Analog links – Introduction, overview of analog links, CNR, multichannel transmission techniques, RF over fiber, key link parameters, Radio over fiber links, microwave photonics.
Digital links – Introduction, point–to–point links, System considerations, link power budget, resistive budget, short wave length band, transmission distance for single mode fibers, Power penalties, nodal noise and chirping. **8 Hrs**

UNIT - 7

WDM CONCEPTS AND COMPONENTS: WDM concepts, overview of WDM operation principles, WDM standards, Mach-Zehender interferometer, multiplexer, Isolators and circulators, direct thin film filters, active optical components, MEMS technology, variable optical attenuators, tunable optical fibers, dynamic gain equalizers, optical drop multiplexers, polarization controllers, chromatic dispersion compensators, tunable light sources.
7 Hrs

UNIT - 8

Optical Amplifiers and Networks – optical amplifiers, basic applications and types, semiconductor optical amplifiers, EDFA.
OPTICAL NETWORKS: Introduction, SONET / SDH, Optical Interfaces, SONET/SDH rings, High – speed light – waveguides. **6 Hrs**

TEXT BOOKS:

1. **"Optical Fiber Communication"**, Gerd Keiser, 4th Ed., MGH, 2008.
2. **"Optical Fiber Communications"**, John M. Senior, Pearson Education. 3rd Impression, 2007.

REFERENCE BOOK:

1. **Fiber Optic Communication** - Joseph C Palais: 4th Edition, Pearson Education.

POWER ELECTRONICS

Subject Code	: **10EC73**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Introduction, Applications of power electronics, Power semiconductor devices, Control characteristics, Types of power electronics circuits, Peripheral effects. **6 Hrs**

UNIT - 2

POWER TRANSISTOR: Power BJT's, Switching characteristics, Switching limits, Base derive control, Power MOSFET's, Switching characteristics, Gate drive, IGBT's, Isolation of gate and base drives.

6 Hrs

UNIT - 3

INTRODUCTION TO THYRISTORS: Principle of operation states anode-cathode characteristics, Two transistor model. Turn-on Methods, Dynamic Turn-on and turn-off characteristics, Gate characteristics, Gate trigger circuits, di / dt and dv / dt protection, Thyristor firing circuits.

7 Hrs

UNIT - 4

CONTROLLED RECTIFIERS: Introduction, Principles of phase controlled converter operation, 1φ fully controlled converters, Duel converters, 1 φ semi converters (all converters with R & RL load).

7 Hrs

UNIT - 5

Thyristor turn off methods, natural and forced commutation, self commutation, class A and class B types, Complementary commutation, auxiliary commutation, external pulse commutation, AC line commutation, numerical problems. **7 Hrs**

UNIT - 6

AC VOLTAGE CONTROLLERS: Introduction, Principles of on and off control, Principles of phase control, Single phase controllers with restive loads and Inductive loads, numerical problems. **6 Hrs**

UNIT - 7

DC CHOPPERS: Introduction, Principles of step down and step up choppers, Step down chopper with RL loads, Chopper classification, Switch mode regulators – buck, boost and buck – boost regulators. **6 Hrs**

UNIT - 8

INVERTORS: Introduction, Principles of operation, Performance parameters, 1φ bridge inverter, voltage control of 1φ invertors, current source invertors, Variable DC link inverter.

7 Hrs

TEXT BOOKS:

4. **"Power Electronics" -** M. H. Rashid 3rd edition, PHI / Pearson publisher 2004.
5. **"Power Electronics" -** M. D. Singh and Kanchandani K.B. TMH publisher, 2nd Ed. 2007.

REFERENCE BOOKS:

6. **"Power Electronics, Essentials and Applications", L Umanand,** John Wiley India Pvt. Ltd, 2009.
7. **"Power Electronics"** , Daniel W. Hart, McGraw Hill, 2010.
8. **"Power Electronics**", V Nattarasu and R.S. Anandamurhty, **Pearson/Sanguine Pub. 2006.**

EMBEDED SYSTEM DESIGN

Subject Code	: **10EC74**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT 1:

Introduction to Embedded System: Introducing Embedded Systems, Philosophy, Embedded Systems, Embedded Design and Development Process. 5 **Hrs**

UNIT 2:

The Hardware Side: An Introduction, The Core Level, Representing Information, Understanding Numbers, Addresses, Instructions, Registers-A First Look, Embedded Systems-An Instruction Set View, Embedded Systems-A Register View, Register View of a Microprocessor
The Hardware Side: Storage Elements and Finite-State Machines (2 hour) The concepts of State and Time, The State Diagram, Finite State Machines-A Theoretical Model. **8 Hrs**

UNIT 3:

Memories and the Memory Subsystem: Classifying Memory, A General Memory Interface, ROM Overview, Static RAM Overview, Dynamic RAM Overview, Chip Organization, Terminology, A Memory Interface in Detail, SRAM Design, DRAM Design, DRAM Memory Interface, The Memory Map, Memory Subsystem Architecture, Basic Concepts of Caching, Designing a Cache System, Dynamic Memory Allocation. **7 Hrs**

UNIT 4:

Embedded Systems Design and Development : System Design and Development, Life-cycle Models, Problem Solving-Five Steps to Design, The Design Process, Identifying the Requirements, Formulating the Requirements Specification, The System Design Specification, System Specifications versus System Requirements, Partitioning and Decomposing a System, Functional Design, Architectural Design, Functional Model versus Architectural Model, Prototyping, Other Considerations, Archiving the Project. **6 Hrs**

UNIT 5 & 6:

Real-Time Kernels and Operating Systems: Tasks and Things, Programs and Processes, The CPU is a resource, Threads – Lightweight and heavyweight, Sharing Resources, Foreground/Background Systems, The operating System, The real time operating system (RTOS), OS architecture, Tasks and Task control blocks, memory management revisited.

12 Hrs

UNIT 7 & 8:

Performance Analysis and Optimization: Performance or Efficiency Measures, Complexity Analysis, The methodology, Analyzing code, Instructions in Detail, Time, etc. – A more detailed look, Response Time, Time Loading, Memory Loading, Evaluating Performance, Thoughts on Performance Optimization, Performance Optimization, Tricks of the Trade, Hardware Accelerators, Caches and Performance. **12 Hrs**

Text Book:

1. **Embedded Systems – A contemporary Design**

Tool, James K. Peckol**,** John Weily India Pvt. Ltd, 2008

Reference Books:

1. **Embedded Systems: Architecture and Programming,** Raj Kamal, TMH. 2008
2. **Embedded Systems Architecture – A Comprehensive Guide for Engineers and Programmers**, Tammy Noergaard, Elsevier Publication, 2005
3. **Programming for Embedded Systems**, Dreamtech Software Team, John Wiley India Pvt. Ltd, 2008

VLSI LAB

Subject Code	: **10ECL77**	IA Marks	: 25
No. of Practical Hrs/Week	: 03	Exam Hours	: 03
Total no. of Practical Hrs.	: 42	Exam Marks	: 50

(Wherever necessary Cadence/Synopsis/Menta Graphics tools must be used)

PART - A

DIGITAL DESIGN

ASIC-DIGITAL DESIGN FLOW

1. Write Verilog Code for the following circuits and their Test Bench for **verification**, observe the waveform and **synthesize** the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

1. An inverter
2. A Buffer
3. Transmission Gate
4. Basic/universal gates
5. Flip flop -RS, D, JK, MS, T
6. Serial & Parallel adder
7. 4-bit counter [Synchronous and Asynchronous counter]
8. Successive approximation register [SAR]

** An appropriate constraint should be given*

PART - B
ANALOG DESIGN

Analog Design Flow

1. Design an **Inverter** with given specifications*, completing the design flow mentioned below:
   a. **Draw the schematic** and verify the following
      i) DC Analysis
      ii) Transient Analysis
   b. **Draw the Layout** and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design
   e. Verify & Optimize for Time, Power and Area to the given constraint***

2. Design the following circuits with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.
      i) A Single Stage differential amplifier
      ii) Common source and Common Drain amplifier

3. Design an **op-amp** with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii). AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

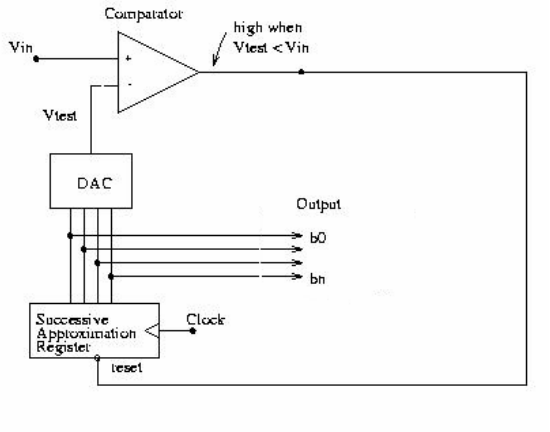
4. Design a **4 bit R-2R based DAC** for the given specification and completing the design flow mentioned using given op-amp in the library**.
   a. Draw the schematic and verify the following

i) DC Analysis
ii) AC Analysis
iii) Transient Analysis

b. Draw the Layout and verify the DRC, ERC
c. Check for LVS
d. Extract RC and back annotate the same and verify the Design.

5. For the **SAR based ADC** mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.

[Specifications to GDS-II]



***** Appropriate specification should be given.
** Applicable Library should be added & information should be given to the Designer.
*** An appropriate constraint should be given

POWER ELECTRONICS LAB

Subject Code	: **10ECL78**	IA Marks	: 25
No. of Practical Hrs/Week: 03		Exam Hours	: 03
Total no. of Practical Hrs. : 42		Exam Marks	: 50

Any five converter circuits experiment from the below list **must be** simulated using the **spice-simulator**.

- Static characteristics of SCR and DIAC.
- Static characteristics of MOSFET and IGBT.
- Controlled HWR and FWR using RC triggering circuit
- SCR turn off using i) LC circuit ii) Auxiliary Commutation
- UJT firing circuit for HWR and FWR circuits.
- Generation of firing signals for thyristors/ trials using digital circuits / microprocessor.
- AC voltage controller using triac – diac combination.
- Single phase Fully Controlled Bridge Converter with R and R-L loads.
- Voltage (Impulse) commutated chopper both constant frequency and variable frequency operations.
- Speed control of a separately exited DC motor.
- Speed control of universal motor.
- Speed control of stepper motor.
- Parallel / series inverter.

Note: Experiments to be conducted with isolation transformer and low voltage.

DSP ALGORITHMS AND ARCHITECTURE

Subject Code	: **10EC751**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **6 Hrs**

UNIT - 2

ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL-PROCESSORS: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. **7 Hrs**

UNIT - 3

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Introduction,

Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control. **6 Hrs**

UNIT - 4

Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor. **7 Hrs**

UNIT - 5

IMPLEMENTATION OF BASIC DSP ALGORITHMS: Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **7 Hrs**

UNIT - 6

IMPLEMENTATION OF FFT ALGORITHMS: Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS32OC54xx. **6 Hrs**

UNIT - 7

INTERFACING MEMORY AND PARALLEL I/O PERIPHERALS TO DSP DEVICES: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I / O Direct Memory Access (DMA). **6 Hrs**

UNIT - 8

INTERFACING AND APPLICATIONS OF DSP PROCESSOR: Introduction, Synchronous Serial Interface, A CODEC Interface Circuit. DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System. **7 Hrs**

TEXT BOOK:

4. **"Digital Signal Processing"**, Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

REFERENCE BOOKS:

1. **Digital Signal Processing: A practical approach**, Ifeachor E. C., Jervis B. W Pearson-Education, PHI/ 2002
2. **"Digital Signal Processors"**, B Venkataramani and M Bhaskar TMH, 2nd, 2010
3. **"Architectures for Digital Signal Processing"**, Peter Pirsch John Weily, 2008

MICRO AND SMART SYSTEMS TECHNOLOGY

Subject Code	:	**10MS752**	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

UNIT - 1

INTRODUCTION TO MICRO AND SMART SYSTEMS:

a) What are smart-material systems? Evolution of smart materials, structures and systems. Components of a smart system. Application areas. Commercial products.

b) What are microsystems? Feynman's vision. Micromachined transducers. Evolution of micro-manufacturing. Multi-disciplinary aspects. Applications areas. Commercial products. **6 Hrs**

UNIT - 2

MICRO AND SMART DEVICES AND SYSTEMS: PRINCIPLES AND MATERIALS:

a) Definitions and salient features of sensors, actuators, and systems.

b) Sensors: silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, fiber-optic gyroscope and surface-acoustic-wave based wireless strain sensor.

c) Actuators: silicon micro-mirror arrays, piezo-electric based inkjet print-head, electrostatic comb-drive and micromotor, magnetic micro relay, shape-memory-alloy based actuator, electro-thermal actuator.

d) Systems: micro gas turbine, portable clinical analyzer, active noise control in a helicopter cabin. **7 Hrs**

UNIT - 3

MICROMANUFACTURING AND MATERIAL PROCESSING:

a. Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization.
b. Silicon micromachining: surface, bulk, moulding, bonding based process flows.
c. Thick-film processing:
d. Smart material processing:
e. Processing of other materials: ceramics, polymers and metals
f. Emerging trends. **7 Hrs**

UNIT - 4

MODELING:

a. Scaling issues.
b. Elastic deformation and stress analysis of beams and plates. Residual stresses and stress gradients. Thermal loading. Heat transfer issues. Basic fluids issues.
c. Electrostatics. Coupled electromechanics. Electromagnetic actuation. Capillary electro-phoresis. Piezoresistive modeling. Piezoelectric modeling. Magnetostrictive actuators. **6 Hrs**

UNIT - 5

COMPUTER-AIDED SIMULATION AND DESIGN:

Background to the finite element element method. Coupled-domain simulations using Matlab. Commercial software. **6 Hrs**

UNIT - 6

ELECTRONICS, CIRCUITS AND CONTROL:

Carrier concentrations, semiconductor diodes, transistors, MOSFET amplifiers, operational amplifiers. Basic Op-Amp circuits. Charge-measuring circuits. Examples from microsystems. Transfer function, state-space modeling, stability, PID controllers, and model order reduction. Examples from smart systems and micromachined accelerometer or a thermal cycler. **7 Hrs**

UNIT - 7

INTEGRATION AND PACKAGING OF MICROELECTRO MECHANICAL SYSTEMS:

Integration of microelectronics and micro devices at wafer and chip levels. Microelectronic packaging: wire and ball bonding, flip-chip. Low-temperature-cofired-ceramic (LTCC) multi-chip-module technology. Microsystem packaging examples. **7 Hrs**

UNIT - 8

CASE STUDIES:

BEL pressure sensor, thermal cycler for DNA amplification, and active vibration control of a beam. **6 Hrs**

UNIT - 9

Mini-projects and class-demonstrations (<u>not for Examination</u>)

a) CAD lab (coupled field simulation of electrostatic-elastic actuation with fluid effect)

b) BEL pressure sensor
c) Thermal-cycler for PCR
d) Active control of a cantilever beam

TEXT BOOKS AND A CD-SUPPLEMENT:

1. **MEMS & Microsystems: Design and Manufacture,** Tai-Ran Tsu, Tata Mc-Graw-Hill.
2. **"Micro and Smart Systems"** by Dr. A.K.Aatre, Prof. Ananth Suresh, Prof.K.J.Vinoy, Prof. S. Gopalakrishna,, Prof. K.N.Bhat.,John Wiley Publications.

REFERENCE BOOKS:

2. Animations of working principles, process flows and processing techniques, A CD-supplement with Matlab codes, photographs and movie clips of processing machinery and working devices.
3. **Laboratory hardware kits for** (i) BEL pressure sensor, (ii) thermal-cycler and (iii) active control of a cantilever beam.

1. **Microsystems Design,** S. D. Senturia, 2001, Kluwer Academic Publishers, Boston, USA. ISBN 0-7923-7246-8.
2. **Analysis and Design Principles of MEMS Devices,** Minhang Bao, Elsevier, Amsterdam, The Netherlands, ISBN 0-444-51616-6.
3. **Design and Development Methodologies,** Smart Material Systems and MEMS: V. Varadan, K. J. Vinoy, S. Gopalakrishnan, Wiley.
4. **MEMS-** Nitaigour Premchand Mahalik, TMH 2007

ARTIFICIAL NEURAL NETWORKS

Subject Code	: **10EC753**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Introduction, history, structure and function of single neuron, neural net architectures, neural learning, use of neural networks. **6 Hrs**

UNIT - 2

Supervised learning, single layer networks, perceptions, linear separability, perceptions training algorithm, guarantees of success, modifications. **7 Hrs**

UNIT - 3

Multiclass networks-I, multilevel discrimination, preliminaries, back propagation, setting parameter values, theoretical results. **7 Hrs**

UNIT - 4

Accelerating learning process, application, mandaline, adaptive multilayer networks. **6 Hrs**

UNIT - 5

Prediction networks, radial basis functions, polynomial networks, regularization, unsupervised learning, winner take all networks. **6 Hrs**

UNIT - 6

Learning vector quantizing, counter propagation networks, adaptive resonance theorem, toplogically organized networks, distance based learning, neo-cognition. **7 Hrs**

UNIT - 7

Associative models, hop field networks, brain state networks, Boltzmann machines, hetero associations. **6 Hrs**

UNIT - 8

Optimization using hop filed networks, simulated annealing, random search, evolutionary computation. **7 Hrs**

TEXT BOOK:

1. **Elements of Artificial Neural Networks**, Kishan Mehrotra, C. K. Mohan, Sanjay Ranka, Penram, 1997.

REFERENCE BOOKS:

1. **Artificial Neural Networks**, R. Schalkoff, MGH, 1997.
2. **Introduction to Artificial Neural Systems**, J. Zurada, Jaico, 2003.
3. **Neural Networks,** Haykins, Pearson Edu., 1999.

CAD FOR VLSI

Subject Code	: **10EC754**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT – 1&2

INTRODUCTION TO VLSI METHODOLOGIES: VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabrication process and its impact on Physical Design. **12 Hrs**

UNIT – 3&4

A QUICK TOUR OF VLSI DESIGN AUTOMATION TOOLS: Data structures and Basic Algorithms, Algorithmic Graph theory and computational complexity, Tractable and Intractable problems. **14 Hrs**

UNIT – 5&6

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: partitioning, floor planning and pin assignment, placement, routing. **14 Hrs**

UNIT – 7&8

SIMULATION-LOGIC SYNTHESIS: Verification-High level synthesis - Compaction. Physical Design Automation of FPGAs, MCMS-VHDL-Verilog-Implementation of Simple circuits using VHDL and Verilog.

12 Hrs

REFERENCE BOOKS:

1. **"Algorithms for VLSI Physical Design Automation"**, N. A. Shervani, 1999.
2. **"Algorithms for VLSI Design Automation"**, S. H. Gerez, 1998.

APPLIED EMBEDDED SYSTEM DESIGN

Subject Code	: **10EC755**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART-A

Unit 1. Introduction to the Embedded Systems:
An embedded System, Processor embedded into a system (A). Embedded Hardware Units and devices in a system, Embedded software in a system, Examples of embedded systems,
Embedded system-on-chip (SoC) and use of VLSI circuits design technology (A), Complex systems design and processors, Design process in embedded system, Formalism of system design, Design process and design examples, Classification of embedded systems. Skills required for an embedded system designer**.** **5 Hours**

Unit 2. 8051 and Advanced Processor Architecture:
8051 Architecture, Real world interfacing, Introduction to advanced architecture
Processor and memory architecture, Instruction level parallelism, Performance metrics
Memory types and addresses, Processor selection, Memory selection
5 Hours

Unit 3. Devices and Communication Buses for Devices Network:
Devices and Communication buses for Networks, Serial communication devices
Parallel port devices, Sophisticated interfacing features in device ports, Wireless
communication devices, Timer and counting devices, Watchdog timers, Real time clocks
Parallel bus device protocols – parallel communication network using the ISA, PCI, PCI-X and
advanced buses, Wireless and mobile system protocols.
6 Hours

Unit 4. Device drivers and interrupts servicing mechanism:
Port or device access without interrupt servicing mechanism, Interrupt service routine, thread
and device driver concept, Interrupt sources, Interrupt servicing (handling) mechanism

Multiple interrupts, Context and the periods for context-switching, interrupt latency and

Deadline Classification of processors interrupt service mechanism from context saving angle

Direct memory access, Device driver programming, Parallel port device drivers in a system

Serial port device drivers in a system, Timer devices and devices interrupts **8 Hours**

PART-B

Unit 5. Programming concepts and embedded programming in C, C++ and Java:

Software programming in assembly language (ALP) and in high level language 'C'

'C' programming elements: header and source files and preprocessor directives

Program elements : macros and functions, Program elements: data types, data structures,

modifiers, statements, loops and pointers, Objected oriented programming

Embedded programming in Java, Optimisation of Memory needs. **5 Hours**

Unit 6. Program modeling concepts in single and multiprocessor systems software – development process:

Program models, Data flow graph models, State machine programming models for event

controlled programs, Modeling of multiprocessor systems, UML modeling **5 Hours**

Unit 7. Real time operating systems – I: Inter process communication and synchronization of processes, Task and Threads):

Multiple processes in an application, Multiple threads in an applications, Task

Tasks and states, Tasks and data, Clear cut distinction between Functions, ISRs and Tasks by

their Characteristics, Concept of semaphores, Shared data, Inter process communications

Signals, Semaphores, Message queues, Mailboxes, Pipes, Sockets, Remote procedure calls
(RPCs).

8 Hours

Unit 8. Real time operating systems:

Operating system service, Process management, Timer functions, Event functions,
Memory management, Device, file and IO subsystems management
Interrupt routines in RTOS environment and handling of interrupt source calls by RTOS
Introduction to Real Time Operating System, Basic design using a Real Time Operating
System, RTOS Task Scheduling Models, Latency, Response Times, Deadline as Performance
Metric, OS security issues, IEEE Standard POSIX 1003.1b Functions for Standardisation of
RTOS and Inter Process Communication Functions, Types of Real Time Operating Systems
RTOSµC/OS-II, RTOS Vx Works.

10 Hours

TEXTBOOK

Embedded System Architecture & Programming by Raj Kamal, TMH, 2008 (latest edition).

REFERENCE BOOKS

12. **Introduction to Embedded System Design – A certified Hardware / Software** by Bank Vahid, John Wikey & Sons, 2002.
13. **An embedded Software Primer** by David E Simon, Pearson Edition 1999.

Lab Work:(Part of the theory class)

5. Write C prog to iniitalise the I/O ports and interface the following:
   a. LED / LCD Display
   b. Stepper Motor
   c. Elevator

d. Dot – matrix Printer.

6. Write C Prog uisng ADC/DAC to perform various conversions.
7. Write C Prog for delay using in-built timer.
8. Write C prog for serial-communication using in-built 8251.
9. Write C prog for Scheduling algorithms like FIFO, SJF and Round-Robin
10. Implement Real-Time deadline algrithms.
11. Write C Prog. to control I/O devices (hard disk, speaker, etc).
12. Write C Prog to test the functions of Semaphore, Mutex, Lock etc.
13. Write C Prog to communicate between processes uisng Pipe, Send() & Recev(), IPC().
14. Write C Prog to perform matrix mulitpliation using pthreads.

Embedded Systems : Architecture, Programming, and Design,
Raj Kamal, 2nd Edn. TMH, 2008.

REFERENCE BOOKS:

1. **Embedded System Design – A certified Hardware / Software Introduction,** Frank Vahid, John Wikey & Sons, 2002.
2. **An embedded Software Primer** by David E Simon, Pearson Edition 1999.

SPEECH PROCESSING

Subject Code	: **10EC756**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

PRODUCTION AND CLASSIFICATION OF SPEECH SOUNDS: Introduction, mechanism of speech production. Acoustic phonetics: vowels, diphthongs, semivowels, nasals, fricatives, stops and affricates. **6 Hrs**

UNIT - 2

TIME-DOMAIN METHODS FOR SPEECH PROCESSING: time dependent processing of speech, short-time energy and average magnitude, short-time average zero crossing rate. **6 Hrs**

UNIT - 3

Speech vs. silence detection, pitch period estimation using parallel processing approach, short-time autocorrelation function. **7 Hrs**

UNIT - 4

Brief Applications of temporal processing of speech signals in synthesis, enhancement, hearing applications and clear speech. **7 Hrs**

UNIT - 5

FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING: Introduction, definitions and properties: Fourier transforms interpretation and linear filter interpretation, sampling rates in time and frequency. **7 Hrs**

UNIT - 6

Filter bank summation and overlap add methods for short-time synthesis of speech, sinusoidal and harmonic plus noise method of analysis/synthesis. **6 Hrs**

UNIT - 7

HOMOMORPHIC SPEECH PROCESSING: Introduction, homomorphic system for convolution, the complex cepstrum of speech, homomorphic vocoder.

6 Hrs

UNIT - 8

APPLICATIONS OF SPEECH PROCESSING: Brief applications of speech processing in voice response systems hearing aid design and recognition systems. **7 Hrs**

TEXT BOOK:

1. **Digital Processing of Speech Signals**, L. R. Rabiner and R. W. Schafer, Pearson Education Asia, 2004.

REFERENCE BOOKS:

15. **Discrete Time Speech Signal Processing**, T. F. Quatieri, Pearson Education Asia, 2004.

16. **Speech and Audio Signal Processing: Processing and Perception of Speech and Music**, B. Gold and N. Morgan, John Wiley India Pvt. Ltd, 2004.

ELECTIVE-3 (GROUP-C)
PROGRAMMING IN C++

Subject Code	: **10EC761**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

C++, AN OVERVIEW: Getting started, the C++ program, Preprocessor Directives, The Built-In Array Data Type, Dynamic Memory Allocation and Pointers, An Object – based Design, An Object-Oriented Design, An Exception – based Design, An array. **7 Hrs**

UNIT - 2

THE BASIC LANGUAGE: Literal Constant, Variables, Pointer Type, String Types, const Qualifier, Reference Types, the bool type, Enumeration types, Array types. The vector container type. **6 Hrs**

UNIT - 3

OPERATORS: Arithmetic Operators, Equality, Relational and Logical operators, Assignment operators, Increment and Decrement operator, The conditional Operator, Bitwise operator, bitset operations. Statements: if, switch, for Loop, while, break, goto, continue statements. **7 Hrs**

UNIT - 4

FUNCTIONS: Prototype, Argument passing, Recursion and linear function. **6 Hrs**

UNIT - 5

EXCEPTION HANDLING: Throwing an Exception, Catching an exception, Exception Specification and Exceptions and Design Issues. **7 Hrs**

UNIT - 6

CLASSES: Definition, Class Objects, Class Initailization, Class constructior, The class destructor, Class Object Arrays and Vectors. **7 Hrs**

UNIT - 7

Overload Operators, Operators ++ and --, Operators new and delete.

6 Hrs

UNIT - 8

Multiple Inheritances**,** public, private & protected inheritance, Class scope under Inheritance. **6 Hrs**

TEXT BOOK:

1. **C++ Primer**, S. B. Lippman & J. Lajoie, 3rd Edition, Addison Wesley, 2000.

REFERENCE BOOKS:

1. **C++ Program Design: An Introduction to Programming and Object- Oriented Design**. Cohoon and Davidson, 3rd Edn. TMH publication. 2004.
2. **Object Oriented Programming using C++**, R. Lafore, Galgotia Publications, 2004.

REAL-TIME SYSTEMS

Subject Code	: **10EC762**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION TO REAL-TIME SYSTEMS: Historical background, RTS Definition, Classification of Real-time Systems, Time constraints, Classification of Programs. **6 Hrs**

UNIT - 2

CONCEPTS OF COMPUTER CONTROL: Introduction, Sequence Control, Loop control, Supervisory control, Centralised computer control, Distributed system, Human-computer interface, Benefits of computer control systems.

6 Hrs

UNIT - 3

COMPUTER HARDWARE REQUIREMENTS FOR RTS: Introduction, General purpose computer, Single chip microcontroller, Specialized processors, Process-related Interfaces, Data transfer techniques, Communications, Standard Interface. **7 Hrs**

UNIT - 4

LANGUAGES FOR REAL-TIME APPLICATIONS: Introduction, Syntax layout and readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation, Data types, Control Structure, Exception Handling, Low-level facilities, Co routines, Interrupts and Device handling, Concurrency, Real-time support, Overview of real-time languages. **7 Hrs**

UNIT - 5 & 6

OPERATING SYSTEMS: Introduction, Real-time multi-tasking OS, Scheduling strategies, Priority Structures, Task management, Scheduler and real-time clock interrupt handles, Memory Management, Code sharing, Resource control, Task co-operation and communication, Mutual exclusion, Data transfer, Liveness, Minimum OS kernel, Examples. **14 Hrs**

UNIT - 7

DESIGN OF RTSS – GENERAL INTRODUCTION: Introduction, Specification documentation, Preliminary design, Single-program approach, Foreground/background, Multi-tasking approach, Mutual exclusion, Monitors. **6 Hrs**

UNIT - 8

RTS DEVELOPMENT METHODOLOGIES: Introduction, Yourdon Methodology, Requirement definition for Drying Oven, Ward and Mellor Method, Hately and Pirbhai Method. 6 **Hrs**

TEXT BOOKS:

4. **Real - Time Computer Control- An Introduction**, Stuart Bennet, 2nd Edn. Pearson Education. 2005.

REFERENCE BOOKS:

1. **Real-Time Systems Design and Analysis**, Phillip. A. Laplante, second edition, PHI, 2005.
2. **Real-Time Systems Development**, Rob Williams, Elsevier. 2006.
3. **Embedded Systems**, Raj Kamal, Tata Mc Graw Hill, India, 2005.

IMAGE PROCESSING

Subject Code	: **10EC763**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

DIGITAL IMAGE FUNDAMENTALS: What is Digital Image Processing. fundamental Steps in Digital Image Processing, Components of an Image processing system, elements of Visual Perception. **6 Hrs**

UNIT - 2

Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships between Pixels, Linear and Nonlinear Operations. **6 Hrs**

UNIT - 3

IMAGE TRANSFORMS: Two-dimensional orthogonal & unitary transforms, properties of unitary transforms, two dimensional discrete Fourier transform. **7 Hrs**

UNIT - 4

Discrete cosine transform, sine transform, Hadamard transform, Haar transform, Slant transform, KL transform. **7 Hrs**

UNIT - 5

IMAGE ENHANCEMENT: Image Enhancement in Spatial domain, Some Basic Gray Level Trans -formations, Histogram Processing, Enhancement Using Arithmetic/Logic Operations. **7 Hrs**

UNIT - 6

Basics of Spatial Filtering Image enhancement in the Frequency Domain filters, Smoothing Frequency Domain filters, Sharpening Frequency Domain filters, homomorphic filtering. 6 **Hrs**

UNIT - 7

Model of image degradation/restoration process, noise models, Restoration in the Presence of Noise, Only-Spatial Filtering Periodic Noise Reduction by Frequency Domain Filtering, Linear Position-Invariant Degradations, inverse filtering, minimum mean square error (Weiner) Filtering, **7 Hrs**

UNIT - 8

Color Fundamentals. Color Models, Pseudo color Image Processing., processing basics of full color image processing

6 Hrs

TEXT BOOK:

1. **"Digital Image Processing"**, Rafael C.Gonzalez, Richard E. Woods, etl , TMH , 2nd Edition 2010.

REFERENCE BOOKS:

1. **"Fundamentals of Digital Image Processing"**, Anil K. Jain, Pearson Education, 2001.
2. **"Digital Image Processing and Analysis"**, B. Chanda and D. Dutta Majumdar, PHI, 2003.

RADIO FREQUENCY INTEGRATED CIRCUITS

Subject Code	: **10EC764**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

OVERVIEW OF WIRELESS PRINCIPLES: A brief history of wireless systems, Noncellular wireless applications, Shannon, Modulations & Alphabet Soup, Propagation. 3 **Hrs**

PASSIVE RLC NETWORKS: Introduction, Parallel RLC Tank, Series RLC Networks, Other RLC networks, RLC Networks as impedance Transformers. **4 Hrs**

UNIT - 2

CHARACTERISTICS OF PASSIVE IC COMPONENTS: Introduction, Interconnect at radio frequencies: Skin effect, resisters, Capacitors, Inductors, Transformers, Interconnect options at high frequency. **6 Hrs**

UNIT - 3

A REVIEW OF MOS DEVICE PHYSICS: Introduction, A little history, FETs, MOSFET physics, The long – channels approximation, operation in weak inversion (sub threshold), MOS device physics in the short – channel regime, Other effects. **3 Hrs**

DISTRIBUTED SYSTEMS: Introduction, Link between lumped and distributed regimes driving-point impedance of iterated structures, Transmission lines in more detail, Behavior of Finite – length transmission lines, summary of transmission line equations, artificial lines. **4 Htrs**

UNIT - 4

THE SMITH CHART AND S-PARAMETERS: Introduction, The smith chart, S-parameters, Band Width Estimation Techniques, Introduction, The method of open – circuit time constant, The method of short circuit time constant, Risetime, Delay and bandwidth. **6 Hrs**

UNIT - 5

HIGH FREQUENCY AMPLIFIER DESIGN: Introduction, Zeros as bandwidth Enhancers, The shunt –series amplifier, Bandwidth Enhancement with f_T Doublers, Tuned amplifiers, Neutralization and unilateralization, Cascaded amplifiers, AM – PM conversion. **7 Hrs**

UNIT - 6

VOLTAGE REFERENCES AND BIASING: Introduction, Review of diode behavior, Diodes and bipolar transistors in CMOS technology, Supply –independent bias circuits, Bandgap voltage reference, Constant g_m bias. **Noise**: Introduction, Thermal noise, Shot noise, Flicker noise, Popcorn noise, Classical two- port noise theory, Examples of noise calculations, A handy rule of thumb, Typical noise performance. **6 Hrs**

UNIT - 7

LOW NOISE AMPLIFIER DESIGN: Introduction, Derivation of intrinsic MOSFET two-port noise parameters, LNA topologies: Power match versus noise match, Power-constrained noise optimization, Design examples, linearity and large signal performance, Spurious – free Dynamic range. **Mixers:** Introduction, Mixer fundamental, Nonlinear systems as linear mixers. **7 Hrs**

UNIT - 8

Multiplier – based mixers, Sub sampling mixers, Diode ring mixers, RF power amplifiers, Introduction, general considerations, Class A, AB, B and C power amplifier, Class D amplifiers, Class E amplifiers Class F amplifiers, Modulation of power amplifiers, summary of PA characteristics, RF PA design examples, additional design considerations, Design summery.

7 Hrs

TEXT BOOK:

1. **The design of CMOS radio-frequency integrated circuit**, Thomas H. Lee, 2nd edition Cambridge, 2004.

REFERENCE BOOK:

1. **Design of Analog CMOS integrated circuit**, Behzad Razavi, Tata Mc Graw Hill, 2005.

WAVELET TRANSFORMS

Subject Code	: **10EC765**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

CONTINUOUS WAVELET TRANSFORM: Introduction, C-T wavelets, Definition of CWT, The CWT as a correlation. Constant Q-Factor Filtering Interpolation and time frequency resolution, the CWT as an operator, inverse CWT. **6 Hrs**

UNIT - 2

INTRODUCTION TO DISCRETE WAVELET TRANSFORM AND ORTHOGONAL WAVELET DECOMPOSITION: Introduction. Approximation of vectors in nested linear vector spaces, (i) example of approximating vectors in nested subspaces of a finite dimensional liner vector space, (ii) Example of approximating vectors in nested subspaces of an infinite dimensional linear vector space. Example MRA. (i) Bases for the approximations subspaces and Harr scaling function, (ii) Bases for detail subspaces and Haar wavelet. **7 Hrs**

UNIT - 3

MRA, ORTHO NORMAL WAVELETS AND THEIR RELATIONSHIP TO FILTER BANKS: Introduction, Formal definition of an MRA. Construction of a general orthonormal MRA, (i) scaling function and subspaces, (ii) Implication of dilation equation and orthogonality, a wavelet basis for MRA. (i) Two scale relations for (t), (ii) Basis for the detail subspace (iii) Direct sum decomposition, Digital filtering interpolation (i) Decomposition filters, (ii) reconstruction, the signal. **7 Hrs**

UNIT - 4

EXAMPLES OF WAVELETS: Examples of orthogonal basis generating wavelets, (i) Daubechies D_4 scaling function and wavelet. (ii) band limited wavelets, Interpreting orthonormal MRAs for Discrete time MRA, (iii) Basis functions for DTWT. **6 Hrs**

UNIT - 5

ALTERNATIVE WAVELET REPRESENTATIONS: Introduction, Bi-orthogonal wavelet bases, Filtering relationship for bi-orthogonal filters, Examples of bi-orthogonal scaling functions and wavelets. 2-D wavelets.

6 Hrs

UNIT - 6

Non - separable multidimensional wavelets, wavelet packets. Wavelets Transform and Data Compression: Introduction, transform coding, DTWT for image compression (i) Image compression using DTWT and run-length encoding. **7 Hrs**

UNIT - 7

(i) Embedded tree image coding (ii) compression with JPEG audio compression (iii) Audio masking, (iv) Wavelet based audio coding.

6 Hrs

UNIT - 8

CONSTRUCTION OF SIMPLE WAVELETS: Construction of simple wavelets like Harr and DB1. Other Applications of Wavelet Transforms: Introduction, wavelet de-noising, speckle removal, edge detection and object isolation, Image fusions, Object detection by wavelet transforms of projections. **7 Hrs**

TEXT BOOK:

6. **Wavelet transforms- Introduction to theory and applications**, Raghuveer M.Rao and Ajit S. Bapardikar, Person Education, 2000.

REFERENCE BOOKS:

3. **Wavelet transforms,** Prasad and Iyengar, John Wiley India Pvt. Ltd, 2007.
4. **Wave-let and filter banks**, Gilbert Strang and Nguyen Wellesley Cambridge press, 1996
5. **Insight into WAVELETS from theory to practice,** K.P. Soman and K.L. Ramchandran, Eastern Economy Edition, 2008

MODELING AND SIMULATION OF DATA NETWORKS

Subject Code	: **10EC766**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT – 1&2

DELAY MODELS IN DATA NETWORKS: Queuing Models, M/M/1, M/M/m, M/M/□, M/M/m/m and other Markov System, M/G/1 System, Networks of Transmission Lines, Time Reversibility, Networks of Queues. **12 Hrs**

UNIT – 3&4

MULTI-ACCESS COMMUNICATION: Slotted Multi-access and the Aloha System, Splitting Algorithms, Carrier Sensing, Multi-access Reservations, Packet Radio Networks. **12 Hrs**

UNIT – 5&6

ROUTING IN DATA NETWORKS: Introduction, Network Algorithms and Shortest Path Routing, Broadcasting Routing Information: Coping with Link Failures, Flow models, Optimal Routing, and Topological Design, Characterization of Optimal Routing, Feasible Direction Methods for Optimal Routing, Projection Methods for Optimum Routing, Routing in the Codex Network. **14 Hrs**

UNIT – 7&8

FLOW CONTROL: Introduction, Window Flow Control, Rate Control Schemes, Overview of Flow Control in Practice, Rate Adjustment Algorithms. **14 Hrs**

REFERENCE BOOKS:

1. **"Data Networks"** Dimitri Bertsekas and Robert Gallager, 2nd edition, Prentice Hall of India, 2003.

2. **"High-Speed Networks and Internets"** William Stallings, Pearson Education (Asia) Pte. Ltd, 2004.
3. **"High Performance Communication Networks"** J. Walrand and P. Varaya, 2nd edition, Harcourt India Pvt. Ltd. & Morgan Kaufman, 2000.