ENGINEERING MATHEMATICS – III

Sub Code	**:**	**10MAT31**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

PART-A

UNIT-1

Fourier series

Convergence and divergence of infinite series of positive terms, definition and illustrative examples*

Periodic functions, Dirichlet's conditions, Fourier series of periodic functions of period 2π and arbitrary period, half range Fourier series. Complex form of Fourier Series. Practical harmonic analysis.

7 Hours

UNIT-2

Fourier Transforms

Infinite Fourier transform, Fourier Sine and Cosine transforms, properties, Inverse transforms

6 Hours

UNIT-3

Application of PDE

Various possible solutions of one dimensional wave and heat equations, two dimensional Laplace's equation by the method of separation of variables, Solution of all these equations with specified boundary conditions. D'Alembert's solution of one dimensional wave equation.

6 Hours

UNIT-4

Curve Fitting and Optimisation

Curve fitting by the method of least squares- Fitting of curves of the form $y = ax+b,\quad y=a\,x^2 + b\,x+c,\ y = a\,e^{bx},\ y = ax^b$

Optimization: Linear programming, mathematical formulation of linear programming problem (LPP), Graphical method and simplex method.

7 Hours

PART-B

UNIT-5

Numerical Methods - 1

Numerical Solution of algebraic and transcendental equations: Regula-falsi method, Newton - Raphson method. Iterative methods of solution of a system

of equations: Gauss-seidel and Relaxation methods. Largest eigen value and the corresponding eigen vector by Rayleigh's power method.

6 Hours

UNIT-6

Numerical Methods – 2

Finite differences: Forward and backward differences, Newton's forward and backward interpolation formulae. Divided differences - Newton's divided difference formula, Lagrange's interpolation formula and inverse interpolation formula.

Numerical integration: Simpson's one-third, three-eighth and Weddle's rules (All formulae/rules without proof)

7 Hours

UNIT-7

Numerical Methods – 3

Numerical solutions of PDE – finite difference approximation to derivatives, Numerical solution of two dimensional Laplace's equation, one dimensional heat and wave equations

7 Hours

UNIT-8

Difference Equations and Z-Transorms

Difference equations: Basic definition; Z-transforms – definition, standard Z-transforms, damping rule, shifting rule, initial value and final value theorems. Inverse Z-transform. Application of Z-transforms to solve difference equations.

6 Hours

Note: * In the case of illustrative examples, questions are not to be set.

Text Books:

1. B.S. Grewal, Higher Engineering Mathematics, Latest edition, Khanna Publishers.
2. Erwin Kreyszig, Advanced Engineering Mathematics, Latest edition, Wiley Publications.

Reference Books:

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O'Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd.Publishers.

3.

ANALOG ELECTRONIC CIRCUITS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES32**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Diode Circuits: Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers. **6 Hrs**

UNIT 2:

Transistor Biasing: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization. **6 Hrs**

UNIT 3:

Transistor at Low Frequencies: BJT transistor modeling, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Analysis of circuits r_e model; analysis of CE configuration using h- parameter model; Relationship between h-parameter model of CE,CC and CE configuration. **7 Hrs**

UNIT 4:

Transistor Frequency Response: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects. **7 Hrs**

UNIT 5:

(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections. **3 Hrs**

(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. Design procedures for the feedback amplifiers. **4 Hrs**

UNIT 6:

Power Amplifiers: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. Designing of Power amplifiers. **7 Hrs**

UNIT 7:

Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators. **6 Hrs**

UNIT 8:

FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks. **6 Hrs**

TEXT BOOK:

1. **"Electronic Devices and Circuit Theory",** Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9TH Edition.

REFERENCE BOOKS:

1. **'Integrated Electronics',** Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **"Electronic Devices and Circuits",** David A. Bell, PHI, 4th Edition, 2004
3. "**Analog Electronics Circuits: A Simplified Approach"**, U.B. Mahadevaswamy, Pearson/Saguine, 2007.

LOGIC DESIGN
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES33**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Principles of combinational logic-1: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations. **6 Hrs**

UNIT 2:

Principles of combinational Logic-2: Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables, Map entered variables. **7 Hrs**

UNIT 3:

Analysis and design of combinational logic - I: General approach, Decoders-BCD decoders, Encoders. **6 Hrs**

UNIT 4:

Analysis and design of combinational logic - II: Digital multiplexers-Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics.

7 Hrs

UNIT 5:

Sequential Circuits – 1: Basic Bistable Element, Latches, SR Latch, Application of SR Latch, A Switch Debouncer, The $\overline{S}\,\overline{R}$ Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop. **7 Hrs**

UNIT 6:

Sequential Circuits – 2: Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops **7 Hrs**

UNIT 7:

Sequential Design - I: Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis and Design.

6 Hrs

UNIT 8:

Sequential Design - II: Construction of state Diagrams, Counter Design.

6 Hrs

TEXT BOOKS:

1. **"Digital Logic Applications and Design"**, John M Yarbrough, Thomson Learning, 2001.
2. **"Digital Principles and Design ",** Donald D Givone, Tata McGraw Hill Edition, 2002.

REFERENCE BOOKS:

1. **"Fundamentals of logic design",** Charles H Roth, Jr; Thomson Learning, 2004.
2. **"Logic and computer design Fundamentals",** Mono and Kim, Pearson, Second edition, 2001.
3. **"Logic Design",** Sudhakar Samuel, Pearson/Saguine, 2007

NETWORK ANALYSIS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES34**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis With linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh. **7 Hrs**

UNIT 2:

Network Topology: Graph of a network, Concept of tree and co-tree, incidence matrix, tie-set, tie-set and cut-set schedules, Formulation of equilibrium equations in matrix form, Solution of resistive networks, Principle of duality**.** **7 Hrs**

UNIT 3:

Network Theorems – 1: Superposition, Reciprocity and Millman's theorems. **6 Hrs**

UNIT 4:

Network Theorems - II:

Thevinin's and Norton's theorems; Maximum Power transfer theorem **.** **6 Hrs**

UNIT 5: Resonant Circuits: Series and parallel resonance, frequency-response of series and Parallel circuits, Q –factor, Bandwidth.
7 Hrs

UNIT 6:
Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.
7 Hrs

UNIT 7:
Laplace Transformation & Applications : Solution of networks, step, ramp and impulse responses, waveform Synthesis. **6 Hrs**

UNIT 8:
Two port network parameters: Definition of z, y, h and transmission parameters, modeling with these parameters, relationship between parameters sets. **6 Hrs**

TEXT BOOKS:
1. **"Network Analysis",** M. E. Van Valkenburg, PHI / Pearson Education, 3rd Edition. Reprint 2002.
2. **"Networks and systems",** Roy Choudhury, 2nd edition, 2006 re-print, New Age International Publications.

REFERENCE BOOKS:
1. **"Engineering Circuit Analysis",** Hayt, Kemmerly and DurbinTMH 7th Edition, 2010
2. **"Basic Engineering Circuit Analysis"**, J. David Irwin / R. Mark Nelms, John Wiley, 8th ed, 2006.
3. **" Fundamentals of Electric Circuits"**, Charles K Alexander and Mathew N O Sadiku, Tata McGraw-Hill, 3 ed, 2009.

ELECTRONIC INSTRUMENTATION
(Common to EC/TC/IT/BM/ML)

Sub Code	**:**	**10IT35**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT – 1:

Introduction

(a) Measurement Errors: Gross errors and systematic errors, Absolute and relative errors, Accuracy, Precision, Resolution and Significant figures.

(b) Voltmeters and Multimeters Introduction, Multirange voltmeter, Extending voltmeter ranges, Loading, AC voltmeter using Rectifiers – Half wave and full wave, Peak responding and True RMS voltmeters.

3 + 4 Hrs

UNIT – 2:

Digital Instruments

Digital Voltmeters – Introduction, DVM's based on V – T, V – F and Successive approximation principles, Resolution and sensitivity, General specifications, Digital Multi-meters, Digital frequency meters, Digital measurement of time. **6 Hrs**

UNIT – 3:

Oscilloscopes

Introduction, Basic principles, CRT features, Block diagram and working of each block, Typical CRT connections, Dual beam and dual trace CROs, Electronic switch. **6 Hrs**

UNIT – 4:

Special Oscilloscopes

Delayed time-base oscilloscopes, Analog storage, Sampling and Digital storage oscilloscopes. **6 Hrs**

UNIT – 5:

Signal Generators

Introduction, Fixed and variable AF oscillator, Standard signal generator, Laboratory type signal generator, AF sine and Square wave generator, Function generator, Square and Pulse generator, Sweep frequency generator, Frequency synthesizer. **6 Hrs**

UNIT – 6:

Measurement of resistance, inductance and capacitance

Whetstone's bridge, Kelvin Bridge; AC bridges, Capacitance Comparison Bridge, Maxwell's bridge, Wein's bridge, Wagner's earth connection

5 **Hrs**

UNIT – 7:

Transducers - I

Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance thermometer, Thermistor, Inductive transducer, Differential output transducers and LVDT. **6 Hrs**

UNIT – 8:

Miscellaneous Topics

(a) Transducers - II –Piezoelectric transducer, Photoelectric transducer, Photovoltaic transducer, Semiconductor photo devices, Temperature transducers-RTD, Thermocouple .

(b) Display devices: Digital display system, classification of display, Display devices, LEDs, LCD displays.

(c) Bolometer and RF power measurement using Bolometer

(d) Introduction to Signal conditioning.

(e) Introduction to LabView. **10 Hrs**

TEXT BOOKS:

1. **"Electronic Instrumentation",** H. S. Kalsi, TMH, 3rd 2010
2. **"Electronic Instrumentation and Measurements",** David A Bell, PHI / Pearson Education, 2006.

REFERENCE BOOKS:

1. **"Principles of measurement systems",** John P. Beately, 3rd Edition, Pearson Education, 2000
2. **"Modern electronic instrumentation and measuring techniques",** Cooper D & A D Helfrick, PHI, 1998.
3. **Electronics & electrical measurements,** A K Sawhney, , Dhanpat Rai & sons, 9th edition.

FIELD THEORY
(Common to EC/TC/ML/EE)

Sub Code	**:**	**10ES36**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**04**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

a. Coulomb's Law and electric field intensity: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge. **3 Hrs**

b. **Electric flux density, Gauss' law and divergence:** Electric flux density, Gauss' law, Divergence, Maxwell's First equation(Electrostatics), vector

operator □ and divergence theorem. 3 **Hrs**

UNIT 2:

a. **Energy and potential :** Energy expended in moving a point charge in an electric field, The line integral, Definition of potential difference and Potential, The potential field of a point charge and system of charges, Potential gradient , Energy density in an electrostatic field. **4 Hrs**

b. Conductors, dielectrics and capacitance: Current and current density, Continuity of current, metallic conductors, Conductor properties and boundary conditions, boundary conditions for perfect Dielectrics, capacitance and examples. **4 Hrs**

UNIT 3:

Poisson's and Laplace's equations: Derivations of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solutions of Laplace's and Poisson's equations. **6 Hrs**

UNIT 4:

The steady magnetic field: Biot-Savart law, Ampere's circuital law, Curl, Stokes' theorem, magnetic flux and flux density, scalar and Vector magnetic potentials. **6 Hrs**

UNIT 5:

a. Magnetic forces: Force on a moving charge and differential current element, Force between differential current elements, Force and torque on a closed circuit. **4 Hrs**

b. Magnetic materials and inductance: Magnetization and permeability, Magnetic boundary conditions, Magnetic circuit, Potential energy and forces on magnetic materials, Inductance and Mutual Inductance. **4 Hrs**

UNIT 6:

Time varying fields and Maxwell's equations: Faraday's law, displacement current, Maxwell's equation in point and Integral form, retarded potentials. **6 Hrs**

UNIT 7:

Uniform plane wave: Wave propagation in free space and dielectrics, Poynting's theorem and wave power, propagation in good conductors – (skin effect). **6 Hrs**

UNIT 8:

Plane waves at boundaries and in dispersive media: Reflection of uniform plane waves at normal incidence, SWR, Plane wave propagation in general directions. **6 Hrs**

TEXT BOOK:

1. "Engineering Electromagnetics", William H Hayt Jr. and John A Buck**,** Tata McGraw-Hill, 7th edition, 2006

REFERENCE BOOKS:

1. **"Electromagnetics with Applications",** John Krauss and Daniel A Fleisch, McGraw-Hill, 5th edition, 1999
2. **"Electromagnetic Waves And Radiating Systems,"** Edward C. Jordan and Keith G Balmain, Prentice – Hall of India / Pearson Education, 2nd edition, 1968.Reprint 2002
3. **"Field and Wave Electromagnetics",** David K Cheng, Pearson Education Asia, 2nd edition, - 1989, Indian Reprint – 2001.

ANALOG ELECTRONICS LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ESL37**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**03**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**		**Exam Marks**	**:**	**50**

NOTE: Use the Discrete components to test the circuits. LabView can be used for the verification and testing along with the above.

1. Wiring of RC coupled Single stage FET & BJT amplifier and determination of the gain-frequency response, input and output impedances.

2. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances (Single circuit) (One Experiment)

3. Wiring of a two stage BJT Voltage series feed back amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback (One Experiment)

4. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for $f_0 \leq 10$ KHz

5. Testing for the performance of BJT – Hartley & Colpitts Oscillators for RF range $f_0 \geq 100$KHz.

6. Testing for the performance of BJT -Crystal Oscillator for f_0 > 100 KHz
7 Testing of Diode clipping (Single/Double ended) circuits for peak clipping, peak detection

8. Testing of Clamping circuits: positive clamping /negative clamping.
9. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.

10. Testing of Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency

11. Verification of Thevinin's Theorem and Maximum Power Transfer theorem for DC Circuits.

12. Characteristics of Series and Parallel resonant circuits.

LOGIC DESIGN LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ESL38**	**IA Marks**	**:**	**25**
Hrs/ Week	**:**	**03**	**Exam Hours**	**:**	**03**
Total Hrs.	**:**		**Exam Marks**	**:**	**50**

NOTE: Use discrete components to test and verify the logic gates. LabView can be used for designing the gates along with the above.

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
   (ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).

10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.