VI SEMESTER

DIGITAL COMMUNICATION

Subject Code	: **10EC61**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Basic signal processing operations in digital communication. Sampling Principles: Sampling Theorem, Quadrature sampling of Band pass signal, Practical aspects of sampling and signal recovery. **7 Hrs**

UNIT - 2

PAM, TDM. Waveform Coding Techniques, PCM, Quantization noise and SNR, robust quantization. **6 Hrs**

UNIT - 3

DPCM, DM, applications. Base-Band Shaping for Data Transmission, Discrete PAM signals, power spectra of discrete PAM signals. **7 Hrs**

UNIT - 4

ISI, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern, base-band M-ary PAM systems, adaptive equalization for data transmission. **6 Hrs**

UNIT - 5

DIGITAL MODULATION TECHNIQUES: Digital Modulation formats, Coherent binary modulation techniques, Coherent quadrature modulation techniques. Non-coherent binary modulation techniques. **6 Hrs**

UNIT - 6

Detection and estimation, Model of DCS, Gram-Schmidt Orthogonalization procedure, geometric interpretation of signals, response of bank of correlators to noisy input. **6 Hrs**

UNIT - 7

Detection of known signals in noise, correlation receiver, matched filter receiver, detection of signals with unknown phase in noise. **7 Hrs**

UNIT - 8

Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum, coherent binary PSK, frequency hop spread spectrum, applications. **7 Hrs**

TEXT BOOK:

1. **Digital communications**, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

REFERENCE BOOKS:

1. **Digital and Analog communication systems,** Simon Haykin, John Wildy India Lts, 2008
2. **An introduction to Analog and Digital Communication**, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 2008.
3. **Digital communications** - Bernard Sklar: Pearson education 2007

MICROPROCESSOR

Subject Code	: **10EC62**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

8086 PROCESSORS: Historical background, The microprocessor-based personal computer system, 8086 CPU Architecture, Machine language instructions, Instruction execution timing. **6 Hrs**

UNIT - 2

INSTRUCTION SET OF 8086: Assembler instruction format, data transfer and arithmetic, branch type, loop, NOP & HALT, flag manipulation, logical and shift and rotate instructions. Illustration of these instructions with example programs, Directives and operators. **6 Hrs**

UNIT - 3

BYTE AND STRING MANIPULATION: String instructions, REP Prefix, Table translation, Number format conversions, Procedures, Macros, Programming using keyboard and video display. **7 Hrs**

UNIT - 4

8086 INTERRUPTS: 8086 Interrupts and interrupt responses, Hardware interrupt applications, Software interrupt applications, Interrupt examples. **7 Hrs**

UNIT - 5

8086 INTERFACING: Interfacing microprocessor to keyboard (keyboard types, keyboard circuit connections and interfacing, software keyboard

interfacing, keyboard interfacing with hardware), Interfacing to alphanumeric displays (interfacing LED displays to microcomputer), Interfacing a microcomputer to a stepper motor. **7 Hrs**

UNIT - 6

8086 BASED MULTIPROCESSING SYSTEMS: Coprocessor configurations, The 8087 numeric data processor: data types, processor architecture, instruction set and examples. **6 Hrs**

UNIT - 7

SYSTEM BUS STRUCTURE: Basic 8086 configurations: minimum mode, maximum mode, Bus Interface: peripheral component interconnect (PCI) bus, the parallel printer interface (LPT), the universal serial bus (USB)

6 Hrs

UNIT - 8

80386, 80486 AND PENTIUM PROCESSORS: Introduction to the 80386 microprocessor, Special 80386 registers, Introduction to the 80486 microprocessor, Introduction to the Pentium microprocessor. **7 Hrs**

TEXT BOOKS:

4. **Microcomputer systems-The 8086 / 8088** Family – Y.C. Liu and G. A. Gibson, 2E PHI -2003
5. **The Intel Microprocessor, Architecture, Programming and Interfacing**-Barry B. Brey, 6e, Pearson Education / PHI, 2003

REFERENCE BOOKS:

2. **Microprocessor and Interfacing- Programming & Hardware**, Douglas hall, 2nd , TMH, 2006.
3. **Advanced Microprocessors and Peripherals** - A.K. Ray and K.M. Bhurchandi, TMH, 2nd , 2006.
4. **8088 and 8086 Microprocessors - Programming, Interfacing, Software, Hardware & Applications** - Triebel and Avtar Singh, 4e, Pearson Education, 2003

MICROELECTRONICS CIRCUITS

Subject Code	: **10EC63**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT – 1

MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation modes, single stage MOS amplifiers. MOSFET internal capacitances and high frequency modes, Frequency response of CS amplifiers, CMOS digital logic inverter, detection type MOSFET. **7 Hrs**

UNIT -2

Single Stage IC Amplifier: IC Design philiosophy, CoUmparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response. **6 Hrs**

UNIT – 3

Single Stage IC amplifiers (continued): CS and CF amplifiers with loads, high frequency response of CS and CF amplifiers, CG and CB amplifiers with active loads, high frequency response of CG and CB amplifiers, Cascade amplifiers. CS and CE amplifiers with source (emitter) degeneration source and emitter followers, some useful transfer parings, current mirrors with improved performance. SPICE examples. **6 Hrs**

UNIT – 4

Differences and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers. Multistage amplifier. SPICE examples. **7 Hrs**

UNIT – 5

Feedback. General Feedback structure. Properties of negative feedback. Four basic feedback topologies. Series-Shunt feedback. Determining the loop gain. Stability problem. Effect of feedback an amplifier poles. Stability study using Bode plots. Frequency compensation. SPICE examples. **7 Hrs**

UNIT - 6

Operational Amplifiers: The two stage CMOS Op-amp, folded cascade CMOS op-amp, 741 op-amp circuit, DC analysis of the 741, small signal analysis of 741, gain, frequency response and slew rate of 741. Data Converters. A-D and D-A converters. **6 Hrs**

UNIT – 7 & 8

Digital CMOS circuits. Overview. Design and performance analysis of CMOS inverter. Logic Gate Circuits. Pass-transistor logic. Dynamic Logic Circuits. SPICE examples. **12 Hrs**

Text Book:

1. "Microelectronic Circuits", Adel Sedra and K.C. Smith, 5th Edition, Oxford University Press, Interantional Version, 2009.

Reference Book:

1. "**Fundamentals of Microelectronics**" , Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
2. **"Microelectronics – Analysis and Design"**, Sundaram Natarajan, Tata McGraw-Hill, 2007

ANTENNAS AND PROPAGATION

Subject Code	: **10EC64**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

ANTENNA BASICS: Introduction, basic Antenna parameters, patterns, beam area, radiation intensity, beam efficiency, diversity and gain, antenna apertures, effective height, bandwidth, radiation, efficiency, antenna temperature and antenna filed zones. **7 Hrs**

UNIT - 2

POINT SOURCES AND ARRAYS: Introduction, point sources, power patterns, power theorem, radiation intensity, filed patterns, phase patterns. Array of two isotropic point sources. Endfire array and Broadside array. **6 Hrs**

UNIT - 3

ELECTRIC DIPOLES AND THIN LINEAR ANTENNAS: Introduction, short electric dipole, fields of a short dipole(no derivation of field components), radiation resistance of short dipole, radiation resistances of

lambda/2 Antenna, thin linear antenna, micro strip arrays, low side lobe arrays, long wire antenna, folded dipole antennas. **7 Hrs**

UNIT - 4 & 5

LOOP, SLOT, PATCH AND HORN ANTENNA: Introduction, small loop, comparison of far fields of small loop and short dipole, loop antenna general case, far field patterns of circular loop, radiation resistance, directivity, slot antenna, Babinet's principle and complementary antennas, impedance of complementary and slot antennas, patch antennas, horn antennas, rectangular horn antennas. **12 Hrs**

UNIT - 6

ANTENNA TYPES: Helical Antenna, Yagi-Uda array, corner reflectors, parabolic reflectors, log periodic antenna, lens antenna, antenna for special applications – sleeve antenna, turnstile antenna, omni directional antennas, antennas for satellite antennas for ground penetrating radars, embedded antennas, ultra wide band antennas, plasma antenna, high-resolution data, intelligent antennas, antenna for remote sensing. **8 Hrs**

UNIT - 7 & 8

RADIO WAVE PROPAGATION: Introduction, Ground wave propagation, free space propagation, ground reflection, surface wave, diffraction.

TROPOSPHERE WAVE PROPAGATION: Troposcopic scatter, Ionosphere propagation, electrical properties of the ionosphere, effects of earth's magnetic field. **10 Hrs**

TEXT BOOKS:

1. **Antennas and Wave Propagation**, John D. Krauss, 4th Edn,McGraw-Hill International edition, 2010.
2. **Antennas and Wave Propagation** - Harish and Sachidananda: Oxford Press 2007

REFERENCE BOOKS:

1. **Antenna Theory Analysis and Design** - C A Balanis, 3rd Edn, John Wiley India Pvt. Ltd, 2008
2. **Antennas and Propagation for Wireless Communication Systems** - Sineon R Saunders, John Wiley, 2003.
3. **Antennas and wave propagation** - G S N Raju: Pearson Education 2005

OPERATING SYSTEMS

Subject Code	: **10EC65**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION AND OVERVIEW OF OPERATING SYSTEMS: Operating system, Goals of an O.S, Operation of an O.S, Resource allocation and related functions, User interface related functions, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems, distributed operating systems. **6 Hrs**

UNIT - 2

STRUCTURE OF THE OPERATING SYSTEMS: Operation of an O.S, Structure of the supervisor, Configuring and installing of the supervisor, Operating system with monolithic structure, layered design, Virtual machine operating systems, Kernel based operating systems, and Microkernel based operating systems. **7 Hrs**

UNIT - 3

PROCESS MANAGEMENT: Process concept, Programmer view of processes, OS view of processes, Interacting processes, Threads, Processes in UNIX, Threads in Solaris**.** **6 Hrs**

UNIT - 4

MEMORY MANAGEMENT: Memory allocation to programs, Memory allocation preliminaries, Contiguous and noncontiguous allocation to programs, Memory allocation for program controlled data, kernel memory allocation. 7 **Hrs**

UNIT - 5

VIRTUAL MEMORY: Virtual memory basics, Virtual memory using paging, Demand paging, Page replacement, Page replacement policies, Memory allocation to programs, Page sharing, UNIX virtual memory. **6 Hrs**

UNIT - 6

FILE SYSTEMS: File system and IOCS, Files and directories, Overview of I/O organization, Fundamental file organizations, Interface between file system and IOCS, Allocation of disk space, Implementing file access, UNIX file system. **7 Hrs**

UNIT - 7

SCHEDULING: Fundamentals of scheduling, Long-term scheduling, Medium and short term scheduling, Real time scheduling, Process scheduling in UNIX. **6 Hrs**

UNIT - 8

MESSAGE PASSING: Implementing message passing, Mailboxes, Inter process communication in UNIX. 7 **Hrs**

TEXT BOOK:

1. **"Operating Systems - A Concept based Approach"**, D. M. Dhamdhare, TMH, 3rd Ed, 2010.

REFERENCE BOOK:

1. **Operating Systems Concepts**, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th Edition, 2001.
2. **Operating System – Internals and Design Systems**, Willaim Stalling, Pearson Education, 4th Ed, 2006.
3. **Design of Operating Systems,** Tennambhaum, TMH, 2001.

ADVANCED COMMUNICATION LAB

Subject Code	: **10ECL67**	IA Marks	: 25
No. of Practical Hrs/Week: 03		Exam Hours	: 03
Total no. of Practical Hrs. : 42		Exam Marks	: 50

LIST OF EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW – 2009 can be used for verification and testing.

1. TDM of two band limited signals.
2. ASK and FSK generation and detection
3. PSK generation and detection
4. DPSK generation and detection
5. QPSK generation and detection
6. PCM generation and detection using a CODEC Chip
7. Measurement of losses in a given optical fiber (propagation loss, bending loss) and numerical aperture

8. Analog and Digital (with TDM) communication link using optical fiber.
9. Measurement of frequency, guide wavelength, power, VSWR and attenuation in a microwave test bench
10. Measurement of directivity and gain of antennas: Standard dipole (or printed dipole), microstrip patch antenna and Yagi antenna (printed).
11. Determination of coupling and isolation characteristics of a stripline (or microstrip) directional coupler
12. (a) Measurement of resonance characteristics of a microstrip ring resonator and determination of dielectric constant of the substrate.
    (b) Measurement of power division and isolation characteristics of a microstrip 3 dB power divider.

MICROPROCESSOR LAB

Subject Code	: **10ECL68**	IA Marks	: 25
No. of Practical Hrs/Week: 03		Exam Hours	: 03
Total no. of Practical Hrs. : 42		Exam Marks	: 50

I) **Programs involving**

1) Data transfer instructions like:
   - i] Byte and word data transfer in different addressing modes.
   - ii] Block move (with and without overlap)
   - iii] Block interchange

2) Arithmetic & logical operations like:
   - i] Addition and Subtraction of multi precision nos.
   - ii] Multiplication and Division of signed and unsigned Hexadecimal nos.
   - iii] ASCII adjustment instructions
   - iv] Code conversions
   - v] Arithmetic programs to find square cube, LCM, GCD, factorial

3) Bit manipulation instructions like checking:
   - i] Whether given data is positive or negative
   - ii] Whether given data is odd or even
   - iii] Logical 1's and 0's in a given data
   - iv] 2 out 5 code
   - v] Bit wise and nibble wise palindrome

4) Branch/Loop instructions like:
   i] Arrays: addition/subtraction of N nos.
      Finding largest and smallest nos.
      Ascending and descending order
   ii] Near and Far Conditional and Unconditional jumps, Calls and Returns

5) Programs on String manipulation like string transfer, string reversing, searching for a string, etc.

6) Programs involving Software interrupts
   Programs to use DOS interrupt INT 21h Function calls for Reading a Character from keyboard, Buffered Keyboard input, Display of character/ String on console

II) Experiments on interfacing 8086 with the following interfacing modules through DIO (Digital Input/Output-PCI bus compatible) card
   a) Matrix keyboard interfacing
   b) Seven segment display interface
   c) Logical controller interface
   d) Stepper motor interface

III) Other Interfacing Programs
   a) Interfacing a printer to an X86 microcomputer
   b) PC to PC Communication

ELECTIVE – GROUP A
ANALOG AND MIXED MODE VLSI DESIGN

Subject Code	: **10EC661**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

(Text Book 1)

UNIT 1

Data converter fundamentals: Analog versus Digital Discrete Time Signals, Converting Analog Signals to Data Signals, Sample and Hold Characteristics, DAC Specifications, ADC Specifications, Mixed-Signal Layout Issues.

7 Hrs

UNIT 2

Data Converters Architectures: DAC Architectures, Digital Input Code, Resistors String, R-2R Ladder Networks, Current Steering, Charge Scaling

DACs, Cyclic DAC, Pipeline DAC, ADC Architectures, Flash, 2-Step Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. **12 Hrs**

UNIT 3

Non-Linear Analog Circuits: Basic CMOS Comparator Design (Excluding Characterization), Analog Multipliers, Multiplying Quad (Excluding Stimulation), Level Shifting (Excluding Input Level Shifting For Multiplier). **7 Hrs**

(Text Book 2)

UNIT 4:

Data Converter SNR: Improving SNR Using Averaging (Excluding Jitter & Averaging onwards), Decimating Filters for ADCs (Excluding Decimating without Averaging onwards), Interpolating Filters for DAC, Band pass and High pass Sync filters. **8 Hrs**

UNIT 5

Su-Microns CMOS circuit design: Process Flow, Capacitors and Resistors, MOSFET Switch (upto Bidirectional Switches), Delay and adder Elements, Analog Circuits MOSFET Biasing (upto MOSFET Transition Frequency). **10 Hrs**

UNIT 6

OPAmp Design (Excluding Circuits Noise onwards) **8 Hrs**

TEXT BOOK:

1. **Design, Layout, Stimulation ,**R. Jacob Baker, Harry W Li, David E Boyce, CMOS Circuit, PHI Education, 2005
2. **CMOS- Mixed Signal Circuit Design ,**R. Jacob Baker, (Vol II of CMOS: Circuit Design, Layout and Stimulation), John Wiley India Pvt. Ltd, 2008.

REFERENCE BOOKS:

1. **Design of Analog CMOS Integrated Circuits**, B Razavi, First Edition, McGraw Hill,2001.
2. **CMOS Analog Circuit Design**, P e Allen and D R Holberg, 2nd Edition, Oxford University Press,2002.

SATELLITE COMMUNICATION

Subject Code	: **10EC662**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

OVER VIEW OF SATELLITE SYSTEMS: Introduction, frequency allocation, INTEL Sat. **6 Hrs**

UNIT - 2

ORBITS: Introduction, Kepler laws, definitions, orbital element, apogee and perigee heights, orbit perturbations, inclined orbits, calendars, universal time, sidereal time, orbital plane, local mean time and sun synchronous orbits, Geostationary orbit: Introduction, antenna, look angles, polar mix antenna, limits of visibility, earth eclipse of satellite, sun transit outage, leandiag orbits. **7 Hrs**

UNIT - 3

PROPAGATION IMPAIRMENTS AND SPACE LINK: Introduction, atmospheric loss, ionospheric effects, rain attenuation, other impairments.

SPACE LINK: Introduction, EIRP, transmission losses, link power budget, system noise, CNR, uplink, down link, effects of rain, combined CNR.

7 Hrs

UNIT - 4

SPACE SEGMENT: Introduction, power supply units, altitude control, station keeping, thermal control, TT&C, transponders, antenna subsystem.

6 Hrs

UNIT - 5 & 6

EARTH SEGEMENT: Introduction, receive only home TV system, out door unit, indoor unit, MATV, CATV, Tx – Rx earth station. **5 Hrs**

INTERFERENCE AND SATELLITE ACCESS: Introduction, interference between satellite circuits, satellite access, single access, pre-assigned FDMA, SCPC (spade system), TDMA, pre-assigned TDMA, demand assigned TDMA, down link analysis, comparison of uplink power requirements for TDMA & FDMA, on board signal processing satellite switched TDMA. **9 Hrs**

UNIT - 7 & 8

DBS, SATELLITE MOBILE AND SPECIALIZED SERVICES: Introduction, orbital spacing, power ratio, frequency and polarization,

transponder capacity, bit rates for digital TV, satellite mobile services, USAT, RadarSat, GPS, orb communication and Indian Satellite systems.

12 Hrs

TEXT BOOK:

13. **Satellite Communications**, Dennis Roddy, 4th Edition, McGraw-Hill International edition, 2006.

REFERENCES BOOKS:

3. **Satellite Communications**, Timothy Pratt, Charles Bostian and Jeremy Allnutt, 2nd Edition, John Wiley Pvt. Ltd & Sons, 2008.
4. **Satellite Communication Systems Engineering**, W. L. Pitchand, H. L. Suyderhoud, R. A. Nelson, 2nd Ed., Pearson Education., 2007.

RANDOM PROCESSES

Subject Code	: **10EC663**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION TO PROBABILITY THEORY: Experiments, sample space, Events, Axioms, Assigning probabilities, Joint and conditional probabilities, Baye's Theorem, Independence, Discrete Random Variables, Engg Example. **7 Hrs**

UNIT - 2

Random Variables, Distributions, Density Functions: CDF, PDF, Gaussian random variable, Uniform Exponential, Laplace, Gamma, Erlang, Chi-Square, Raleigh, Rician and Cauchy types of random variables.

6 Hrs

UNIT - 3

OPERATIONS ON A SINGLE R V: Expected value, EV of Random variables, EV of functions of Random variables, Central Moments, Conditional expected values. **7 Hrs**

UNIT - 4

Characteristic functions, Probability generating functions, Moment generating functions, Engg applications, Scalar quantization, entropy and source coding.

6 Hrs

UNIT - 5

Pairs of Random variables, Joint CDF, joint PDF, Joint probability mass functions, Conditional Distribution, density and mass functions, EV involving pairs of Random variables, Independent Random variables, Complex Random variables, Engg Application. **7 Hrs**

UNIT - 6

MULTIPLE RANDOM VARIABLES: Joint and conditional PMF, CDF, PDF,.EV involving multiple Random variables, Gaussian Random variable in multiple dimension, Engg application, linear prediction. **6 Hrs**

UNIT - 7

RANDOM PROCESS: Definition and characterization, Mathematical tools for studying Random Processes, Stationary and Ergodic Random processes, Properties of ACF. **6 Hrs**

UNIT - 8

EXAMPLE PROCESSES: Markov processes, Gaussian Processes, Poisson Processes, Engg application, Computer networks, Telephone networks.

7 Hrs

TEXT BOOK:

1. **Probability and random processes: application to Signal processing and communication** - S L Miller and D C Childers**:** Academic Press / Elsivier 2004

REFERENCE BOOKS:

4. **Probability, Random variables and stochastic processes** - A. Papoullis and S U Pillai: McGraw Hill 2002
5. **Probability, Random variables and Random signal principles** - Peyton Z Peebles**:** TMH 4th Edition 2007
6. **Probability, random processes and applications** - H Stark and Woods**:** PHI 2001

LOW POWER VLSI DESIGN

Subject Code	: **10EC664**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT – 1

Introduction, Sources of power dissipation, designing for low power. Physics of power dissipation in MOSFET devices – MIS Structure, Long channel and sub-micron MOSFET, Gate induced Drain leakage. **6 Hrs**

UNIT - 2

Power dissipation in CMOS – Short circuit dissipation, dynamic dissipation, Load capacitance. Low power design limits - Principles of low power design, Hierarchy of limits, fundamental limits, Material, device, circuit and system limits. **8 Hrs**

UNIT – 3&4

SYNTHESIS FOR LOW POWER: Behavioral, Logic and Circuit level approaches, Algorithm level transforms, Power-constrained Least squares optimization for adaptive and non-adaptive filters, Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre- computation, FSM and Combinational logic, Transistor sizing. **12 Hrs**

UNIT – 5&6

DESIGN AND TEST OF LOW-VOLTAGE CMOS CIRCUITS: Introduction, Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect, Low voltage design techniques using reverse V_{gs}, steep sub threshold swing and multiple threshold voltages, Testing with elevated intrinsic leakage, multiple supply voltages. **12 Hrs**

UNIT - 7

LOW ENERGY COMPUTING: Energy dissipation in transistor channel, Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and I/O Buffer, supply clock generation. **7 Hrs**

UNIT - 8

SOFTWARE DESIGN FOR LOW POWER: Introduction, sources of power dissipation, power estimation and optimization. **7 Hrs**

TEXT BOOK:

1. **Low-Power CMOS VLSI Circuit Design**, Kaushik Roy and Sharat C Prasad, John Wiley Pvt. Ltd, 2008.

DATA STRUCTURE USING C++

Subject Code	: **10EC665**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION: Functions and parameters, Dynamic memory allocation classis, Testing and debugging. Data Representation, Introduction, Linear lists, Formula-based representation linked representation, Indirect addressing simulating pointers. **7 Hrs**

UNIT - 2

ARRAYS AND MATRICS: Arrays, Matrices, Special matrices spare matrices. **6 Hrs**

UNIT - 3

STACKS: The abstract data types, Derived classed and inheritance, Formula-based representation, Linked representation, Applications. **7 Hrs**

UNIT - 4

Queues: The abstract data types, Derived classes and inheritance, Formula-based representation, Linked Linked representation, Applications. **6 Hrs**

UNIT - 5

SKIP LISTS AND HASHING: Dictionaries, Linear representation, Skip list presentation, Hash table representation. **6 Hrs**

UNIT - 6

BINARY AND OTHER TREES: Trees, Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT and class extensions. 8 **Hrs**

UNIT - 7

PRIRITY QUEUES: Linear lists, Heaps, Leftist trees. **6 Hrs**

UNIT-8

Search Trees: Binary search trees, B-trees, Applications. **6 Hrs**

TEXT BOOK:

1. **Data structures, Algorithms, and applications in C++ -** Sartaj Sahni, McGraw Hill.2000.

REFERENCE BOOKS:

1. **Object Oriented Programming in C++** - Balaguruswamy. TMH, 1995.
2. **Programming in C++** - Balaguruswamy. TMH, 4th, 2010 .

DIGITAL SYSTEMS DESIGN USING VERILOG

Subject Code	: **10EC666**	IA Marks	: 25
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

UNIT 1

Introduction and Methodology:

Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology. 7 **Hrs**

UNIT 2

Combinational Basics:

Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

7 Hrs

UNIT 3

Number Basics:

Unsigned and Signed Integers, Fixed and Floating-point Numbers. **6 Hrs**

UNIT 4

Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology. 6 **Hrs**

UNIT 5

Memories: Concepts, Memory Types, Error Detection and Correction.

Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **7 Hrs**

UNIT 6

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **6 Hrs**

UNIT 7

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. **6 Hrs**

UNIT 8

Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test,

7 Hrs

Test Book:

1. **"Digital Design: An Embedded Ssytems Approach Using VERILOG", Peter J. Ashenden, Elesvier, 2010.**

VIRTUAL INSTRUMENTATION

Subject Code	: **10EC668**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT 1

Review of Digital Instrumentation: Representation of analog signals in the digital domain – Review of quantization in amplifier and time areas, sample and hold, sampling theorem, ADC and DAC. **8 Hrs**

UNIT 2 & 3

Fundamentals of Virtual Instrumentation: Concept of Virtual Instrumentation – PC based data acquisition – Typical on board DAQ card – Resolution and sampling frequency – Multiplexing of analog inputs – Single-ended and differential inputs – Different strategies for sampling of multi channel analog inputs. Concept of universal DAQ card – Use of timer-counter and analog outputs on the universal DAQ card. **12 Hrs**

UNIT 4

Cluster of Instruments in System: Interfacing of external instruments to a PC – RS 232C, RS – 422, RS 485 and USB standards – IEEE 488 standard – ISO –OSI model for series bus – introduction to bus protocols of MOD bus and CAN bus. 8 **Hrs**

UNIT 5 & 6

Graphical Programming Environment in VI: Concepts of graphical programming – Lab-view software – Concept of VIs and sub VIs – Display types – Digital – Analog – Chart – Oscilloscope types – Loops – Case and sequence structures – Types of data – Arrays – Formulate nodes – Local and Global variables – String and file I/O. 12 **Hrs**

UNIT 7 & 8

Analysis Tools and Simple Application in VI: Fourier transform – Power spectrum – Correlation – Windowing and filtering tools – Simple temperature indicator – ON/OFF controller – PID controller – CRO emulation – Simulation of a simple second order system – Generation of HTML page.

12 Hrs

Text Books:

1. Sanjay Gupta, "**Virtual Instrumentation, LABVIEW"**, TMH, New Delhi, 2003
2. S. Gupta and J P Gupta,"**PC Interfacing for Data Acquisition and Process Control"**, Instrument Society of America, 1994

Reference Books:

3. Peter W Gofton , "**Understanding Serial Communication**", Sybes International, 2000
4. Robert H. Bishop, "**Learning with Lab-View**" Preticee Hall, 2009
5. Ernest O. Doeblin and Dhanesh N Manik, " **Measrement Systems – Application and Design"**, 5th Edn, TMH, 2007.

VII SEMESTER
COMPUTER COMMUNICATION NETWORKS

Subject Code	: **10EC71**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Layered tasks, OSI Model, Layers in OSI model, TCP?IP Suite, Addressing, Telephone and cable networks for data transmission, Telephone networks, Dial up modem, DSL, Cable TV for data transmission. 7 **Hrs**

UNIT - 2

DATA LINK CONTROL: Framing, Flow and error control, Protocols, Noiseless channels and noisy channels, HDLC. **6 Hrs**

UNIT - 3

MULTIPLE ACCESSES: Random access, Controlled access, Channelisation. **6 Hrs**

UNIT - 4

Wired LAN, Ethernet, IEEE standards, Standard Ethernet. Changes in the standards, Fast Ethernet, Gigabit Ethernet, Wireless LAN IEEE 802.11 **7 Hrs**

UNIT - 5

Connecting LANs, Backbone and Virtual LANs, Connecting devices, Back bone Networks, Virtual LANs **7 Hrs**