ENGINEERING MATHEMATICS – III

CODE: 10 MAT 31 **IA Marks: 25**
Hrs/Week: 04 **Exam Hrs: 03**
Total Hrs: 52 **Exam Marks:100**

PART-A

Unit-I: FOURIER SERIES

Convergence and divergence of infinite series of positive terms, definition and illustrative examples*
Periodic functions, Dirichlet's conditions, Fourier series of periodic functions of period 2π and arbitrary period, half range Fourier series. Complex form of Fourier Series. Practical harmonic analysis. **[7 hours]**

Unit-II: FOURIER TRANSFORMS

Infinite Fourier transform, Fourier Sine and Cosine transforms, properties, Inverse transforms **[6 hours]**

Unit-III: APPLICATIONS OF PDE

Various possible solutions of one dimensional wave and heat equations, two dimensional Laplace's equation by the method of separation of variables, Solution of all these equations with specified boundary conditions. D'Alembert's solution of one dimensional wave equation.

[6 hours]

Unit-IV: CURVE FITTING AND OPTIMIZATION

Curve fitting by the method of least squares- Fitting of curves of the form $y = ax+b$, $y=a x^2 + b x+c$, $y = a e^{bx}$, $y = ax^b$

Optimization: Linear programming, mathematical formulation of linear programming problem (LPP), Graphical method and simplex method.

[7 hours]

PART-B

Unit-V: NUMERICAL METHODS - 1

Numerical Solution of algebraic and transcendental equations: Regula-falsi method, Newton - Raphson method. Iterative methods of solution of a system of equations:

Gauss-seidel and Relaxation methods. Largest eigen value and the corresponding eigen vector by Rayleigh's power method.

[6 hours]

Unit-VI: NUMERICAL METHODS – 2

Finite differences: Forward and backward differences, Newton's forward and backward interpolation formulae. Divided differences - Newton's divided difference formula, Lagrange's interpolation formula and inverse interpolation formula.

Numerical integration: Simpson's one-third, three-eighth and Weddle's rules (All formulae/rules without proof)

[7 hours]

Unit-VII: NUMERICAL METHODS – 3

Numerical solutions of PDE – finite difference approximation to derivatives, Numerical solution of two dimensional Laplace's equation, one dimensional heat and wave equations **[7 hours]**

Unit-VIII: DIFFERENCE EQUATIONS AND Z-TRANSFORMS

Difference equations: Basic definition; Z-transforms – definition, standard Z-transforms, damping rule, shifting rule, initial value and final value theorems. Inverse Z-transform. Application of Z-transforms to solve difference equations.

[6 hours]

Note: * In the case of illustrative examples, questions are not to be set.

Text Books:

1. B.S. Grewal, Higher Engineering Mathematics, Latest edition, Khanna Publishers
2. Erwin Kreyszig, Advanced Engineering Mathematics, Latest edition, Wiley Publications.

Reference Book:

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O'Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd.Publishers

ANALOG ELECTRONIC CIRCUITS

(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES32**	***IA Marks***	**:**	**25**
Hrs/ Week	**:**	**04**	Exam Hours	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Diode Circuits: Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers.
6 Hours

UNIT 2:

Transistor Biasing: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization. **6 Hours**

UNIT 3:

Transistor at Low Frequencies: BJT transistor modeling, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Analysis of circuits r_e model; analysis of CE configuration using h- parameter model; Relationship between h-parameter model of CE,CC and CE configuration. **7 Hours**

UNIT 4:

Transistor Frequency Response: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects. **7 Hours**

UNIT 5:

(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections.
3 Hours

(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. Design procedures for the feedback amplifiers.
4 Hours

UNIT 6:

Power Amplifiers: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. Designing of

Power amplifiers. **7 Hours**

UNIT 7:

Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only)

Simple design methods of Oscillators. **6 Hours**

UNIT 8:

FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks.

6 Hours

TEXT BOOK:

1. **"Electronic Devices and Circuit Theory",** Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9TH Edition.

REFERENCE BOOKS:

1. **'Integrated Electronics',** Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **"Electronic Devices and Circuits",** David A. Bell, PHI, 4th Edition, 2004
3. "**Analog Electronics Circuits: A Simplified Approach"**, U.B. Mahadevaswamy, Pearson/Saguine, 2007.

LOGIC DESIGN

(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ES33**	***IA Marks***	**:**	**25**
Hrs/ Week	**:**	**04**	Exam Hours	**:**	**03**
Total Hrs.	**:**	**52**	**Exam Marks**	**:**	**100**

UNIT 1:

Principles of combinational logic-1: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations. **6 Hours**

UNIT 2:

Principles of combinational Logic-2: Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables, Map entered variables. **7 Hours**

UNIT 3:
Analysis and design of combinational logic - I: General approach, Decoders-BCD decoders, Encoders. **6 Hours**

UNIT 4:
Analysis and design of combinational logic - II: Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics.

7 Hours

UNIT 5:
Sequential Circuits – 1: Basic Bistable Element, Latches, SR Latch, Application of SR Latch, A Switch Debouncer, The $\overline{S}\,\overline{R}$ Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop. **7 Hours**

UNIT 6:
Sequential Circuits – 2: Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops **7 Hours**

UNIT 7:
Sequential Design - I: Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis and Design.

6 Hours

UNIT 8:
Sequential Design - II: Construction of state Diagrams, Counter Design.

6 Hours

TEXT BOOKS:
1. **"Digital Logic Applications and Design"**, John M Yarbrough, Thomson Learning, 2001.
2. **"Digital Principles and Design ",** Donald D Givone, Tata McGraw Hill Edition, 2002.

REFERENCE BOOKS:
1. **"Fundamentals of logic design",** Charles H Roth, Jr; Thomson Learning, 2004.
2. **"Logic and computer design Fundamentals",** Mono and Kim, Pearson, Second edition, 2001.
3. **"Logic Design",** Sudhakar Samuel, Pearson/Saguine, 2007

10ES34 NETWORK ANALYSIS (Common to EC/TC/EE/IT/BM/ML)

Subject Code	:	10ES34	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART – A

UNIT 1:

Basic Concepts: Basic definitions. Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh.

7 Hours

UNIT 2:

Network Topology: Graph of a network, Concept of tree and co-tree, incidence matrix, tie-set and cut-set schedules, Formulation of equilibrium equations in matrix form, solution of resistive networks, principle of duality**.**

7 Hours

UNIT 3:

Network Theorems – 1: Superposition, Reciprocity and Millman's theorems

6 Hours

UNIT 4:

Network Theorems - II:

Thevenin's and Norton's theorems, Maximum Power transfer theorem

6 Hours

PART – B

UNIT 5:

Resonant Circuits: Series and parallel resonance, frequency-response of series and parallel circuits, Q factor, Bandwidth. **6Hours**

UNIT 6:

Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations. **7 Hours**

UNIT 7:

Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis

7 Hours

UNIT 8:

Two port network parameters: Definition of z, y, h and transmission parameters, modeling with these parameters, relationship between parameters sets

6 Hours

TEXT BOOKS:

1. **Engineering Circuit Analysis,** Hayt, Kemmerly and Durbin,TMH ,7th Edition, 2010
2. **Networks and systems,** Roy Choudhury, New Age International Publications.,2nd edition, 2006 re-print,

REFERENCE BOOKS:

1. **Electric Circuits,** Schaum's Outlines,M Nahvi & J A Edminister,TMH,5th Edition,2009**.**
2. **Network Analysis,** M. E. Van Valkenburg, PHI, 3rd Edition, Reprint 2009.

3. **Analysis of Linear Systems**, David K. Cheng, Narosa Publishing House, 11th reprint, 2002

10EE35 ELECTRICAL and ELECTRONIC MEASUREMENTS and INSTRUMENTATION

Subject Code	:	10EE35	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART – A

UNIT 1:

1-(a) Units and Dimensions: Review of fundamental and derived units. S.I. units. Dimensional equations, problems. **3 Hours**

1-(b) Measurement of Resistance: Wheatstone's bridge, sensitivity, limitations. Kelvin's double bridge. Earth resistance, measurement by fall of potential method and by using Megger. **3 Hours**

UNIT 2:

Measurement of Inductance and Capacitance: Sources and detectors, Maxwell's inductance bridge, Maxwell's inductance &capacitance bridge,Hay's bridge, Anderson's bridge, Desauty's bridge, Schering bridge. Shielding of bridges. Problems. **07 Hours**

UNIT 3:

Extension of Instrument Ranges: Shunts and multipliers. Construction and theory of instrument transformers, Equations for ratio and phase angle errors of C.T. and P.T (derivations excluded). Turns compensation, illustrative examples (excluding problems on turns compensation),Silsbees's method of testing CT. **07 Hours**

UNIT 4:

Measurement of Power and Energy: Dynamometer wattmeter. UPF and LPF wattmeters, Measurement of real and reactive power in three-phase circuits. Induction type energy meter — construction, theory, errors, adjustments and calibration. Principle of working of electronic energy meter. 0**6 Hours**

PART – B

UNIT 5:

(a) Construction and operation of electro-dynamometer single-phase power factor meter. Weston frequency meter and phase sequence indicator. 0**4 Hours**

(b) Electronic Instruments: Introduction. True RMS responding voltmeter. Electronic multimeters. Digital voltmeters. Q meter. 0**4 Hours**

UNIT 6:

Dual trace oscilloscope — front panel details of a typical dual trace oscilloscope. Method of measuring voltage, current, phase, frequency and period. Use of Lissajous patterns. Working of a digital storage oscilloscope. Brief note on current probes. 0**6 Hours**

UNIT 7:

Transducers: Classification and selection of transducers. Strain gauges. LVDT. Measurement of temperature and pressure. Photo-conductive and photo-voltaic cells.

0**6 Hours**

UNIT 8:

(a) Interfacing resistive transducers to electronic circuits. Introduction to data acquisition systems.

2 Hours

(b) Display Devices and Signal Generators: X-Y recorders. Nixie tubes. LCD and LED display. Signal generators and function generators. **4 Hours**

Text Books

1. **Electrical and Electronic Measurements and Instrumentation,** A. K. Sawhney, Dhanpatrai and Sons, New Delhi.
2. **Modern Electronic Instrumentation and Measuring Techniques,** Cooper D. and A.D. Heifrick, PHI, 2009 Edition.

References

1. **Electronic Instrumentation and Measurement,** David A. Bell, oxford Publication ,2nd Edition, 2009.
2. **Electrical Measurements and Measuring Instruments,** Golding and Widdies, Pitman

10EE36 ELECTRIC POWER GENERATION

Subject Code	:	10EE36	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART – A

UNIT 1:

Sources of Electrical Power: Wind, solar, fuel cell, tidal, geo-thermal, hydro-electric, thermal-steam, diesel, gas, nuclear power plants (block diagram approach only). Concept of co-generation. Combined heat and power distributed generation. 06 **Hours**

UNIT 2:

Diesel electric plants. Gas turbine plants. Mini, micro, and bio generation. Concept of distributed generation. 06 **Hours**

UNIT 3:

(a) Hydro Power Generation: Selection of site. Classification of hydro-electric plants. General arrangement and operation. Hydroelectric plant power station structure and control. 5 **Hours**

(b) Thermal Power Generation: Introduction. Main parts of a thermal power plant. Working. Plant layout. **3 Hours**

UNIT 4:

Nuclear Power Station: Introduction. Pros and cons of nuclear power generation. Selection of site, cost, components of reactors. Description of fuel sources. Safety of nuclear power reactor. **6 Hours**

PART – B

UNIT 5 and 6:

(a) Economics Aspects: Introduction. Terms commonly used in system operation. Diversity factor, load factor, plant capacity factor, plant use factor, plant utilization factor and loss factor, load duration curve. Cost of generating station, factors influencing the rate of tariff designing, tariff, types of tariff**.** Power factor improvement.

(b) Substations: Introduction, types, Bus bar arrangement schemes, Location of substation equipment. Reactors and capacitors. Interconnection of power stations. 1**4 Hours**

UNIT 7 and 8 :

Grounding Systems: Introduction, grounding systems. Neutral grounding. Ungrounded system. Resonant grounding. Solid grounding, reactance grounding, resistance grounding. Earthing transformer. Neutral grounding transformer. **12 Hours**

Text Books

1. **Power System Engineering,** A. Chakrabarti, M. L. Soni, and P.V. Gupta, Dhanpat Rai and Co.,NewDelhi.

2. **Electric Power Generation, Transmission and Distribution,** S. N. Singh, PHI, 2nd Edition,2009.

References

1. **Elements of Electrical Power System Design,** M. V. Deshpande, PHI,2010

ANALOG ELECTRONICS LAB

(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ESL37**	***IA Marks***	**:**	**25**
Hrs/ Week	**:**	**03**	Exam Hours	**:**	**03**
Total Hrs.	**:**		**Exam Marks**	**:**	**50**

NOTE: Use the Discrete components to test the circuits. LabView can be used for the verification and testing along with the above.

1. Wiring of RC coupled Single stage FET & BJT amplifier and determination of the gain-frequency response, input and output impedances.

2. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances (Single circuit) (One Experiment)

3. Wiring of a two stage BJT Voltage series feed back amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback (One Experiment)

4. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for $f_0 \leq 10$ KHz

5. Testing for the performance of BJT – Hartley & Colpitts Oscillators for RF range $f_0 \geq 100$KHz.

6. Testing for the performance of BJT -Crystal Oscillator for $f_0 > 100$ KHz

7 Testing of Diode clipping (Single/Double ended) circuits for peak clipping, peak detection

8. Testing of Clamping circuits: positive clamping /negative clamping.
9. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.

10. Testing of Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency

11. Verification of Thevinin's Theorem and Maximum Power Transfer theorem for DC Circuits.

12. Characteristics of Series and Parallel resonant circuits.

LOGIC DESIGN LAB

(Common to EC/TC/EE/IT/BM/ML)

Sub Code	**:**	**10ESL38**	***IA Marks***	**:**	**25**
Hrs/ Week	**:**	**03**	Exam Hours	**:**	**03**
Total Hrs.	**:**		**Exam Marks**	**:**	**50**

NOTE: Use discrete components to test and verify the logic gates. LabView can be used for designing the gates along with the above.

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
   (ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).
10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.