**EMBEDDED SYSTEMS DESIGN (S2-17-SSCSGZG512) ASSIGNMENT  
PROCESSOR SIMULATOR DATASHEET**

**-Done by:**

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**How to run the Simulator with Web UI:**

Step 1: Run the python file named esd\_assignment\_karthikeyan\_2017cg12539.py

Step 2: Open any browser and type the url http://<ip>:<port>/

IP is the output of ipconfig command in CMD and port is 5000.

eg: <http://192.168.1.8:5000/>

Step 3: Web UI appears in which the input file can be selected and executed

**Salient Features:**

* Ability to select input file containing the assembly code and execute instructions one by one and display the contents of Accumulator, other registers, flags, PC, IR, Stack, Memory etc.
* Supports interrupt handling through ISR.

**Specifications:**

Available Registers: A, B, R0, R1, R2, R3

Size of each register: 8 bits (1 byte)

Memory Size: 256 bytes

No. of interrupts: 1

Size of Stack: 8 bytes

Supported Addressing Modes: Immediate, Register, Direct & Indirect addressing modes

Opcode size: 1 byte for Register and Indirect addressing modes and 2 bytes for Immediate and Direct addressing modes

**APPENDIX A:**

**Supported Instructions and corresponding Opcodes:**

('NOP', '0x00')

('INC A', '0x01')

('INC @R0', '0x02')

('INC @R1', '0x03')

('INC R0', '0x04')

('INC R1', '0x05')

('INC R2', '0x06')

('INC R3', '0x07')

('CLR A', '0x08')

('SETB C', '0x10')

('DEC A', '0x11')

('DEC @R0', '0x12')

('DEC @R1', '0x13')

('DEC R0', '0x14')

('DEC R1', '0x15')

('DEC R2', '0x16')

('DEC R3', '0x17')

('CLR C', '0x18')

('ADD A,#data', '0x20')

('ADD A,directAddress', '0x21')

('ADD A,@R0', '0x22')

('ADD A,@R1', '0x23')

('ADD A,R0', '0x24')

('ADD A,R1', '0x25')

('ADD A,R2', '0x26')

('ADD A,R3', '0x27')

('CPL A', '0x28')

('ADDC A,#data', '0x30')

('ADDC A,directAddress', '0x31')

('ADDC A,@R0', '0x32')

('ADDC A,@R1', '0x33')

('ADDC A,R0', '0x34')

('ADDC A,R1', '0x35')

('ADDC A,R2', '0x36')

('ADDC A,R3', '0x37')

('CPL C', '0x38')

('SUBB A,#data', '0x40')

('SUBB A,directAddress', '0x41')

('SUBB A,@R0', '0x42')

('SUBB A,@R1', '0x43')

('SUBB A,R0', '0x44')

('SUBB A,R1', '0x45')

('SUBB A,R2', '0x46')

('SUBB A,R3', '0x47')

('RL A', '0x48')

('ORL A,#data', '0x50')

('ORL A,directAddress', '0x51')

('ORL A,@R0', '0x52')

('ORL A,@R1', '0x53')

('ORL A,R0', '0x54')

('ORL A,R1', '0x55')

('ORL A,R2', '0x56')

('ORL A,R3', '0x57')

('RR A', '0x58')

('ANL A,#data', '0x60')

('ANL A,directAddress', '0x61')

('ANL A,@R0', '0x62')

('ANL A,@R1', '0x63')

('ANL A,R0', '0x64')

('ANL A,R1', '0x65')

('ANL A,R2', '0x66')

('ANL A,R3', '0x67')

('RLC A', '0x68')

('XRL A,#data', '0x70')

('XRL A,directAddress', '0x71')

('XRL A,@R0', '0x72')

('XRL A,@R1', '0x73')

('XRL A,R0', '0x74')

('XRL A,R1', '0x75')

('XRL A,R2', '0x76')

('XRL A,R3', '0x77')

('RRC A', '0x78')

('MOV A,#data', '0x80')

('MOV A,directAddress', '0x81')

('MOV A,@R0', '0x82')

('MOV A,@R1', '0x83')

('MOV A,R0', '0x84')

('MOV A,R1', '0x85')

('MOV A,R2', '0x86')

('MOV A,R3', '0x87')

('MUL AB', '0x88')

('MOV R0,#data', '0x90')

('MOV R0,directAddress', '0x91')

('MOV R0,@R0', '0x92')

('MOV R0,@R1', '0x93')

('MOV R0,R0', '0x94')

('MOV R0,R1', '0x95')

('MOV R0,R2', '0x96')

('MOV R0,R3', '0x97')

('DIV AB', '0x98')

('MOV R1,#data', '0xa0')

('MOV R1,directAddress', '0xa1')

('MOV R1,@R0', '0xa2')

('MOV R1,@R1', '0xa3')

('MOV R1,R0', '0xa4')

('MOV R1,R1', '0xa5')

('MOV R1,R2', '0xa6')

('MOV R1,R3', '0xa7')

('MOV R2,#data', '0xb0')

('MOV R2,directAddress', '0xb1')

('MOV R2,@R0', '0xb2')

('MOV R2,@R1', '0xb3')

('MOV R2,R0', '0xb4')

('MOV R2,R1', '0xb5')

('MOV R2,R2', '0xb6')

('MOV R2,R3', '0xb7')

('MOV R3,#data', '0xc0')

('MOV R3,directAddress', '0xc1')

('MOV R3,@R0', '0xc2')

('MOV R3,@R1', '0xc3')

('MOV R3,R0', '0xc4')

('MOV R3,R1', '0xc5')

('MOV R3,R2', '0xc6')

('MOV R3,R3', '0xc7')

('MOV A,B', '0xd0')

('MOV B,A', '0xd1')

('MOV @R0,A', '0xd2')

('MOV @R1,A', '0xd3')

('MOV R0,A', '0xd4')

('MOV R1,A', '0xd5')

('MOV R2,A', '0xd6')

('MOV R3,A', '0xd7')