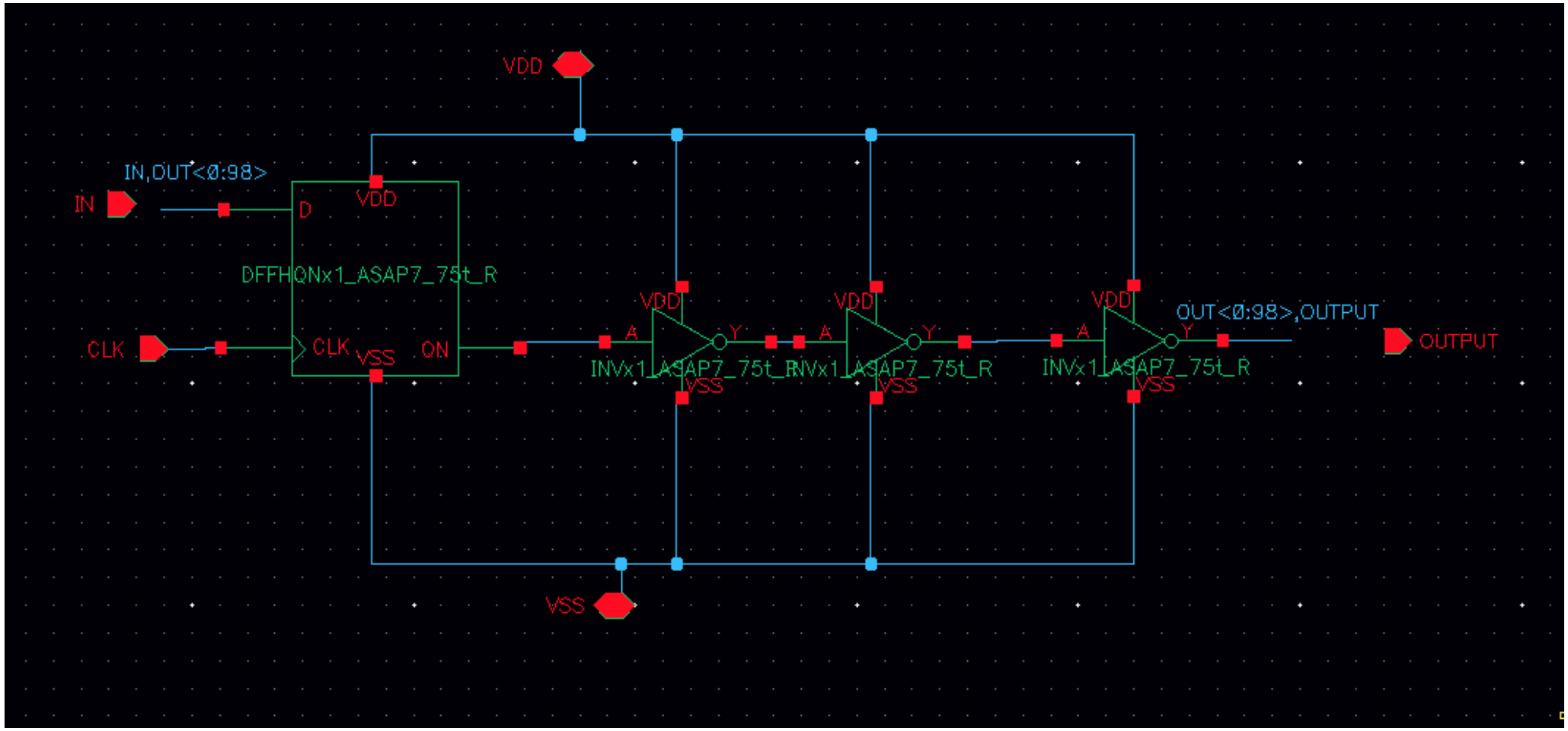
EE5323 HOMEWORK #2: SCAN CHAIN DESIGN

KARTHESHWAR SHANMUGA SUNDARAM

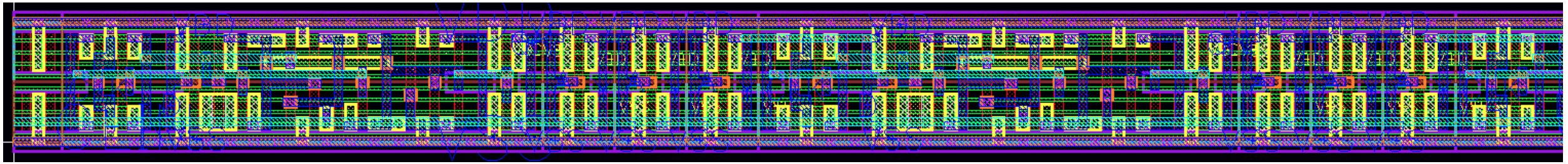
5569005

1.SCHEMATIC FOR SCAN CHAIN IN VIRTUOSO



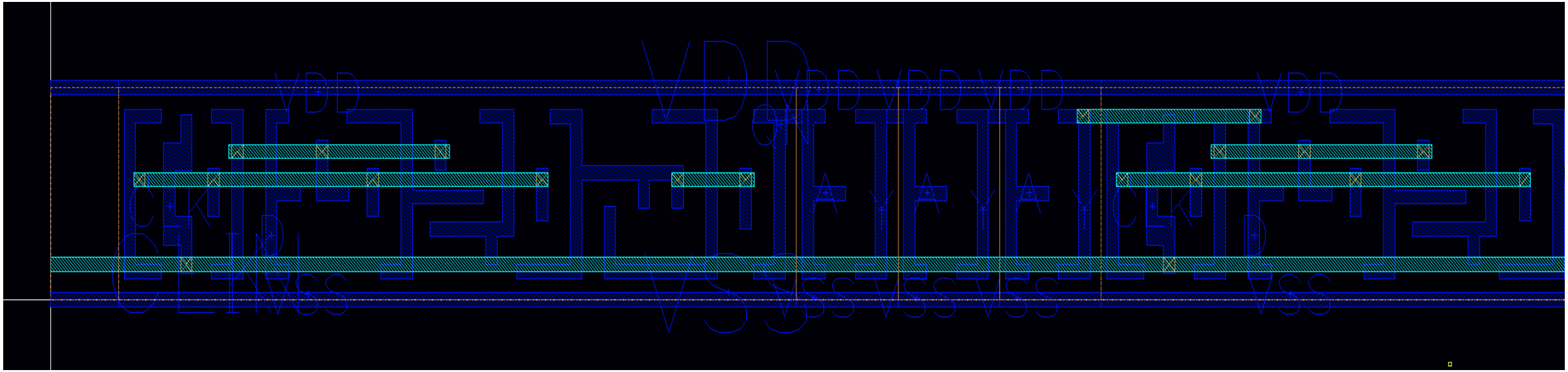
As seen in the schematic a D flip flop and three inverters (1x Inverter) are used. The output at each stage is Q. Bus notation is used to create an array of 100 stage scan-chain

LAYOUT SECTION FOR 100 STAGE SCAN CHAIN

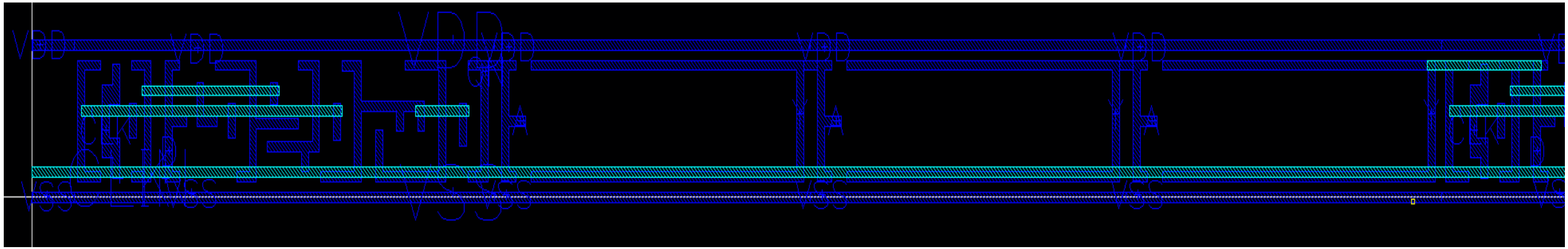


- The layout consists on D Flip-Flip and 3 inverter.
- The connection between these elemets is done using metal M1
- The clock of each D Flip-Flopis is connected by Metal M2 and VIA
- Tap cell is placed every after every 9 cycle, considering worst case scenario of max drive strength of 13x Inverter
- Labels CLK, VDD, VSS, IN, and output are placed

LAYOUT-- SHOWING METAL LAYERS TO INDICATE CONNECTIONS (1 X INVERTER)



LAYOUT-- SHOWING METAL LAYER TO INDICATE CONNECTIONS (13 X INVERTER)



DRC PASS SNAPSHOT FOR (1 X INVERTER)

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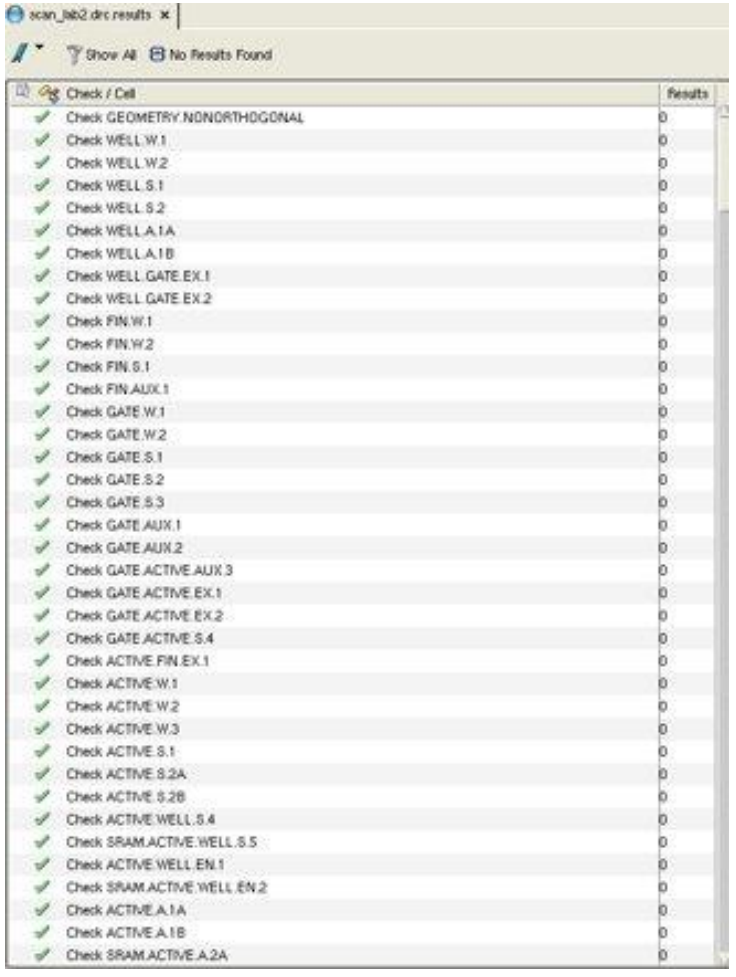
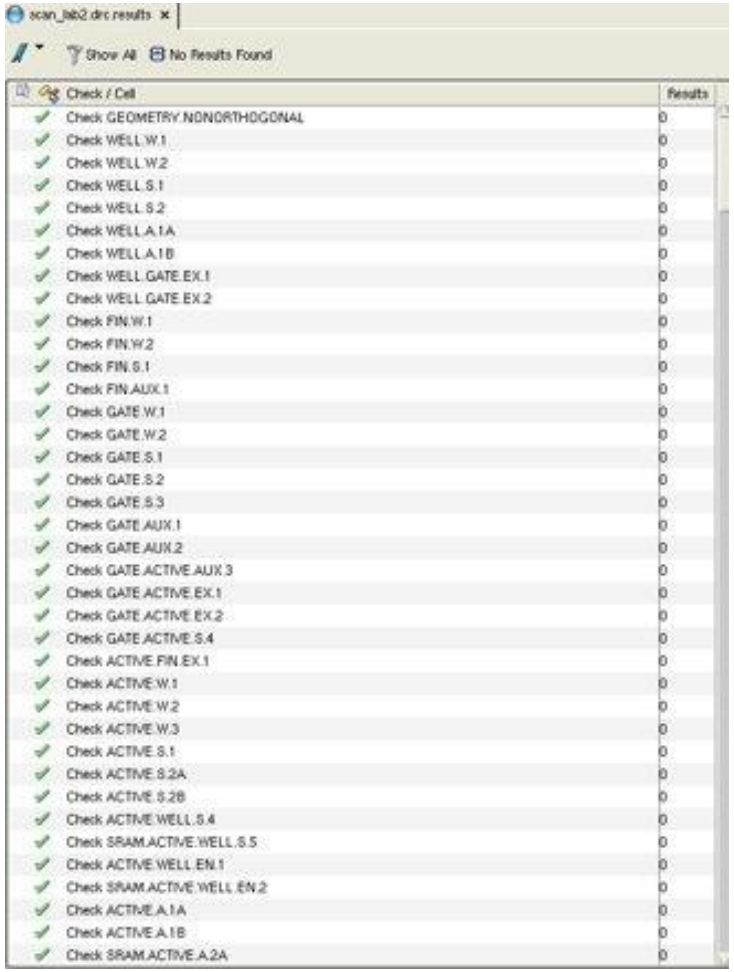
================================================================================
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:        Wed Oct  2 22:54:27 2019
Calibre Version:            v2015.2_19.13    Wed May 13 18:26:03 PDT 2015
Rule File Pathname:         /home/class/shanm107/asap7_rundir/_drcRules_calibre_asap7.rul_
Rule File Title:
Layout System:              GDS
Layout Path(s):             scan_lab2.calibre.db
Layout Primary Cell:        scan_lab2
Current Directory:          /home/class/shanm107/asap7_rundir
User Name:                  shanm107
Maximum Results/RuleCheck:  1000
Maximum Result Vertices:    4096
DRC Results Database:       scan_lab2.drc.results (ASCII)
Layout Depth:               ALL
Text Depth:                 PRIMARY
Summary Report File:        scan_lab2.drc.summary (REPLACE)
Geometry Flagging:          ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID = NO
                            NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:          COMMENT TEXT + RULE FILE INFORMATION
Layers:                     MEMORY-BASED
Keep Empty Checks:          YES
--------------------------------------------------------------------------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
```

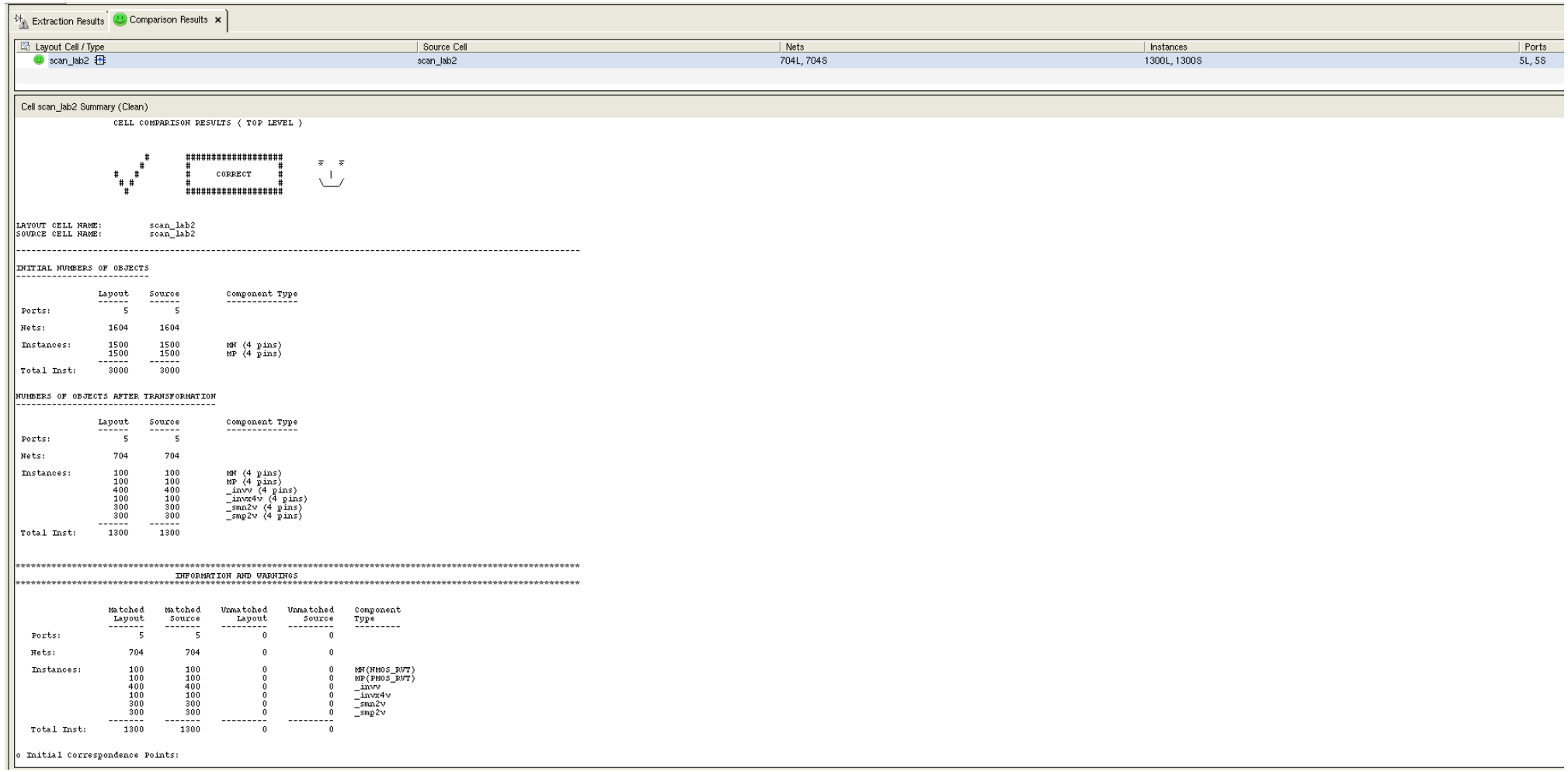
```
RULECHECK M9.S.7 ..................... TOTAL Result Count = 0 (0)
RULECHECK M9.S.8 ..................... TOTAL Result Count = 0 (0)
RULECHECK M9.A.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK M9.L.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK V8.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK V8.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK V8.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK V8.M8.EN.1 ................. TOTAL Result Count = 0 (0)
RULECHECK V8.M9.EN.2 ................. TOTAL Result Count = 0 (0)
RULECHECK V8.AUX.1 ................... TOTAL Result Count = 0 (0)
RULECHECK V9.W.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK V9.S.1 ..................... TOTAL Result Count = 0 (0)
RULECHECK V9.S.2 ..................... TOTAL Result Count = 0 (0)
RULECHECK V9.M9.EN.1 ................. TOTAL Result Count = 0 (0)
RULECHECK V9.PAD.EN.2 ................ TOTAL Result Count = 0 (0)
RULECHECK V9.AUX.1 ................... TOTAL Result Count = 0 (0)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  2
TOTAL REAL Time:                 3
TOTAL Original Layer Geometries: 989 (35748)
TOTAL DRC RuleChecks Executed:   334
TOTAL DRC Results Generated:     0 (0)
```



DRC PASS SNAPSHOT FOR (13 X INVERTER)



LVS PASSING SNAPSHOT



Extraction Results | Comparison Results ×

Layout Cell / Type	Source Cell	Nets	Instances	Ports
scan_lab2	scan_lab2	704L, 704S	1300L, 1300S	5L, 5S

Cell scan_lab2 Summary (Clean)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )


                       #      ###################
                     #        #                 #       ^  ^
                   #   #      #     CORRECT     #      (  |
                    # #       #                 #       \__/
                     #        ###################


LAYOUT CELL NAME:         scan_lab2
SOURCE CELL NAME:         scan_lab2

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INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:               5         5

 Nets:             1604      1604

 Instances:        1500      1500         MN (4 pins)
                   1500      1500         MP (4 pins)
                 ------    ------
 Total Inst:       3000      3000

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source         Component Type
                 ------    ------         --------------
 Ports:               5         5

 Nets:              704       704

 Instances:         100       100         MN (4 pins)
                    100       100         MP (4 pins)
                    400       400         _invv (4 pins)
                    100       100         _invx4v (4 pins)
                    300       300         _sman2v (4 pins)
                    300       300         _smp2v (4 pins)
                 ------    ------
 Total Inst:       1300      1300


************************************************************************************************************
                                  INFORMATION AND WARNINGS
************************************************************************************************************

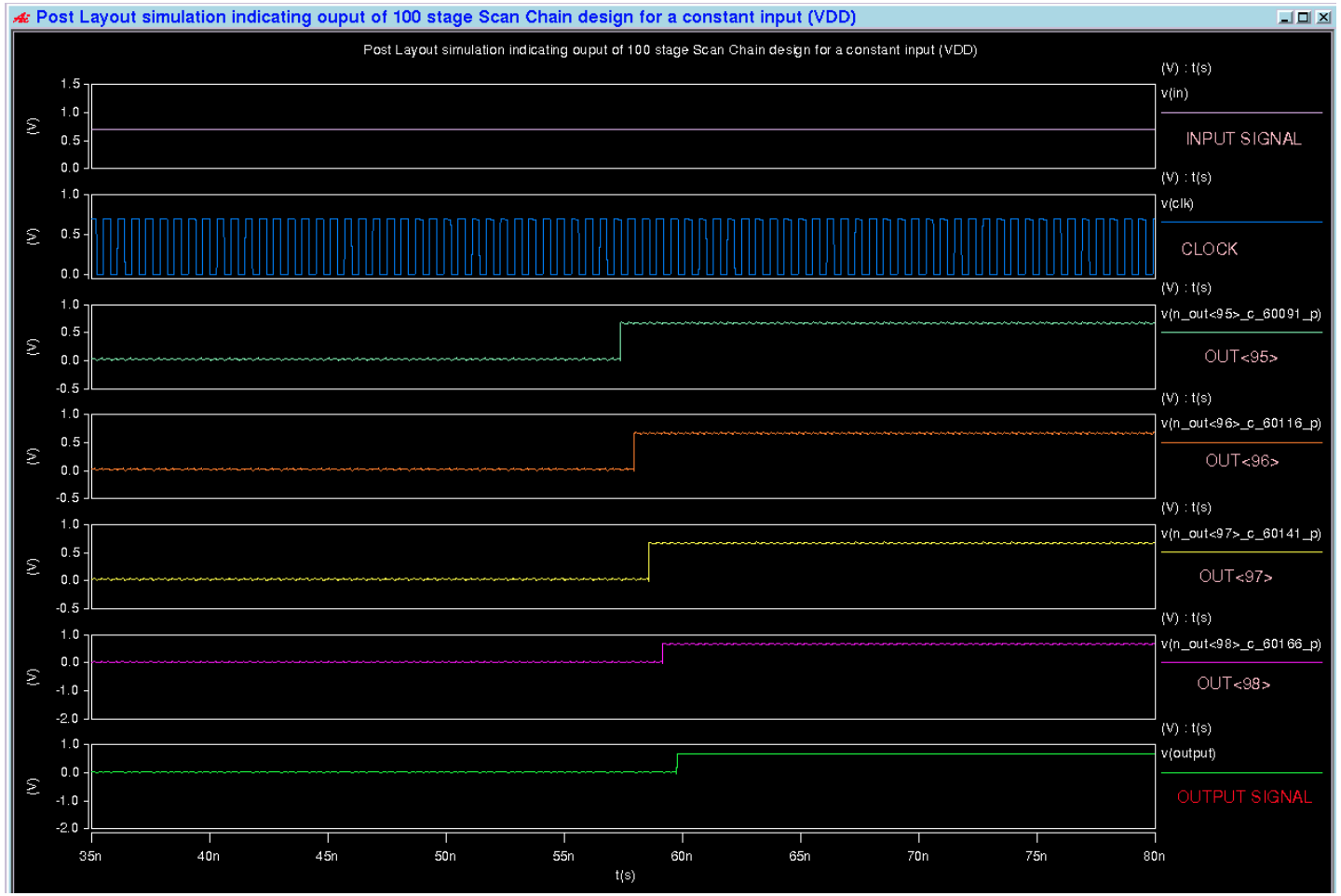

                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    ---------
   Ports:               5          5            0            0

   Nets:              704        704            0            0

   Instances:         100        100            0            0    MN(NMOS_RVT)
                      100        100            0            0    MP(PMOS_RVT)
                      400        400            0            0    _invv
                      100        100            0            0    _invx4v
                      300        300            0            0    _sman2v
                      300        300            0            0    _smp2v
                  -------    -------    ---------    ---------
   Total Inst:       1300       1300            0            0

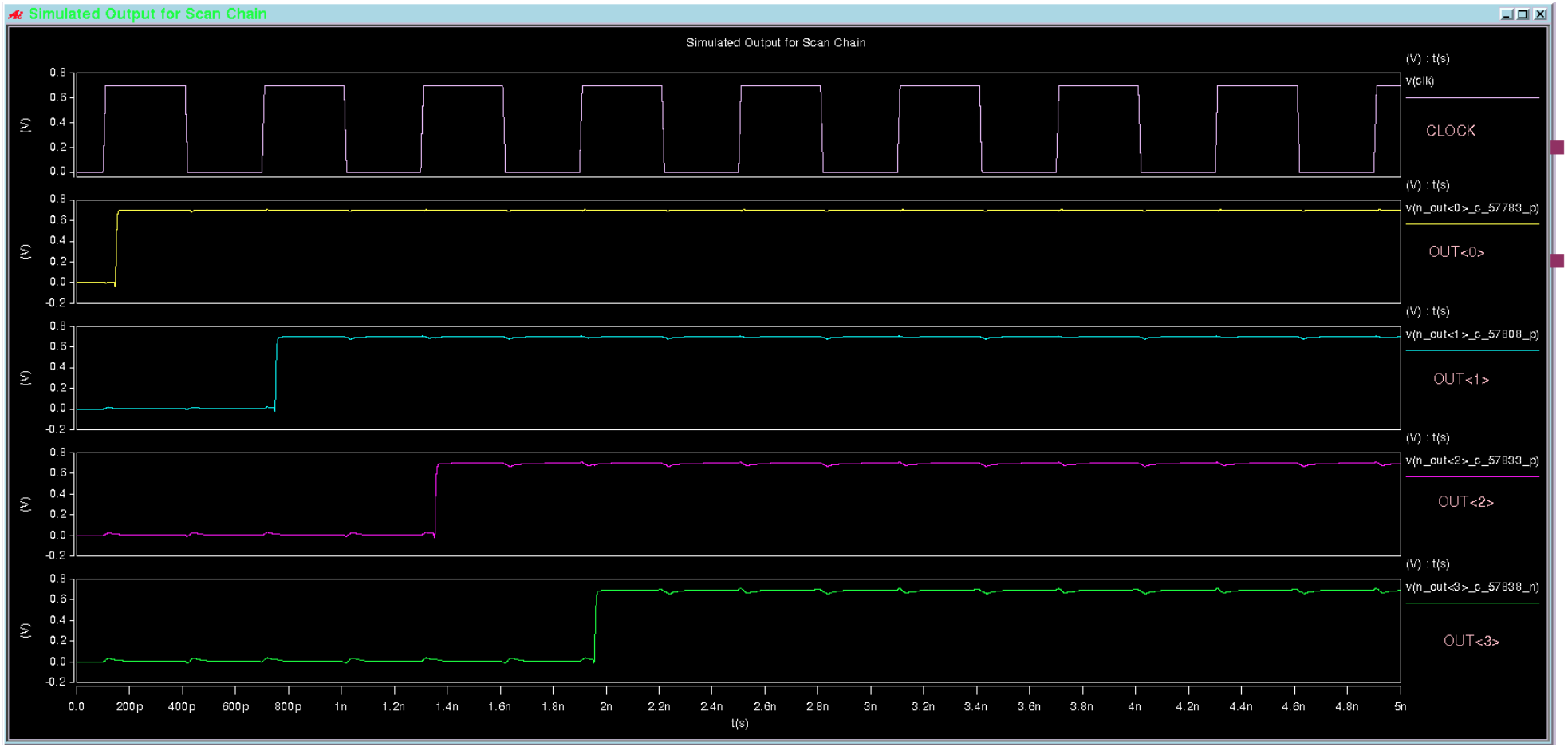
o Initial Correspondence Points:
```

POST LAYOUT SIMULATION (WITH 1 X INVERTER)



- INPUT is given as VDD (constant)
- The figure shows the output signal, OUT<98>, OUT<97>,OUT<96>, OUT<95>, Clock, Input in PVT condition mentioned at slide 14

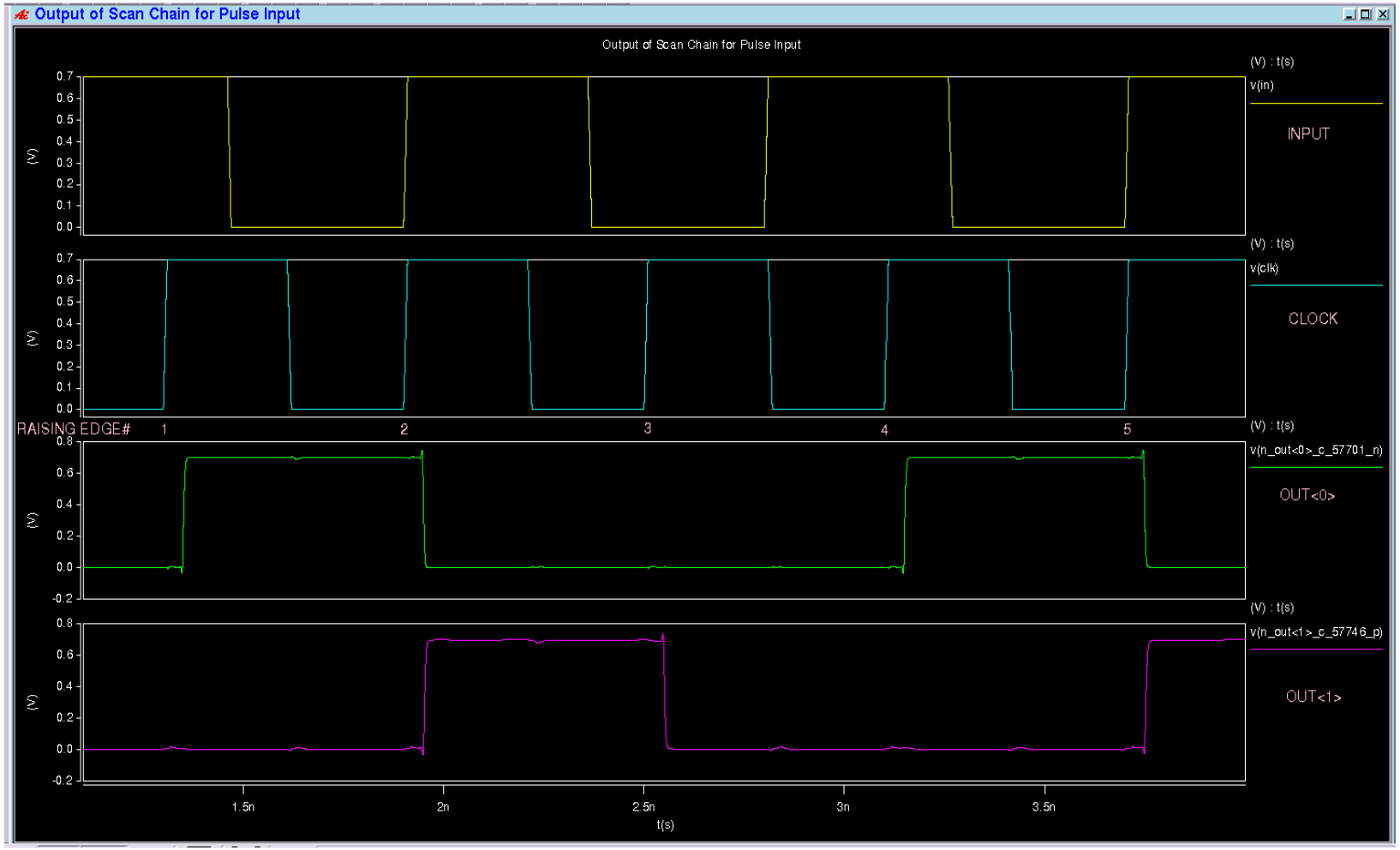
POST LAYOUT SIMULATION (WITH 1 X INVERTER)



- INPUT is given as VDD (constant)
- The figure shows the OUT<0>, OUT<1>,OUT<2>, OUT<3>, CLK in PVT condition mentioned at slide 14

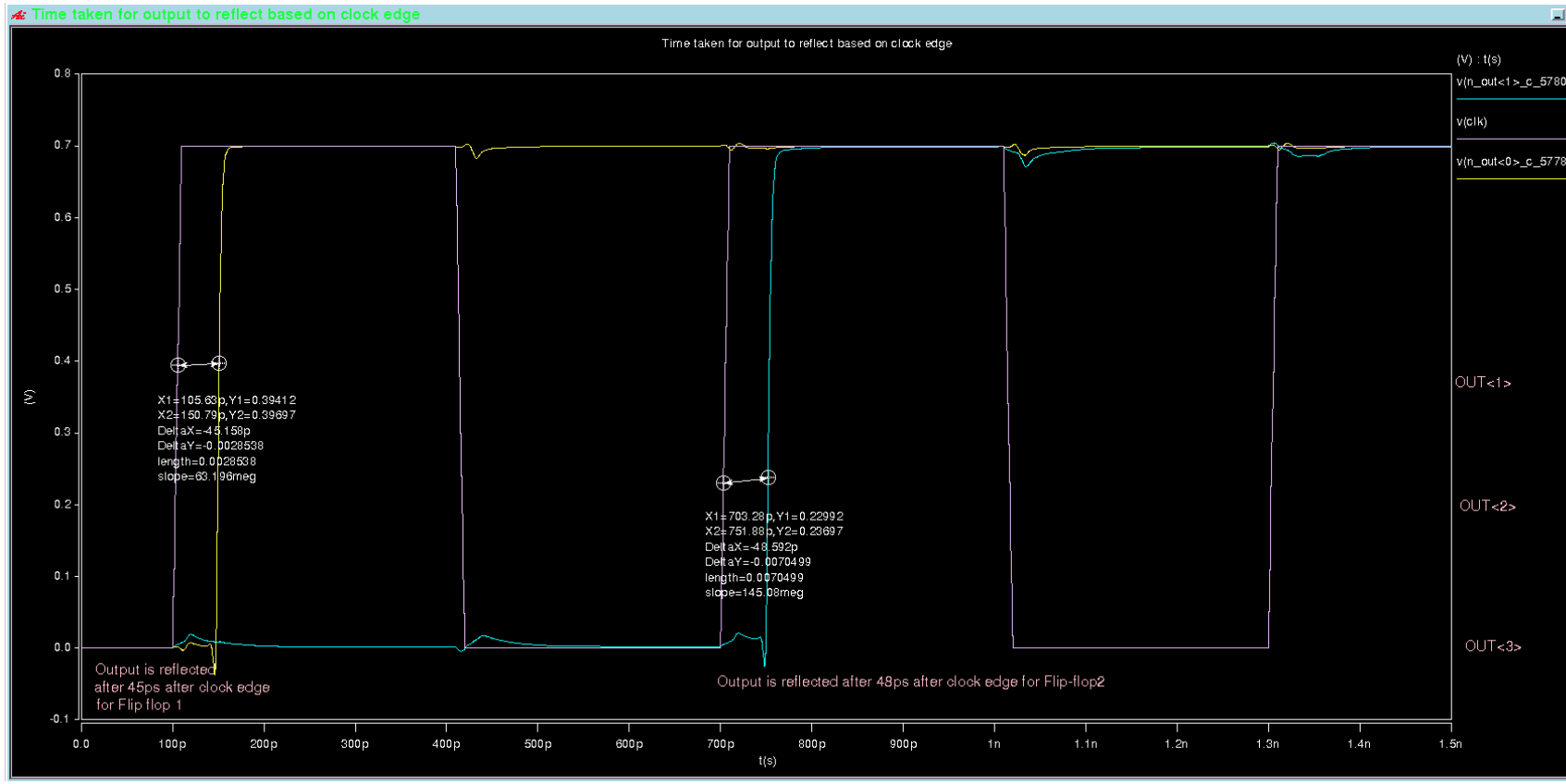
POST LAYOUT SIMULATION (WITH 1 X INVERTER)

- At raising edge #1 indicated in the graph input=1, output of DFF1=0, so output of DFF1=1, DFF2=0
- At raising edge #2 indicated in the graph input=0, output of DFF=1, so output of DFF1=0, DFF2=1
- At raising edge #3 indicated in the graph input=0, output of DFF1=0, so output of DFF1=0, DFF2=0
- At raising edge #4 indicated in the graph input=1, output of DFF1=0, so output of DFF1=1, DFF2=0
- At raising edge #5 indicated in the graph input=0, output of DFF1=1, so output of DFF1=0, DFF2=1



POST LAYOUT PROPAGATION DELAY FOR EACH D-FLIPFLOP (WITH 1 X INVERTER)

- The input at the first D-Flip Flop is taken at the first raising edge.
- It takes approximately 45ps for the output to reflect after the raising edge is detected for first Flip flop.
- The output is reflected 48ps after the raising edge is detected for second Flip flop.



POST LAYOUT SIMULATION PVT

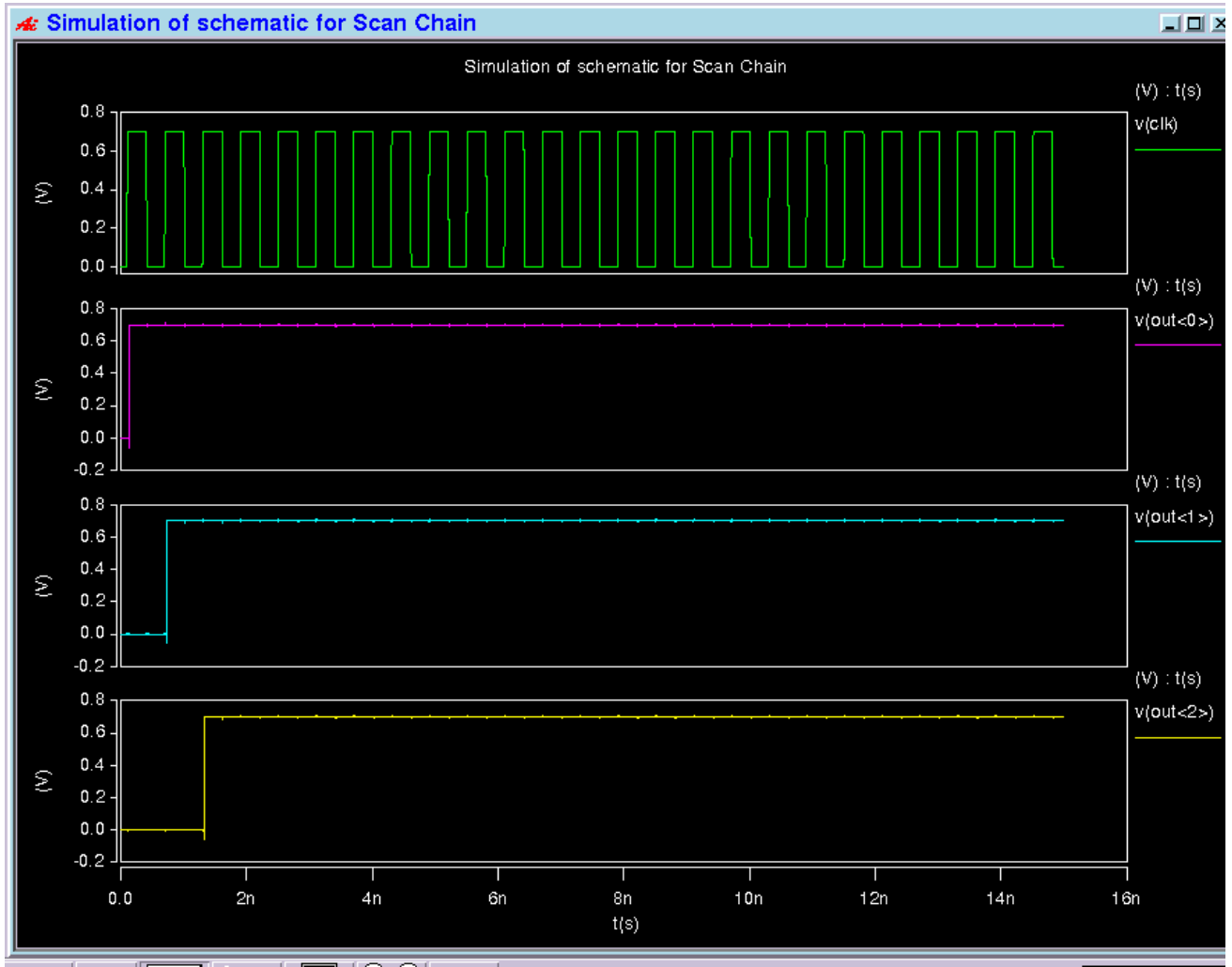
Simulation is run at 110 degree

VDD=0.7V

The input is given in slide 9, 10 is VDD, slide 11 is a pulse .

Clock is given a pulse of 0->0.7V with a total period of 600ps and on time of 300 ps

SIMULATION OF SCHEMATIC FOR 100 STAGE SCAN CHAIN



FILES ATTACHED

- SKILL Code : Kartheshwar_create_arr.il
- Post layout simulation Files: scan_lab2.pex.netlist.SCAN_LAB2.pxi, scan_lab2.pex.netlist.pex, scan_lab2.pex.netlist
- Run file for layout: runinv.sp
- Run file for schematic: runinv_sch.sp