EE5323 HOMEWORK #3: CHARACTERIZING FINFET ASAP 7NM

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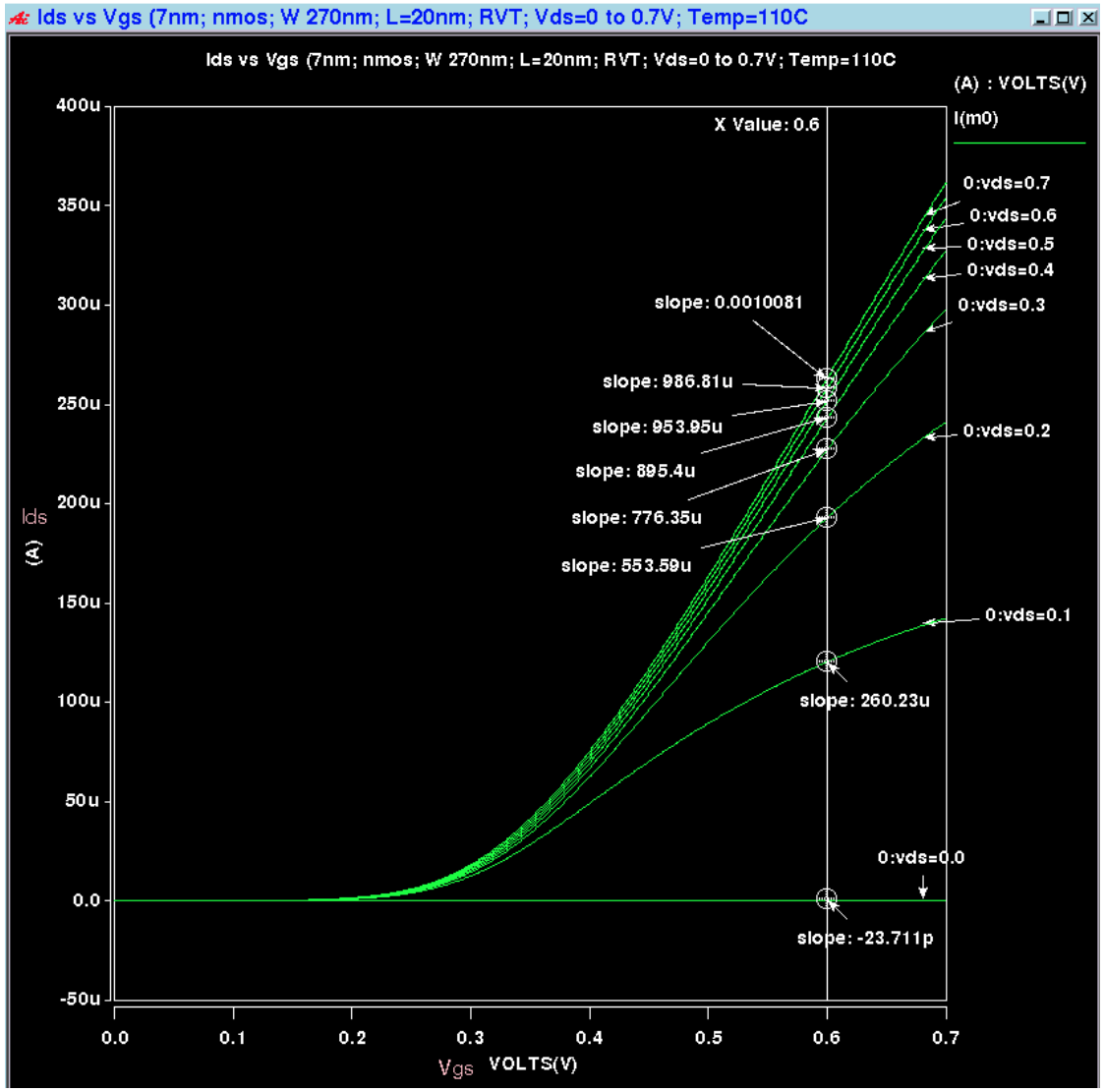
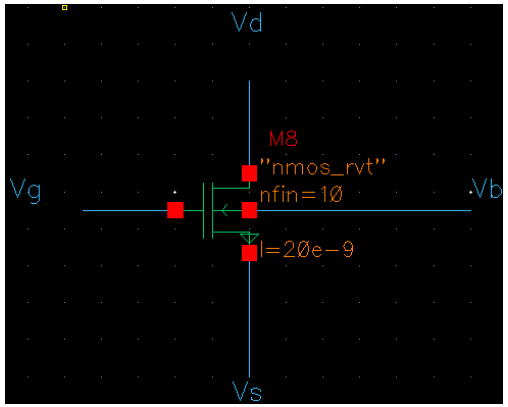
IDS VERSUS VGS (FOR DIFFERENT VDS) -NMOS

- For short channel devices Ids is proportional to (Vgs –Vt – Vdsat/2)
- The current belowVgs= Vt in linear scale is negligible and after Vt there is a linear relation to Vgs

- As theVds increases the current increases as shown in graph

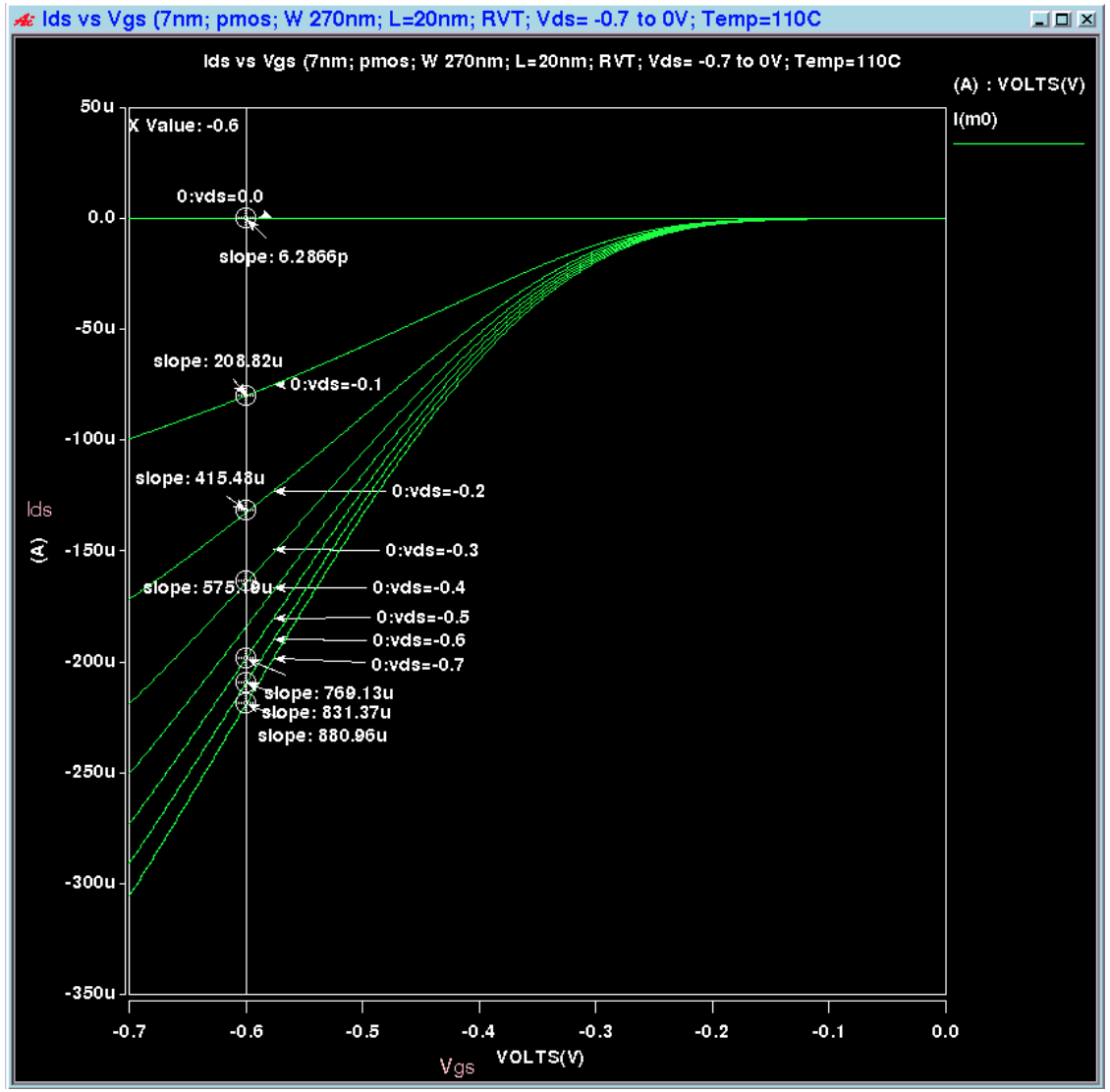


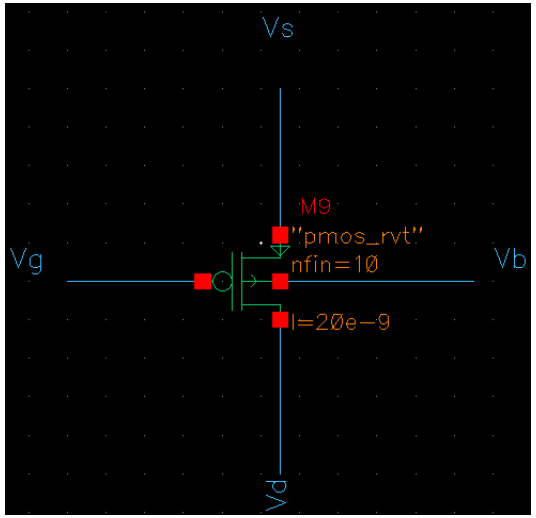


Vs=0, Vb=0,
Vd =0-0.7 in steps of 0.1,
Vg=0-0.7 in steps of 0.001

IDS VERSUS VGS (FOR DIFFERENT VDS) - PMOS

- For short channel devices Ids is proportional to (Vgs –Vt – Vdsat/2)
- The current below Vt in linear scale is negligible and after Vt
- As the Vds increases the current increases as shown in graph
- As compared to nmos the pmos current is little lower, say for Vds=0.7V the pmos current is 300uA but nmos current is 350uA, this is due to higher mobility of nmos.

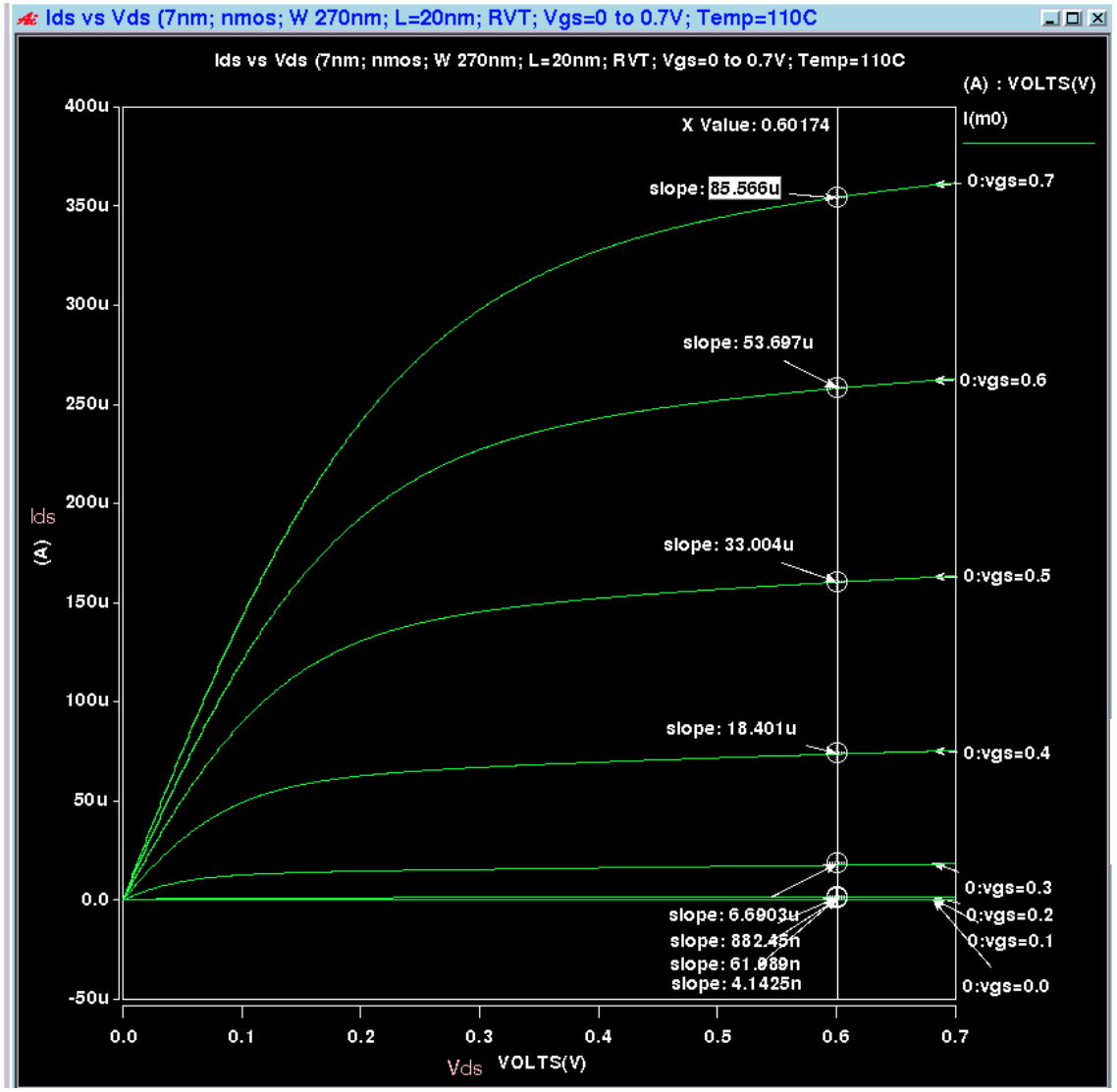


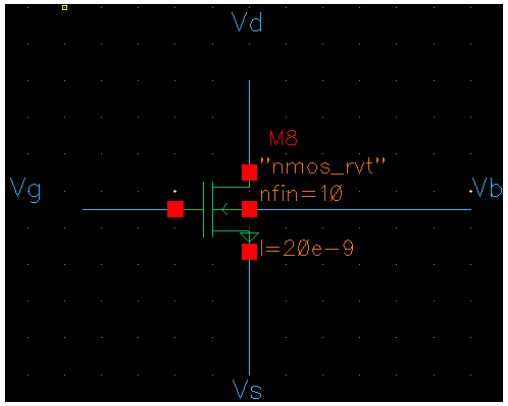


Vs=0 , Vb=0
Vd = 0 to -0.7 in steps of -0.1
Vg= 0 to -0.7 in steps of -0.001

IDS VERSUS VDS (FOR DIFFERENT VGS)- NMOS

- For a given Vgs as Vds increases the current increases
- For short channel devices Ids is proportional to (Vgs –Vt – Vdsat/2)



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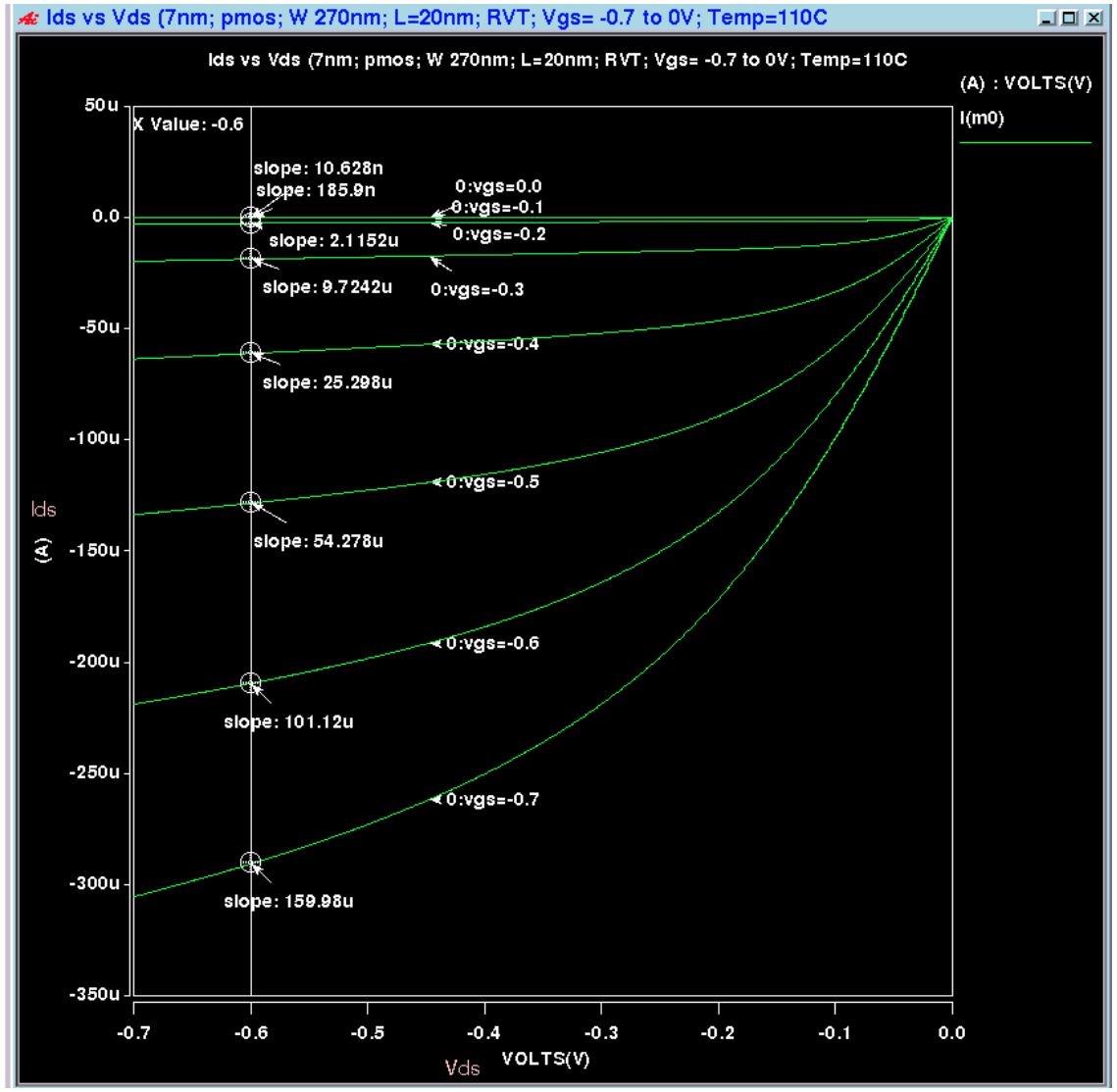
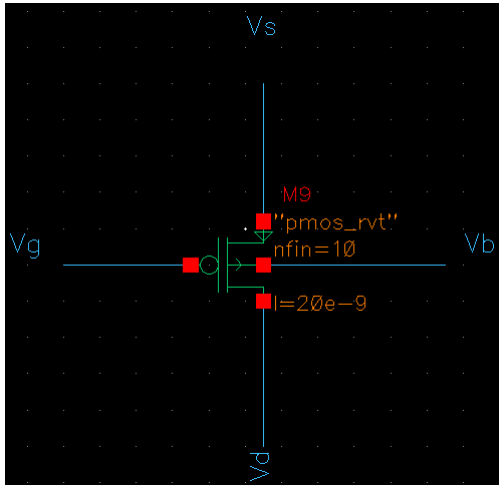
Vs=0, Vb=0,
Vd = 0 to 0.7 in steps of 0.001,
Vg= 0 to 0.7 in steps of 0.1
```

IDS VERSUS VDS (FOR DIFFERENT VGS)- PMOS

- For a given Vgs as Vds increases the current increases
- For short channel devices Ids is proportional to (Vgs –Vt – Vdsat/2)
- As compared to nmos the pmos current is little lower, say for Vds=0.7V the pmos current is 300uA but nmos current is 350uA, this is due to higher mobility of nmos.

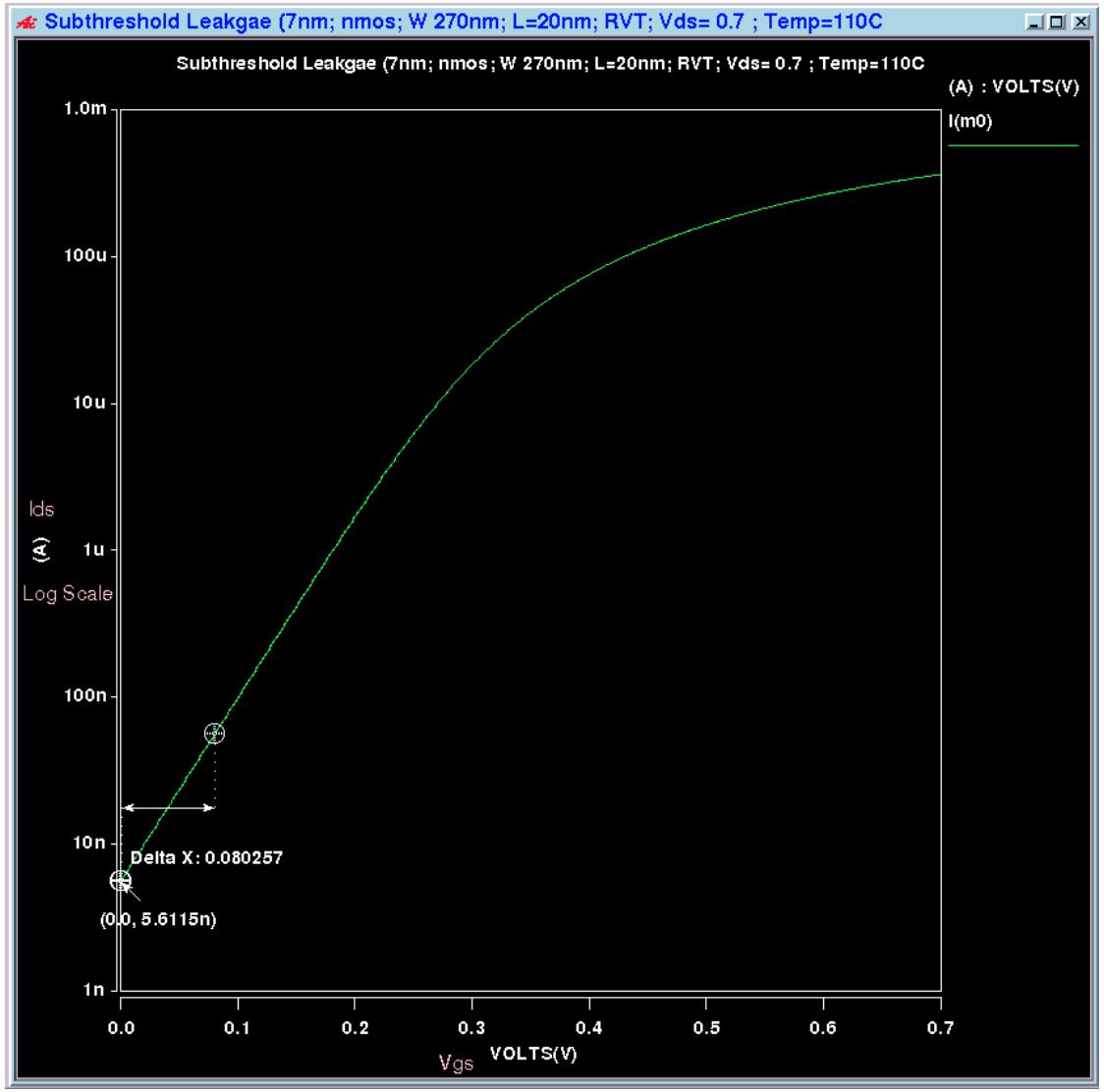


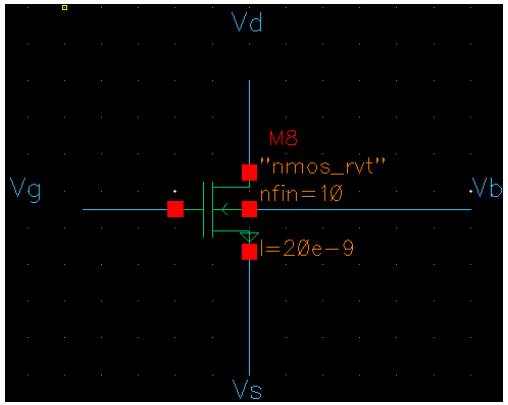


Vs=0, Vb=0,
Vd = -0.7 to 0 in steps of 0.001,
Vg= -0.7 to 0 in steps of 0.1

SUB-THRESHOLD SWING [V/DEC]- NMOS

- Subthreshold current is the current when transistor is off and MOS behaves as BJT
- Ids = exp(Vgs-vt/(mkT/q))
- As shown in graph current is plotted in log scale and below Vt there is a linear relation.
- m=1 for Finfet and operating temperature is 110deg.
- The Sub threshold swing is given as (ln10 *m*k*T/q) which is current for a 10x change in voltage = 80 mV

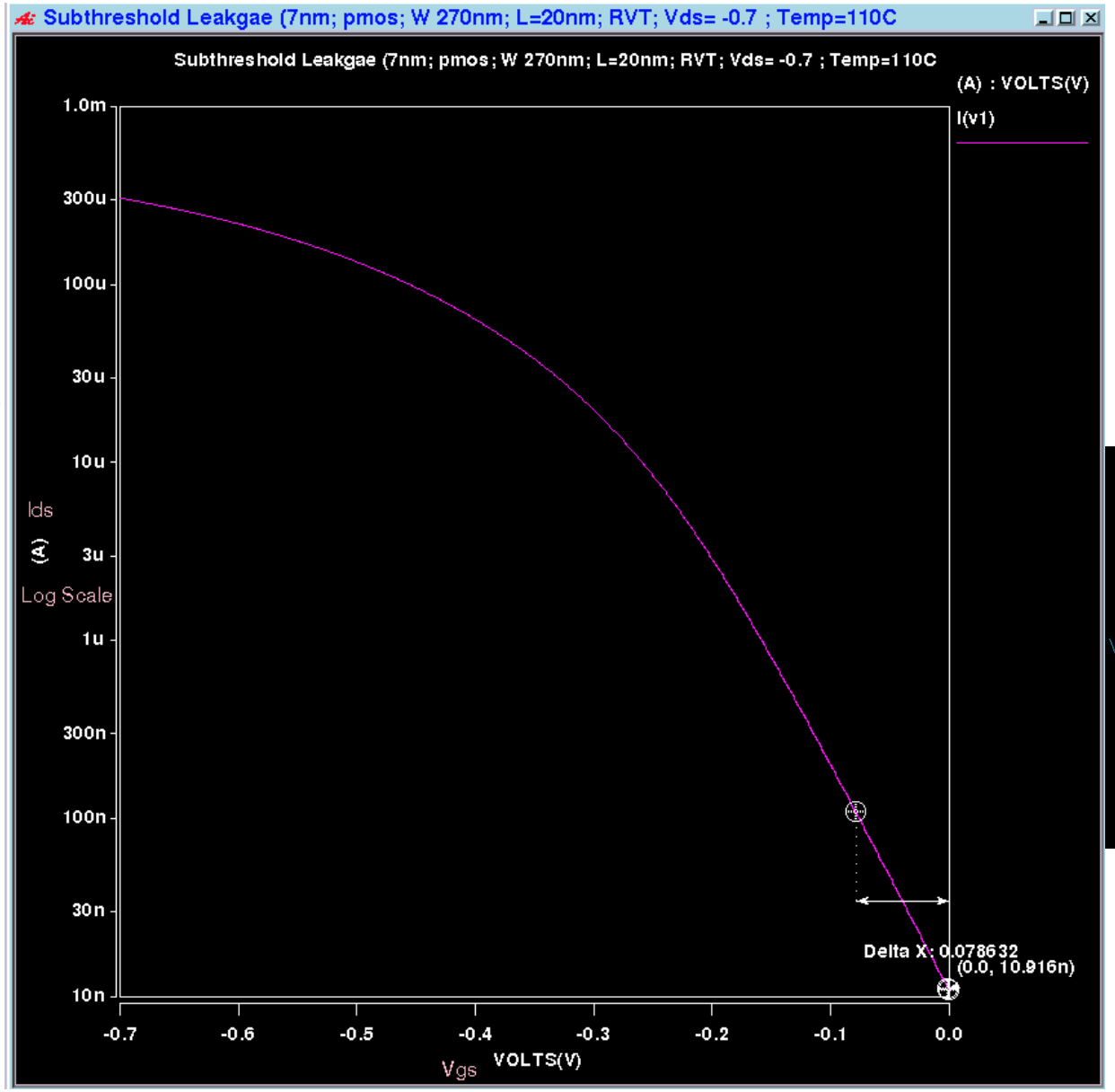


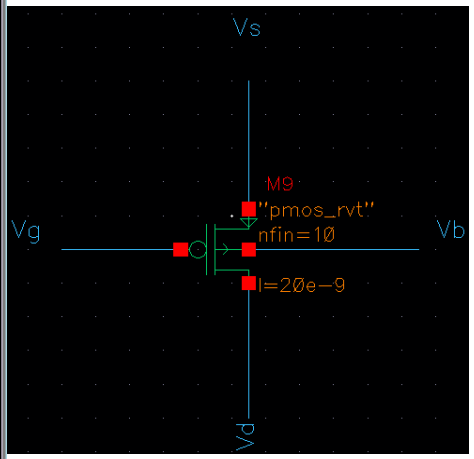


Vs=0, Vb=0,
Vd = 0.7
Vg= 0 to 0.7 in steps of 0.001

SUB-THRESHOLD SWING [V/DEC] - PMOS

- Subthreshold current is the current when transistor is off and MOS behaves as BJT
- Ids = exp(Vgs-vt/(mkT/q))
- As shown in graph current is plotted in log scale and below Vt there is a linear relation.
- m=1 for Finfet and operating temerature is 110deg.
- The Sub threshold swing is given as (ln10 *m*k*T/q) which is current for a 10x change in voltage = 78 mV
- The subtreshold swing for nmos and pmos are almost same.

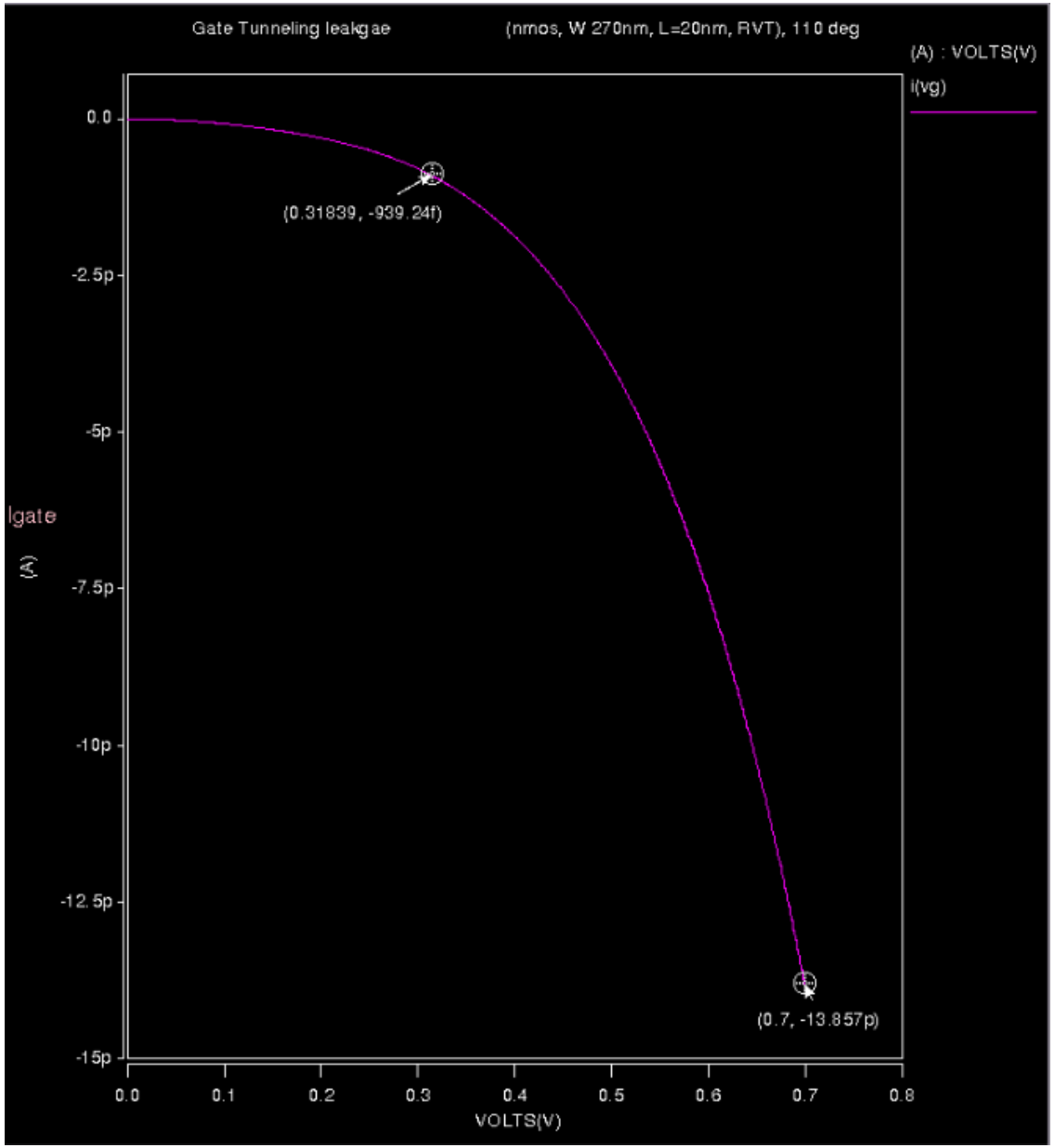


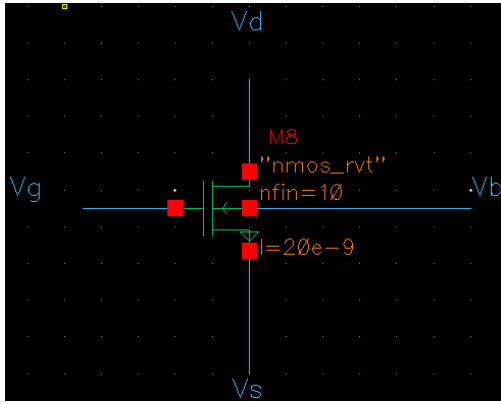


Vs=0, Vb=0,
Vd = -0.7
Vg= -0.7 to 0 in steps of 0.001

GATE TUNNELING LEAKAGE VERSUS VDD -NMOS

- Gate tunneling is maximum for ON device
- It is 3-10 times higher than pmos gate leakgae
- It is strong function of (Vox/tox).
- So as Vg increases then there is exponential increase as seen in the graph






```
Vs=0, Vb=0,
Vd = 0
Vg= 0 to 0.7 in steps of 0.001
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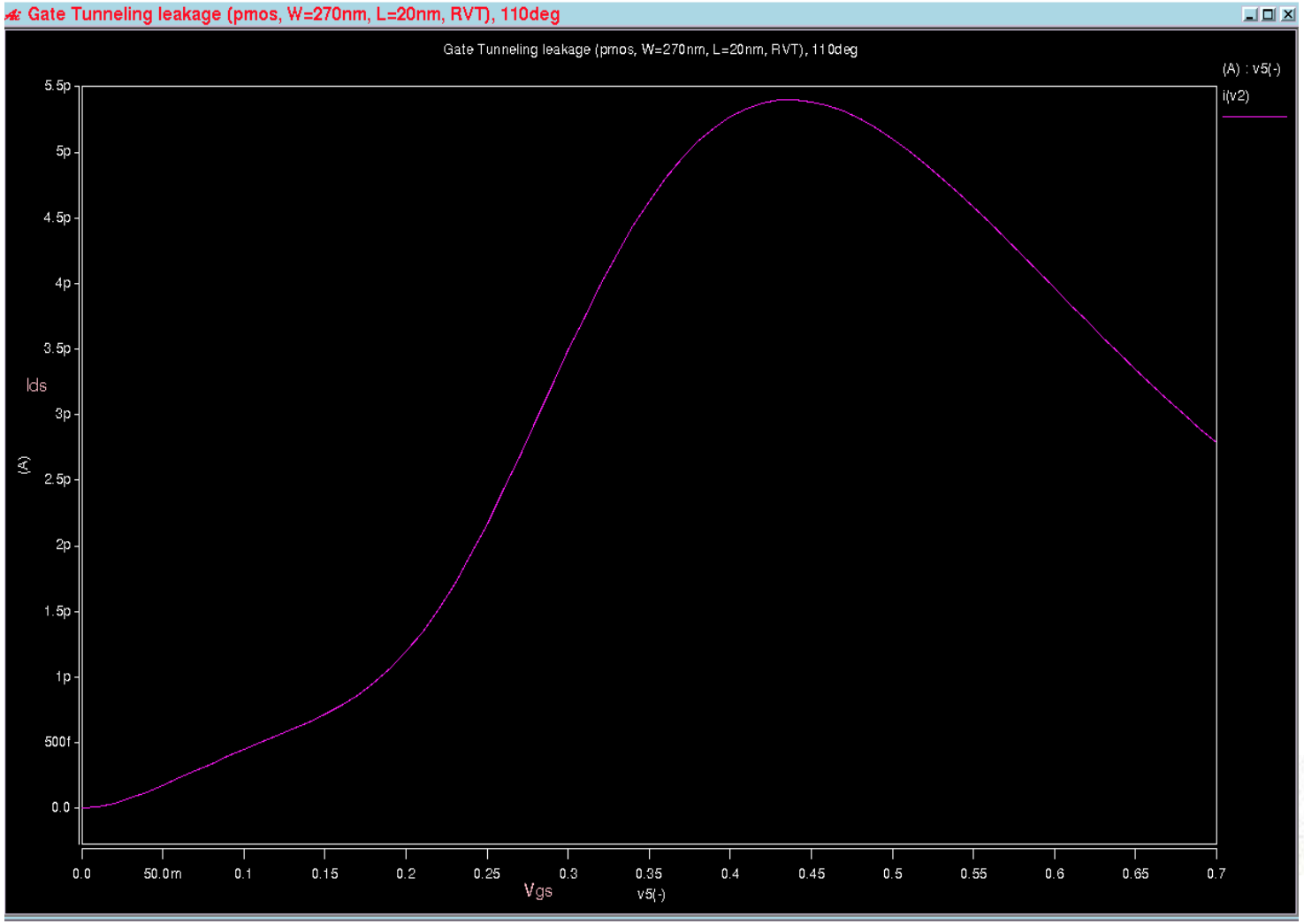
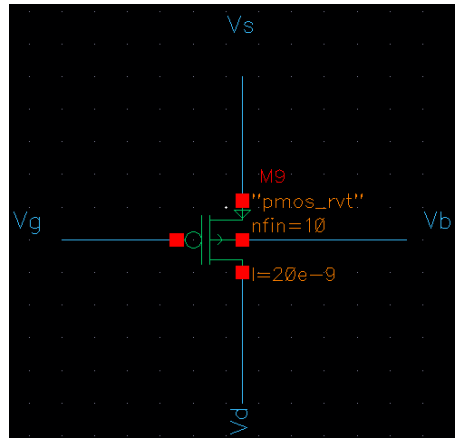
GATE TUNNELING LEAKAGE VERSUS VDD - PMOS

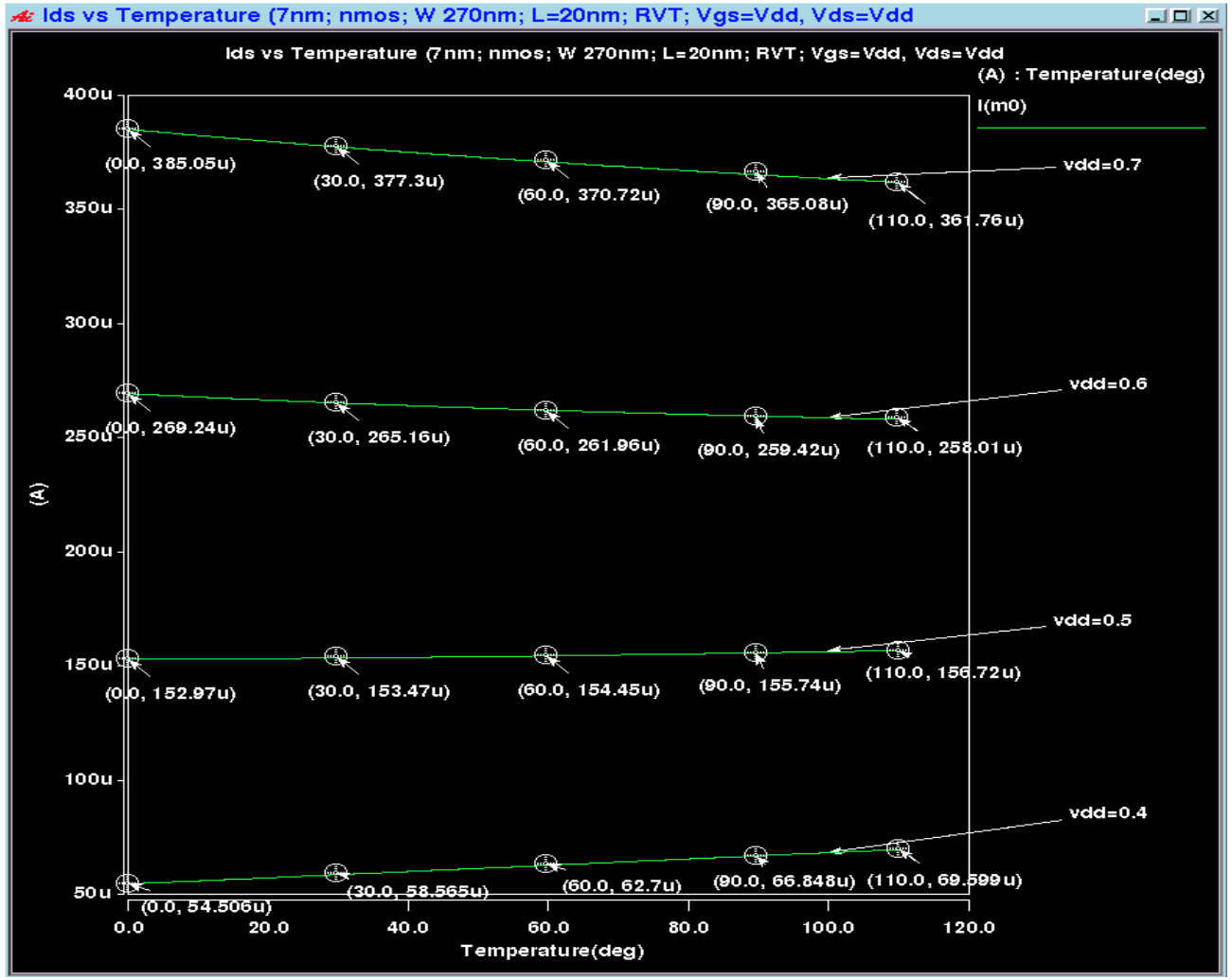
- Pmos the maximum gate leakage current is 5pA which is approximately 3 times lesser than nmos gate leakage

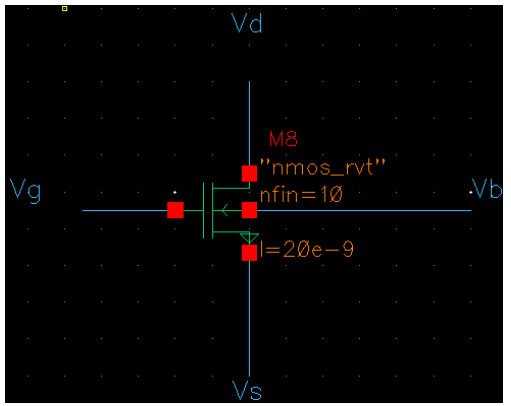





```
Vs=0 to 0.7 in steps of 0.001,
Vb=0 to 0.7 in steps of 0.001,
Vd = 0 to 0.7 in steps of 0.001
Vg= 0
```

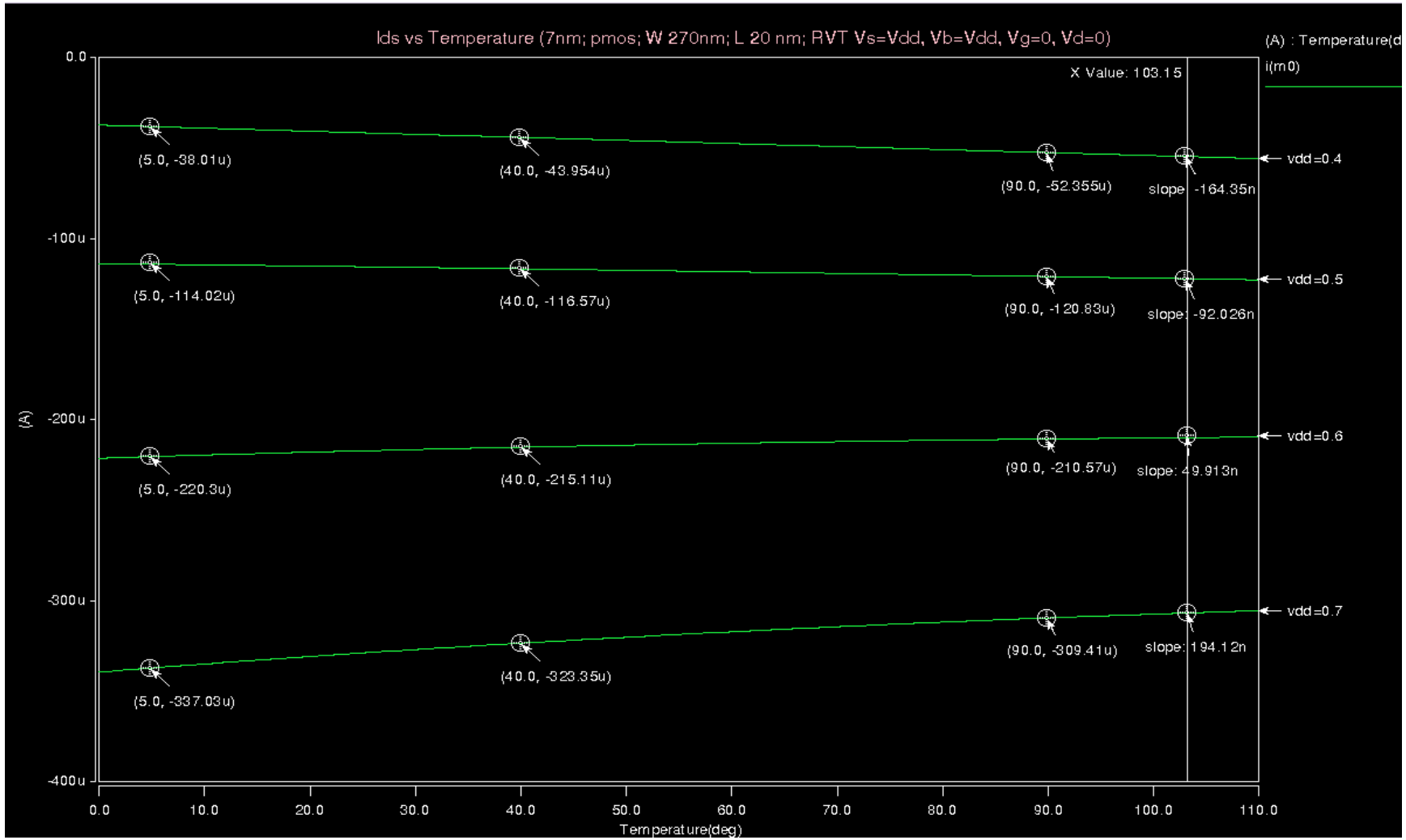
IDS (VGS=VDS=VDD) VERSUS TEMPERATURE (0C ~ 110C), FOR VDD=0.7V, 0.6V, 0.5V, 0.4V - NMOS

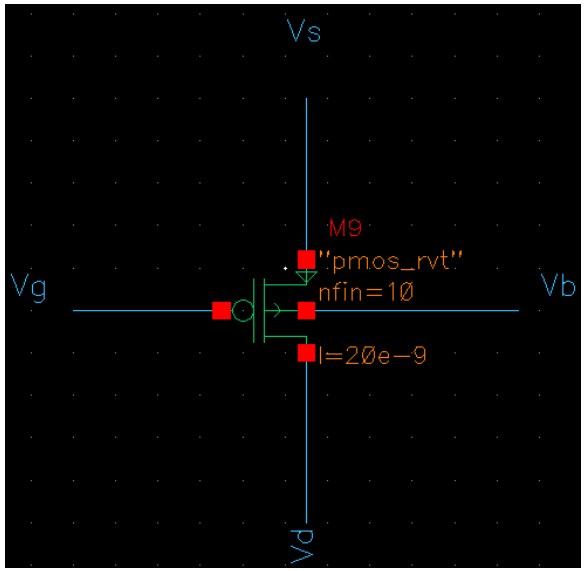




Vs=0, Vb=0,
Vd = 0.4 0.7 in steps of 0.1
Vg= 0.4 0.7 in steps of 0.1
temerature sweep from: 0-110 in steps of 0.5

IDS (VGS=VDS=VDD) VERSUS TEMPERATURE (0C ~ 110C), FOR VDD=0.7V, 0.6V, 0.5V, 0.4V - PMOS





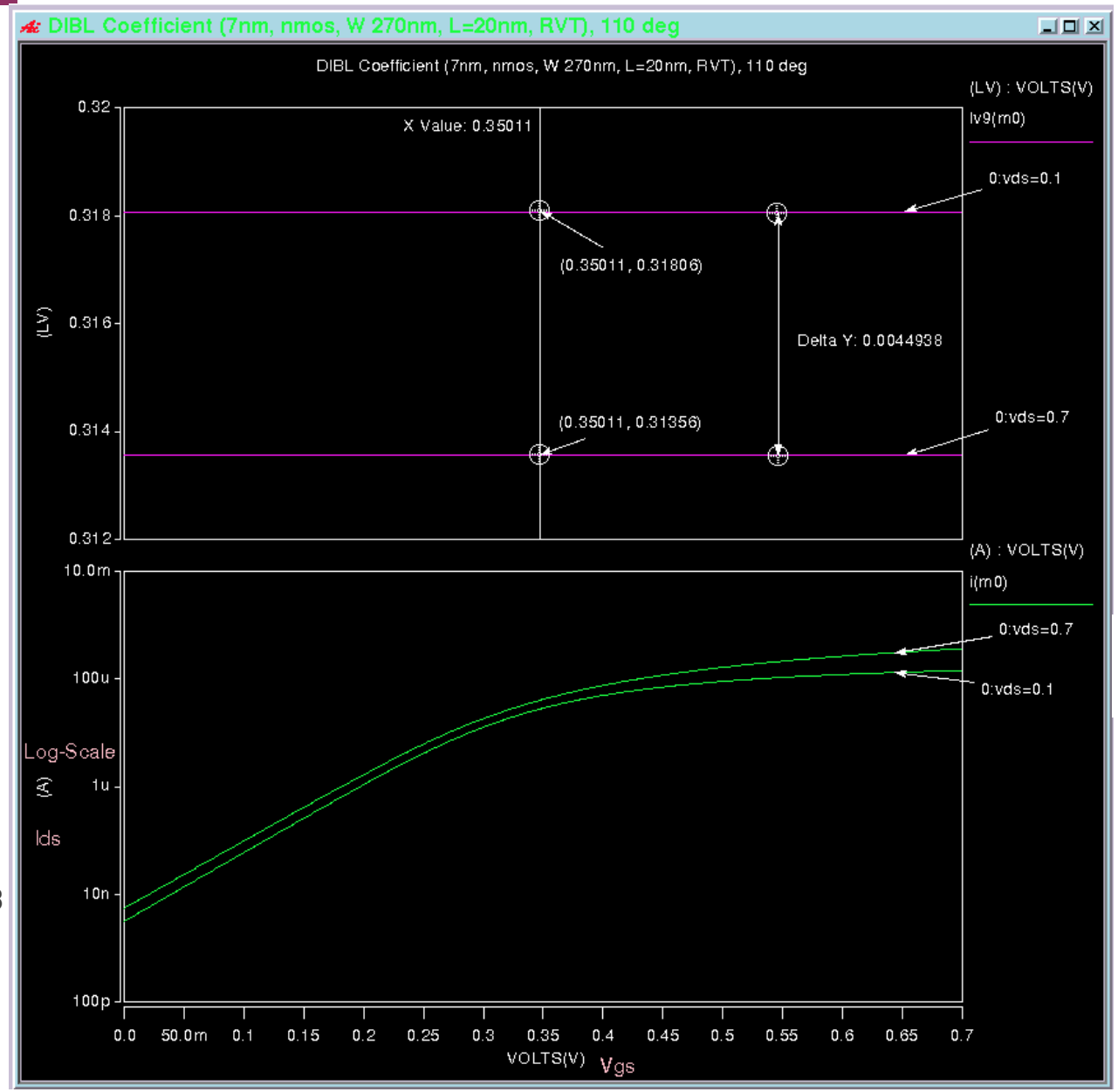
Vs=0.4 0.7 in steps of 0.1
Vb=0.4 0.7 in steps of 0.1
Vd = 0, Vg= 0
temerature sweep from: 0-110 in steps of 0.5

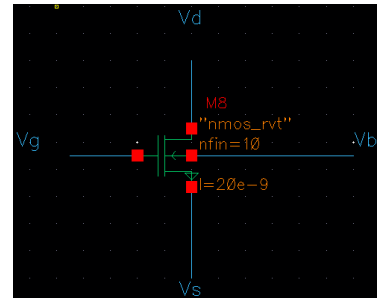
TEMPERATURE DEPENDENCE

- As temperature increases
  - Mobility decreases (scattering effect) => Ids decreases
  - Threshold voltage increase => Ids increases
- Based on the operating voltage either of the two phenomenon takes place
- If transistor is operating at region closer to Vt then Vt effect dominates => for higher temperature there is more current
- If transistor is operating at a higher voltage then mobility dominates => for higher temperature the current is lesser
- This behavior is clearly seen in the graph show in in previous two slides
- For Vdd of 0.7, 0.6 current is reducing as temperature increases
- For Vdd of 0.4, 0.5 current is increasing as temperature increases
- The dependance of temperature is same for both nmos and pmos

DIBL COEFFICIENT [V/V] - NMOS

- DIBL refers to Drain Induced barrier lowering; it refers to lowering of Vt on increased Vds (because of increasing depletion layer width)
- Vt= Vt0 - (ñ)Vds where ñ is dibl coefficient
- As seen from the curve as Vds is increased Vt has reduced.
- Vt for Vds=0.7V is 0.31356V
- Vt for Vds=0.1V is 0.31806V
- Lv9(mo) shows the Vt value
- Ids vs Vgs (logscale) is plotted and the curve has shifted as shown in fig.
- DIBL coefficient for nmos from figure is obtained as (ΔVt)/(ΔVds)= 0.0044/0.6=0.0073

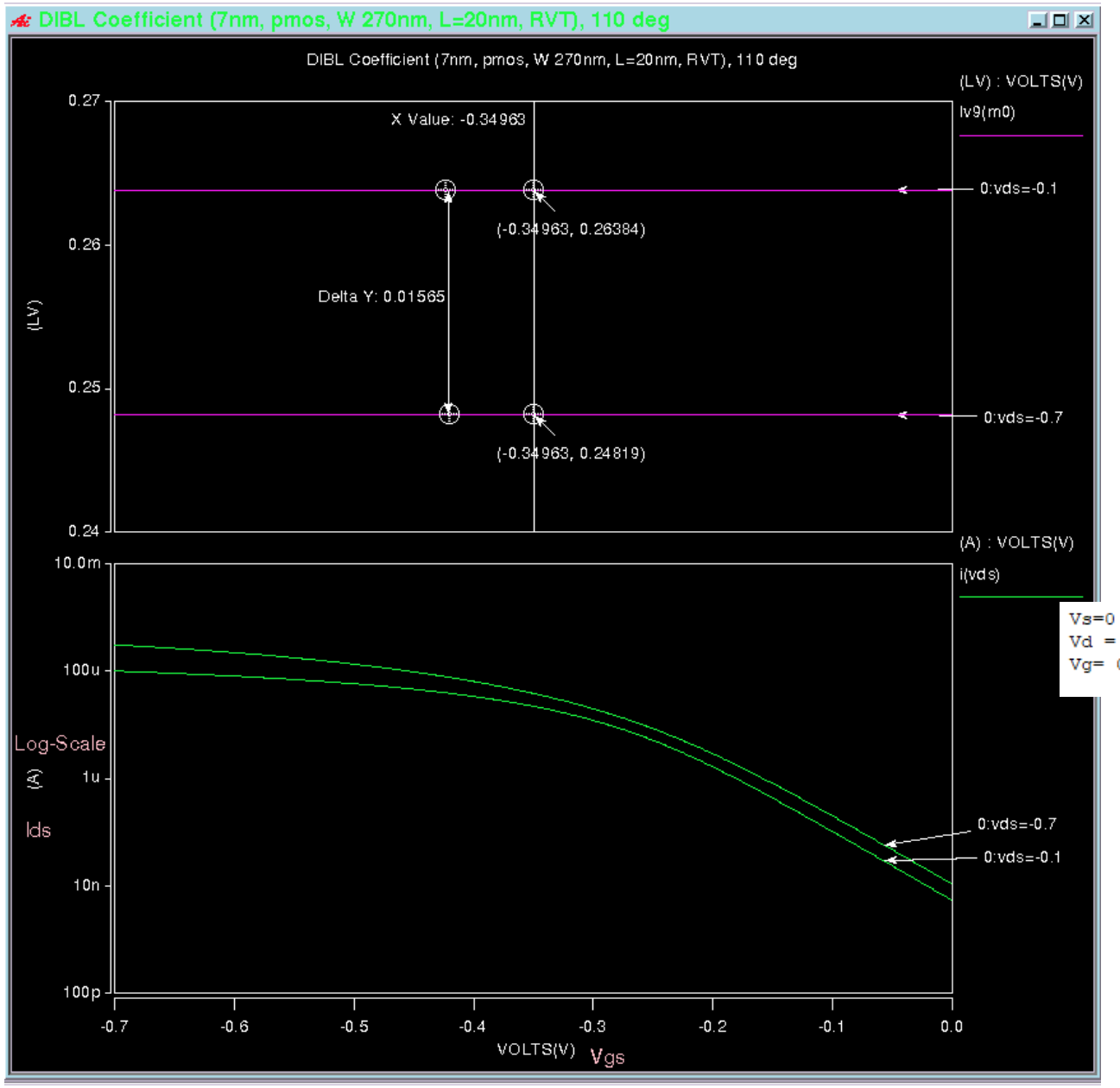


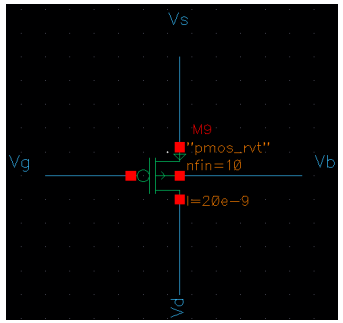


Vs=0, Vb=0,
Vd = 0.1, 0.7
Vg= 0 0.7 in steps of 0.001

DIBL COEFFICIENT [V/V] - PMOS

- DIBL refers to Drain Induced barrier lowering; it refers to lowering of Vt on increased Vds (because of increasing depletion layer width)
- Vt= Vt0 - (ñ)Vds where ñ is dibl coefficient
- As seen from the curve as Vds is increased Vt has reduced.
- Vt for Vds=-0.7V is 0.24819V
- Vt for Vds=-0.1V is 0.26384V
- Lv9(mo) shows the Vt value
- Ids vs Vgs is plotted and the curve has shifted as shown in fig.
- DIBL coefficient for pmos from figure is obtained as (ΔVt)/(ΔVds)= 0.01565/0.6=0.02608
- DIBL coefficient for pmos is higher as (ΔVt) for pmos is higher

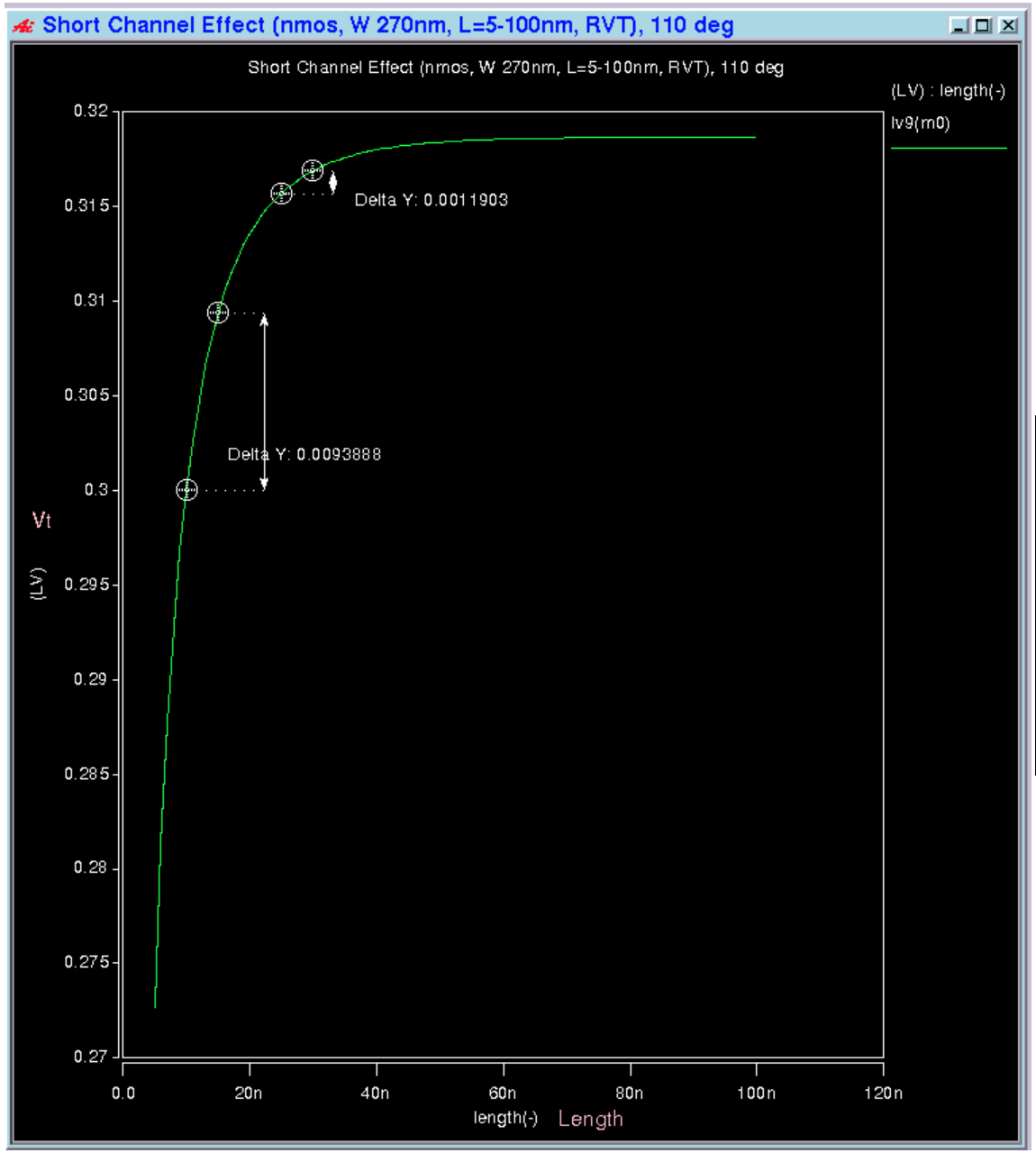


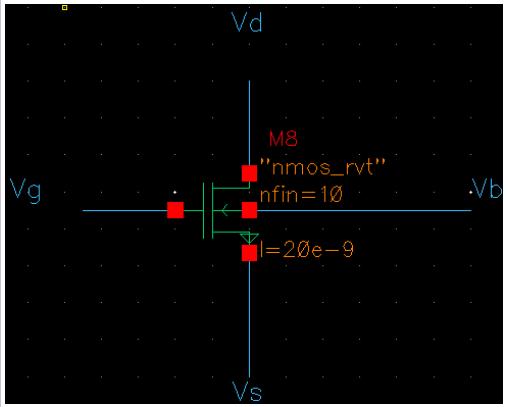


Vs=0 , Vb=0
Vd = -0.7,-0.1,
Vg= 0 to -0.7 in steps of -0.001

SHORT CHANNEL EFFECT - NMOS

- Short channel effect refers to variation of Vt wrt length
- For ASAP 7nm PDK the channel length is 20 nm.
- As it can be seen as the length decreases(<20nm) the variation in Vt is very drastic (Delta Y is more for same delta x) ie for a small change in length there is a large change in Vt
- But for length greater than 20 nm there is not much variation

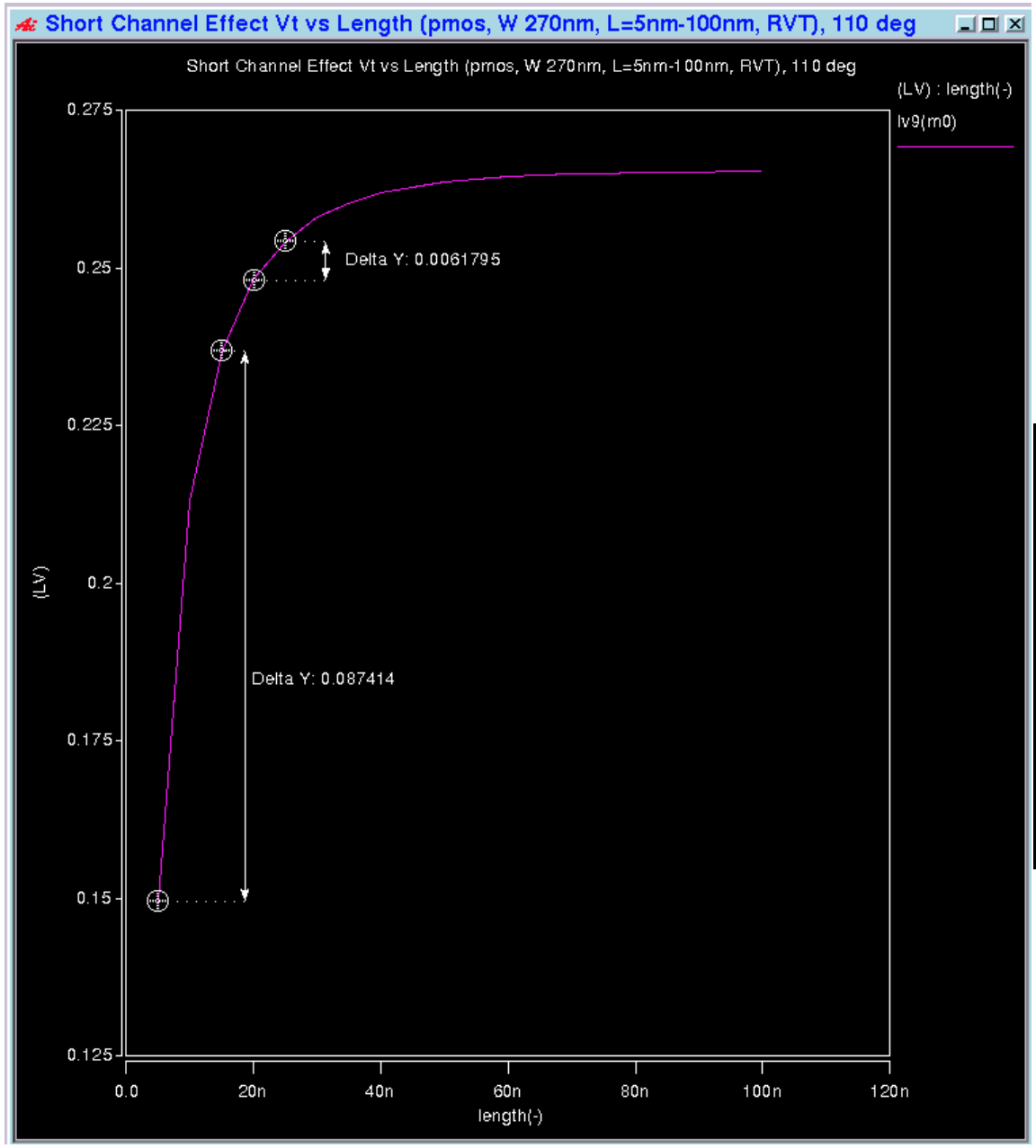


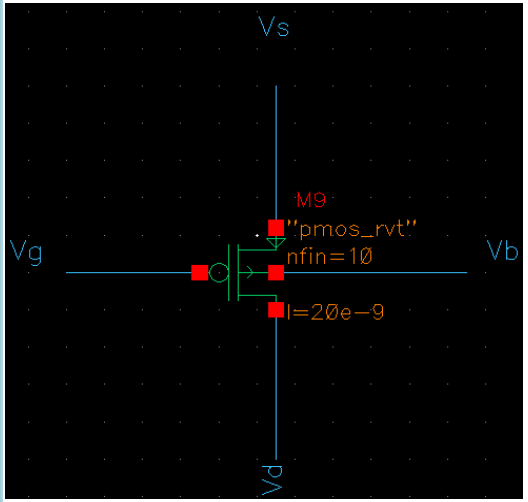



```
Vs=0, Vb=0,
Vd =  0.7
Vg=  0.7
length sweep 5nm-100nm
```

SHORT CHANNEL EFFECT - PMOS

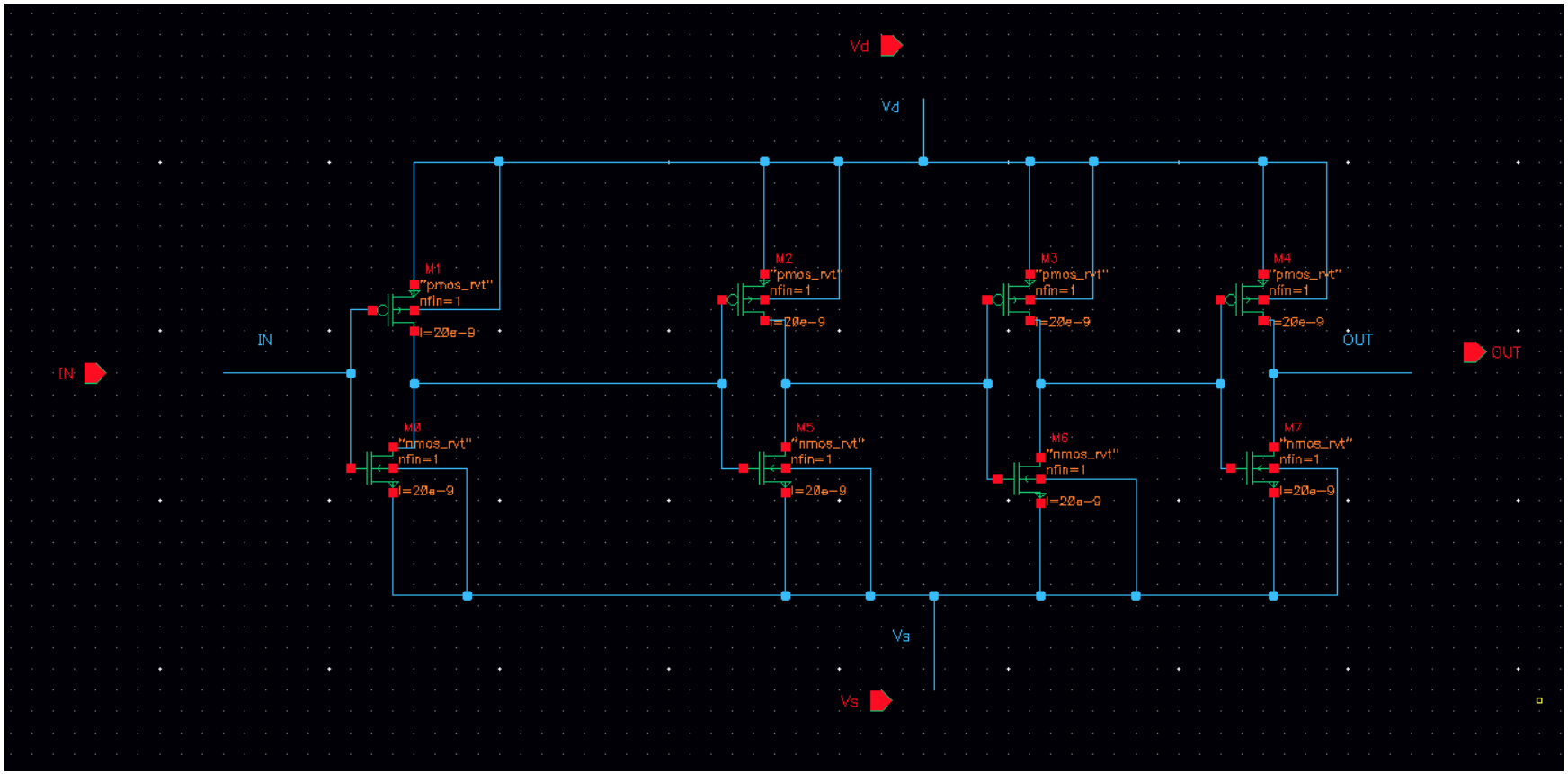
- Short channel effect refers to variation of Vt wrt length
- For ASAP 7nm PDK the channel length is 20 nm.
- As it can be seen as the length decreases(<20nm) the variation in Vt is very drastic (Delta Y is more for same delta x) ie for a small change in length there is a large change in Vt
- But for length greater than 20 nm there is not much variation
- Short channel effect follows the same behavior for nmos and pmos





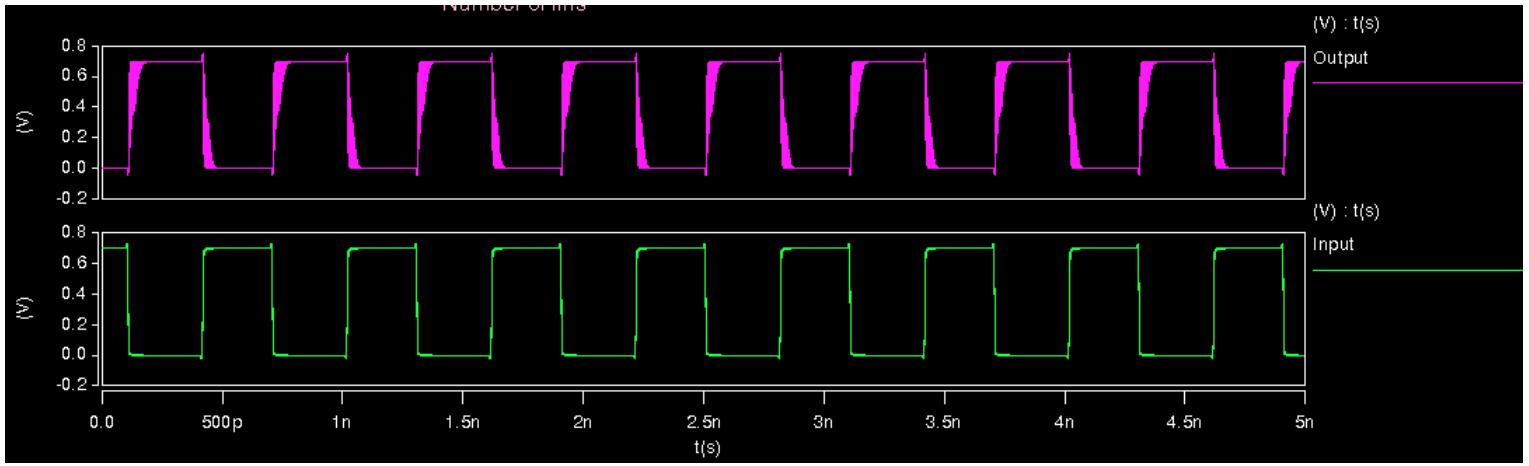
Vs=0 , Vb=0.7
Vd = 0.7
Vg= 0
length sweep 5nm-100nm

7. DELAY CHARACTERIZATION OF INVERTER - SCHEMATIC



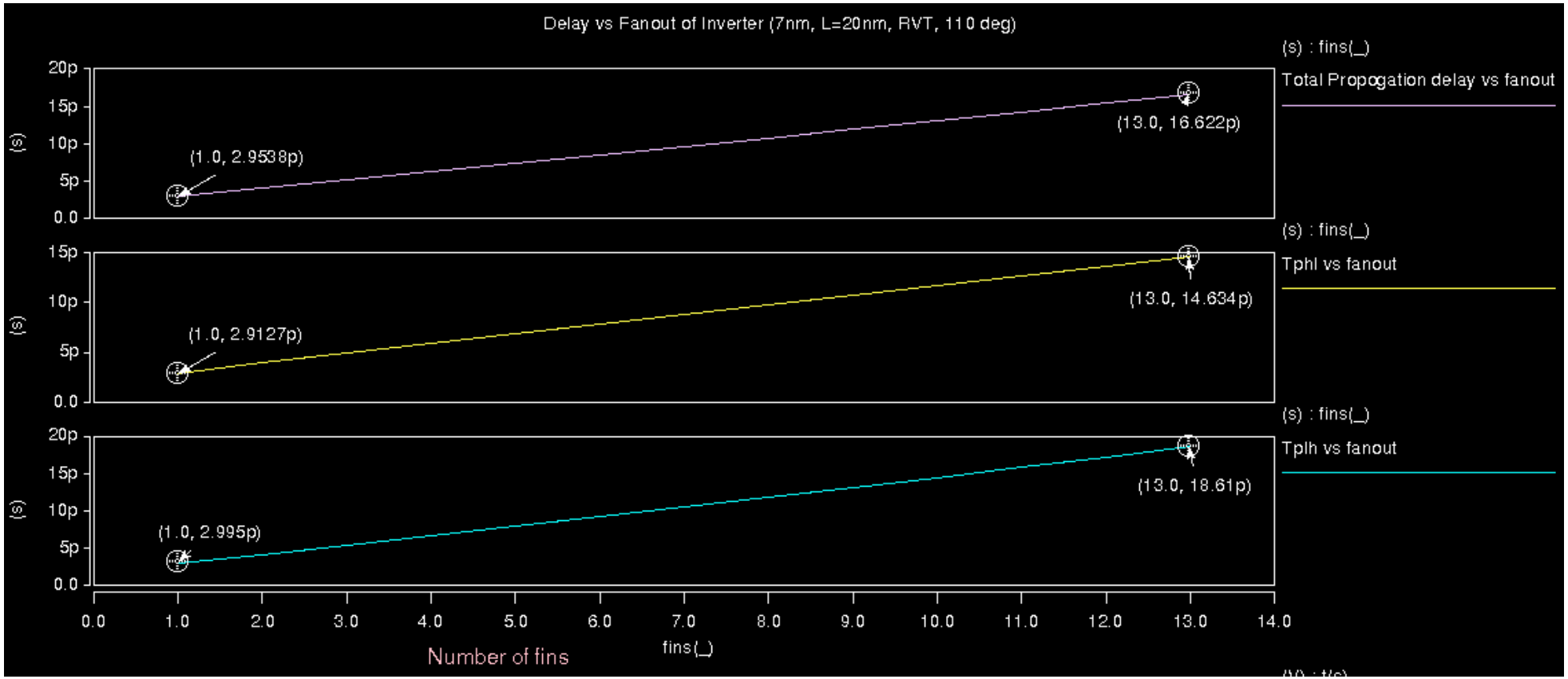
- For characterizing delay of an inverter 4 inverters are placed.
- 1st inverter makes sure that input is a curve and not a step input
- 2nd inverter is the inverter to be characterized
- 3 rd inverter acts as a load. Therefore the width of this 3rd inverter is changed to vary the load capacitance
- There is a 4th inverter kept to account for the miller effect of 3rd inverter

INPUT : INPUT OF 2ND INVERTER
OUTPUT: OUTPUT OF 2ND INVERTER FOR DIFFERENT FANOUTS



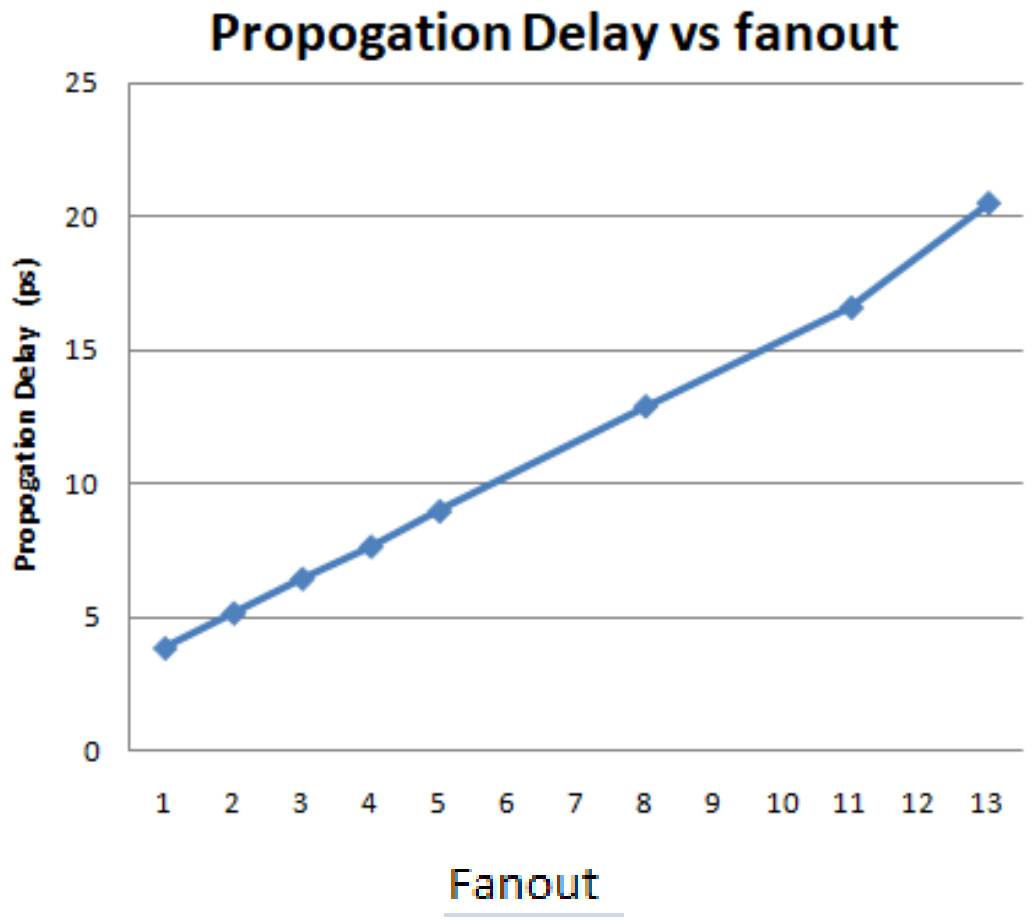
- As shown in previous slide the voltage given at
  - Vd :VDD=0.7V
  - Vs :VSS=0V
  - IN : Clock pulse with on time 300 ps, off time 300 ps
- Parameter width=81e-9*fanout
- # Fin = 3* fanout
- Fanout is swept from 1 to 13

DELAY (T PHL ,T PLH ,AND AVERAGE OF THE TWO) VERSUS FANOUT OF AN INVERTER- SCHEMATIC

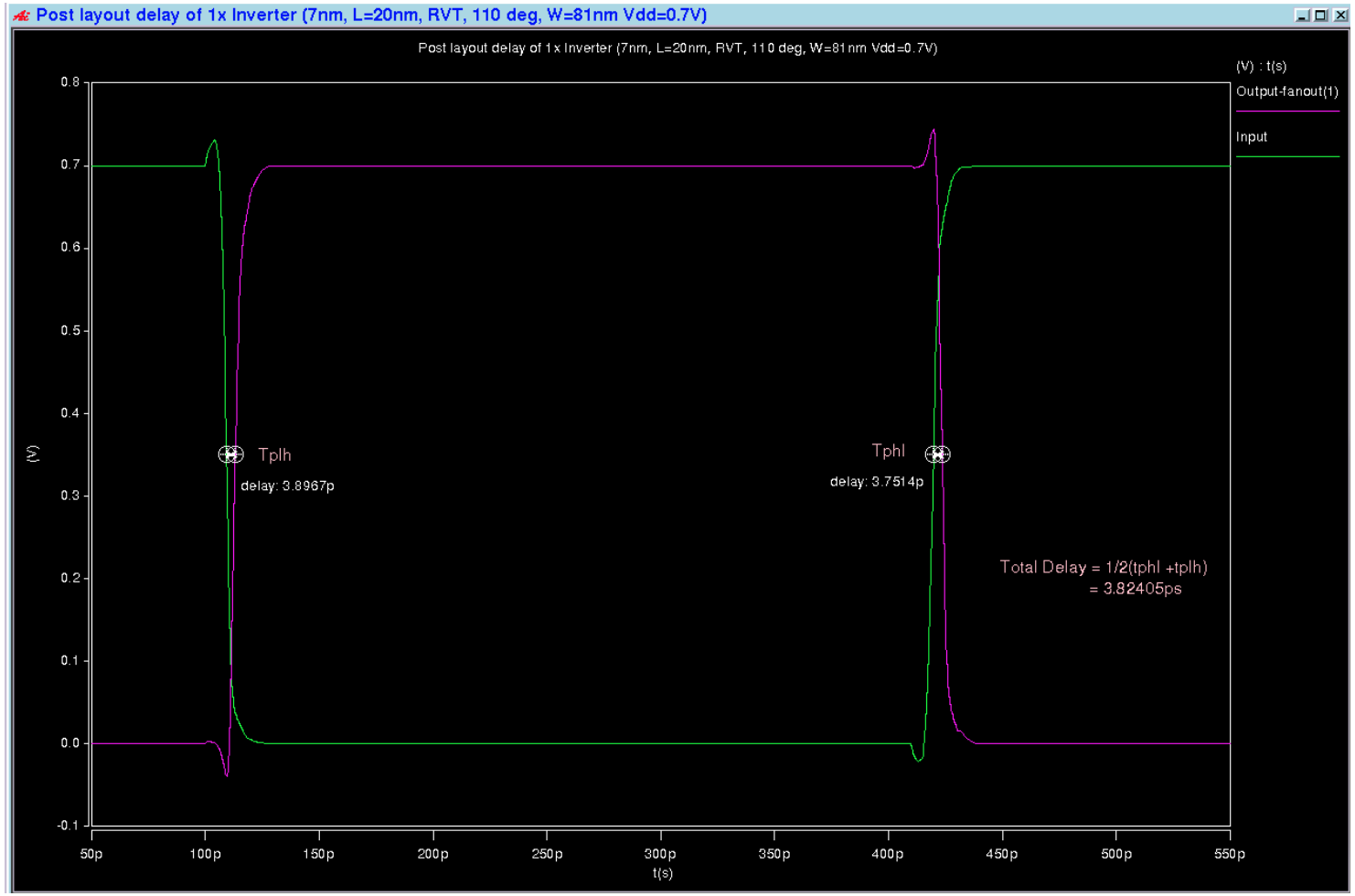


- Delay is a function of (Reff * Cl) ln 2
- As the fanout increases the load capacitance increases
- Also tp= tp0(1+f/(gama))
- Therefore we see delay vs fanout graph as a linear function
- tplh delay for a fanout of 1 inverter is 2.995 ps
- tphl delay for a fanout of 1 inverter is 2.9127 ps
- Total propgation delay is the average of two = 2.9538 ps

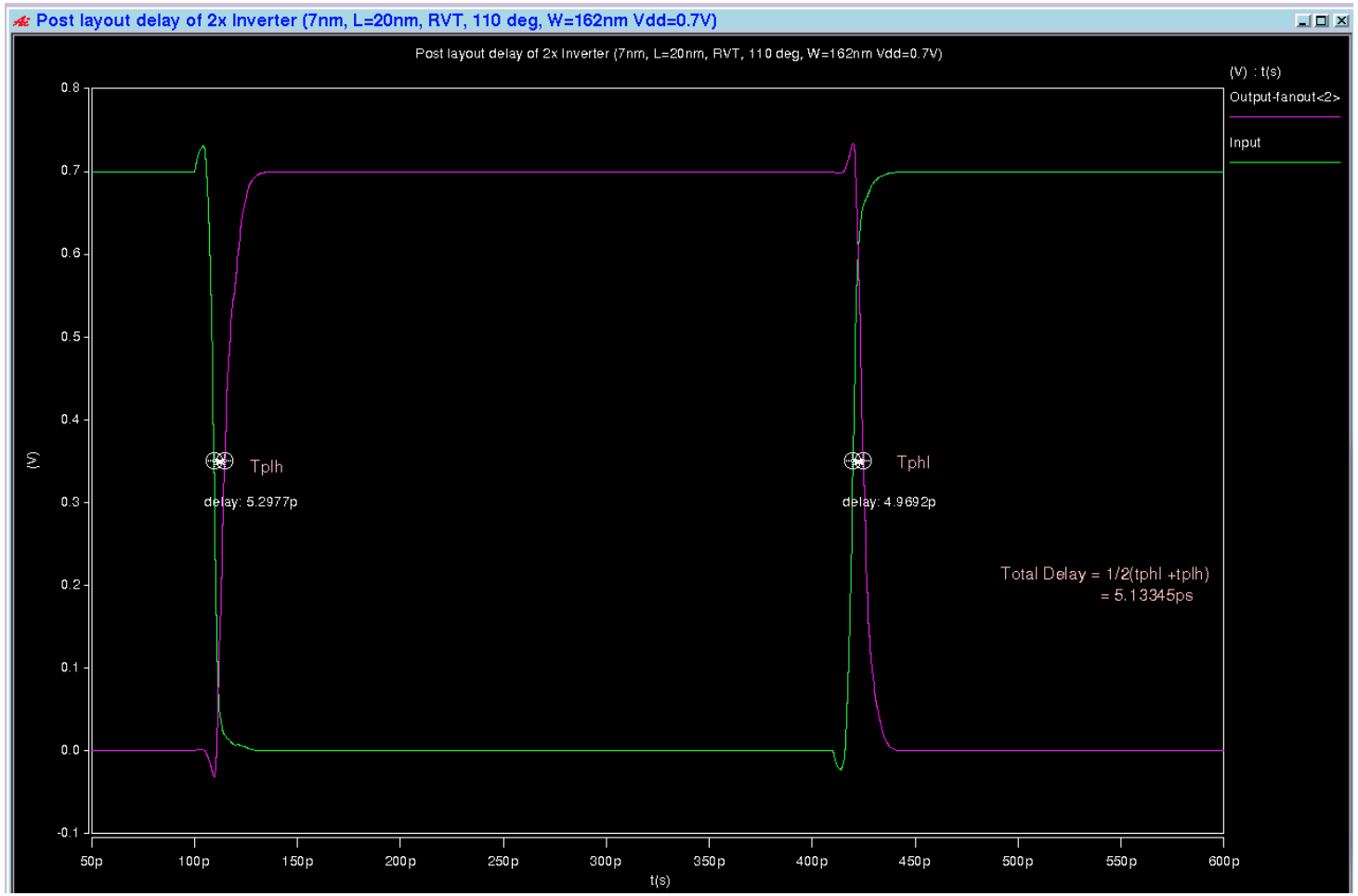
LAYOUT- DELAY VS FANOUT



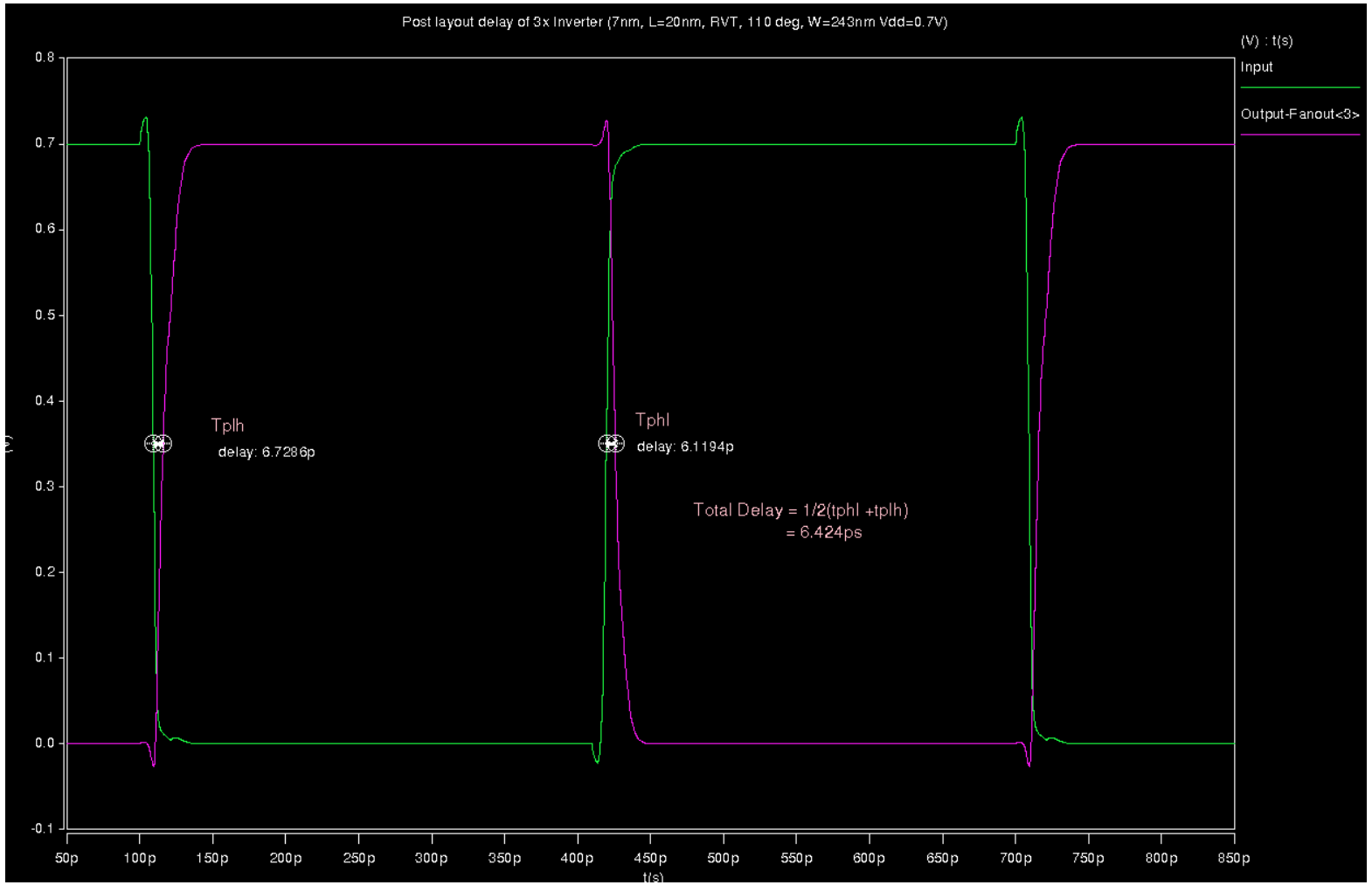
DELAY FOR 1X INVERTER- LAYOUT



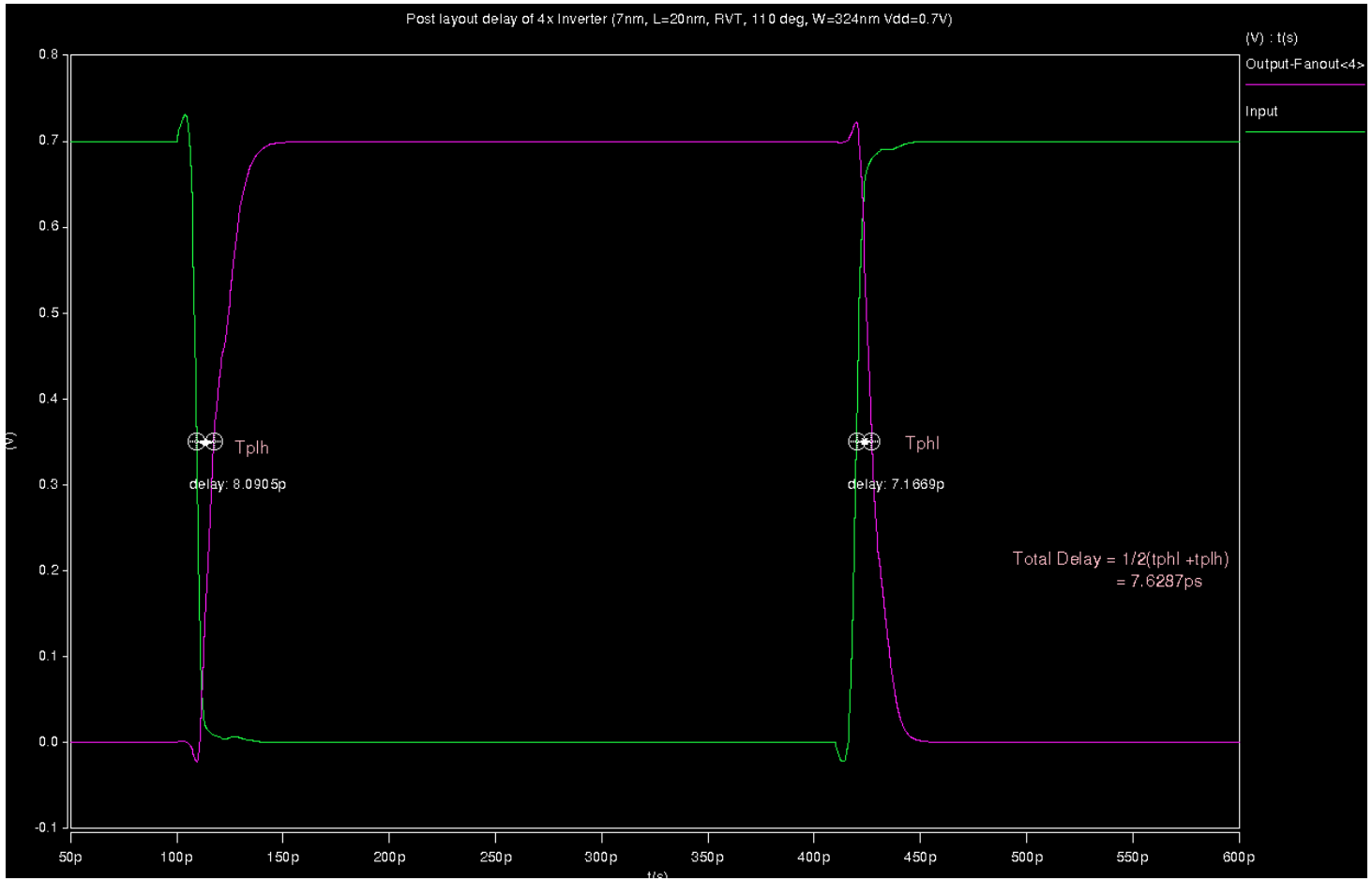
DELAY FOR 2X INVERTER- LAYOUT



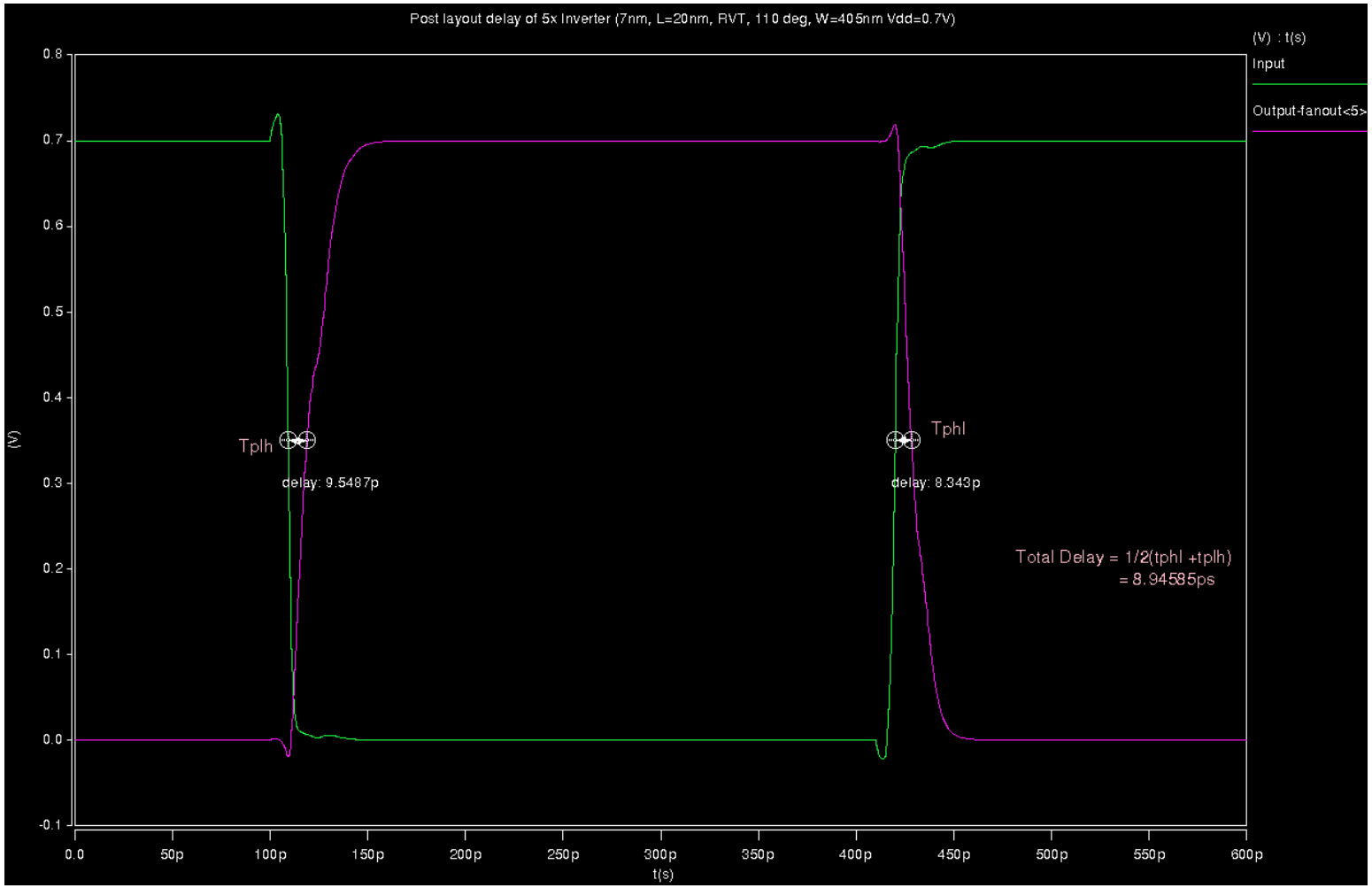
DELAY FOR 3X INVERTER - LAYOUT



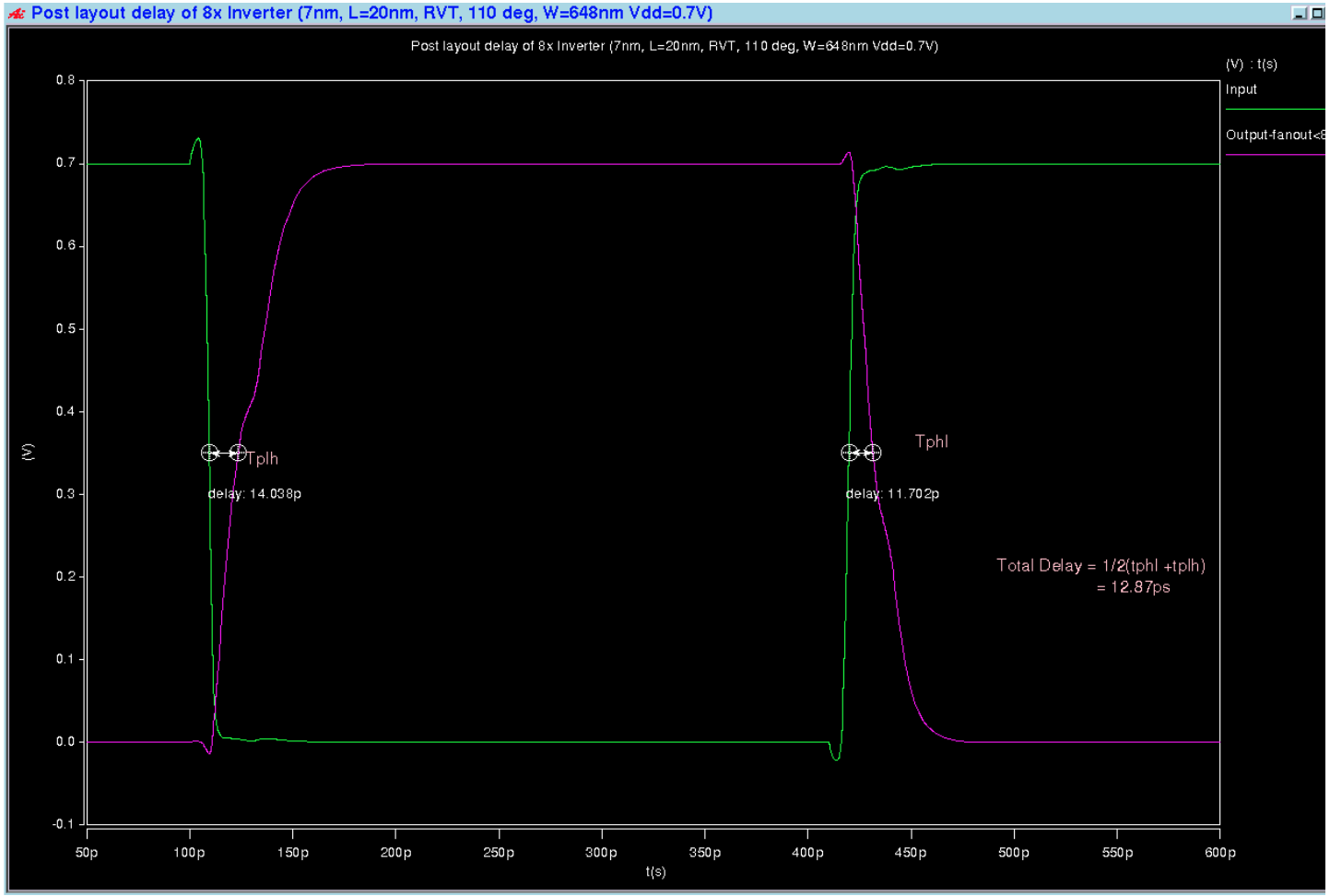
DELAY FOR 4X INVERTER- LAYOUT



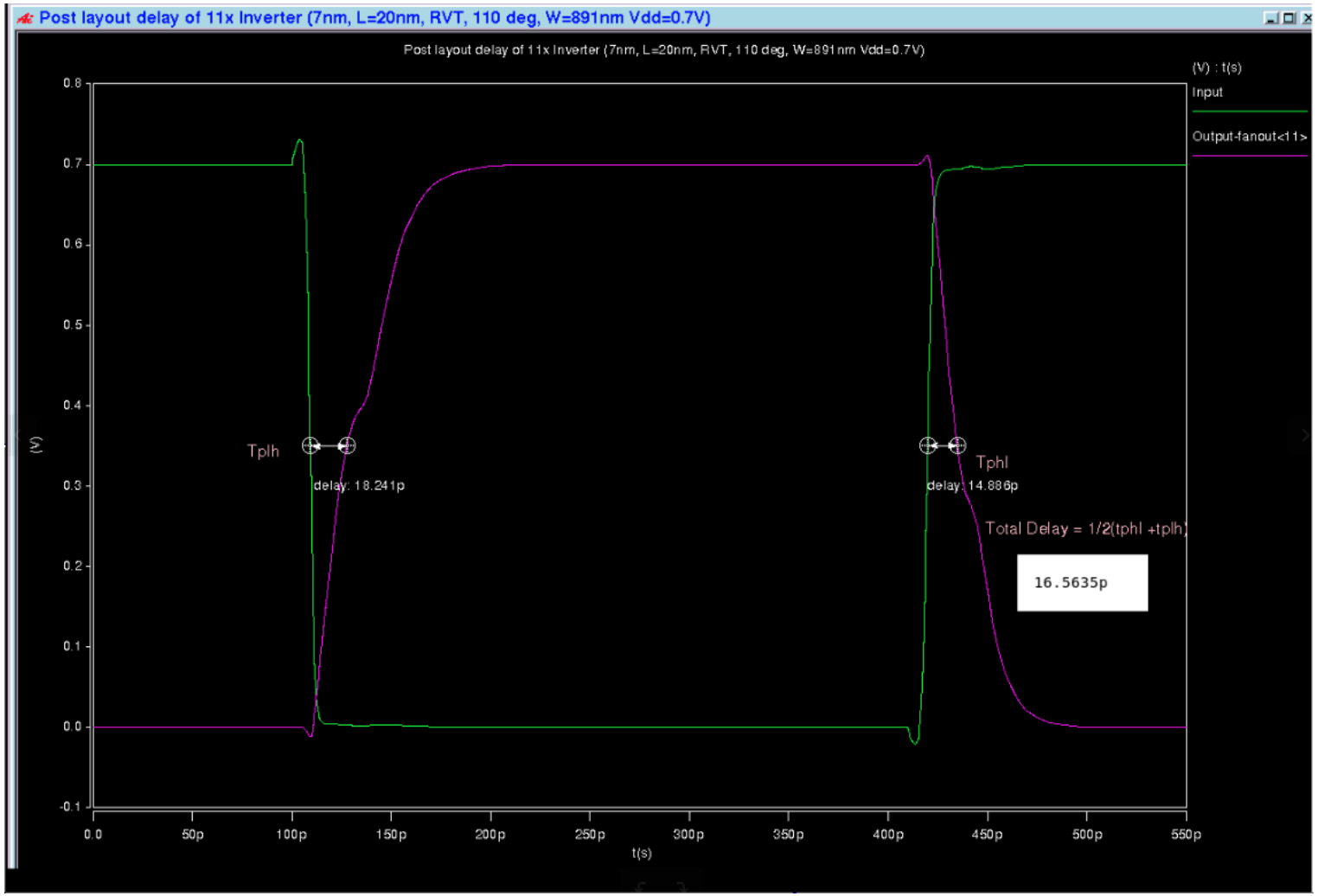
DELAY FOR 5X INVERTER - LAYOUT



DELAY FOR 8X INVERTER - LAYOUT



DELAY FOR 11X INVERTER - LAYOUT



DELAY FOR 13X INVERTER - LAYOUT