EE5323 HOMEWORK #4

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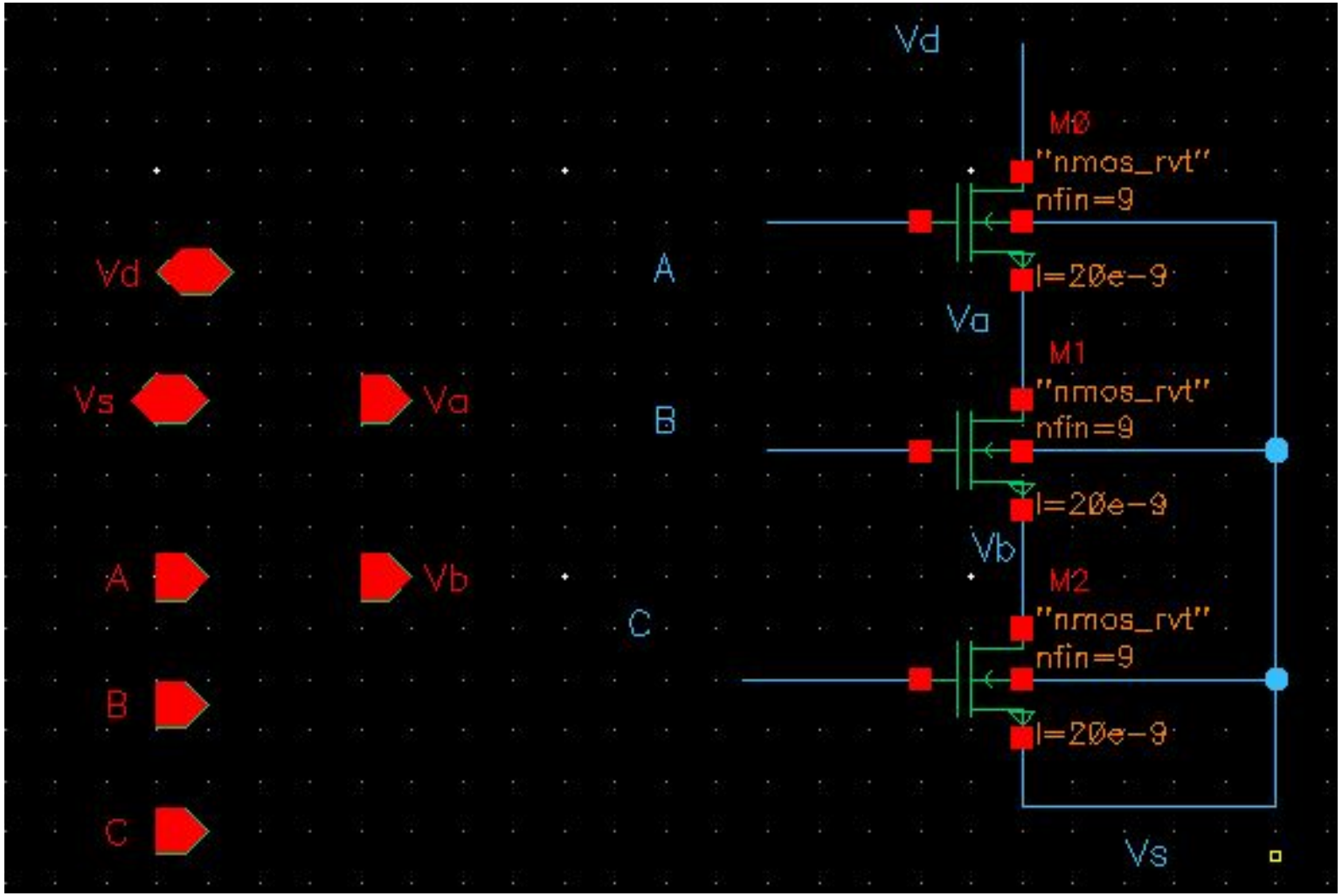
Question 1

The figure on the right shows the three stacked nmos (9 fin for each nmos)

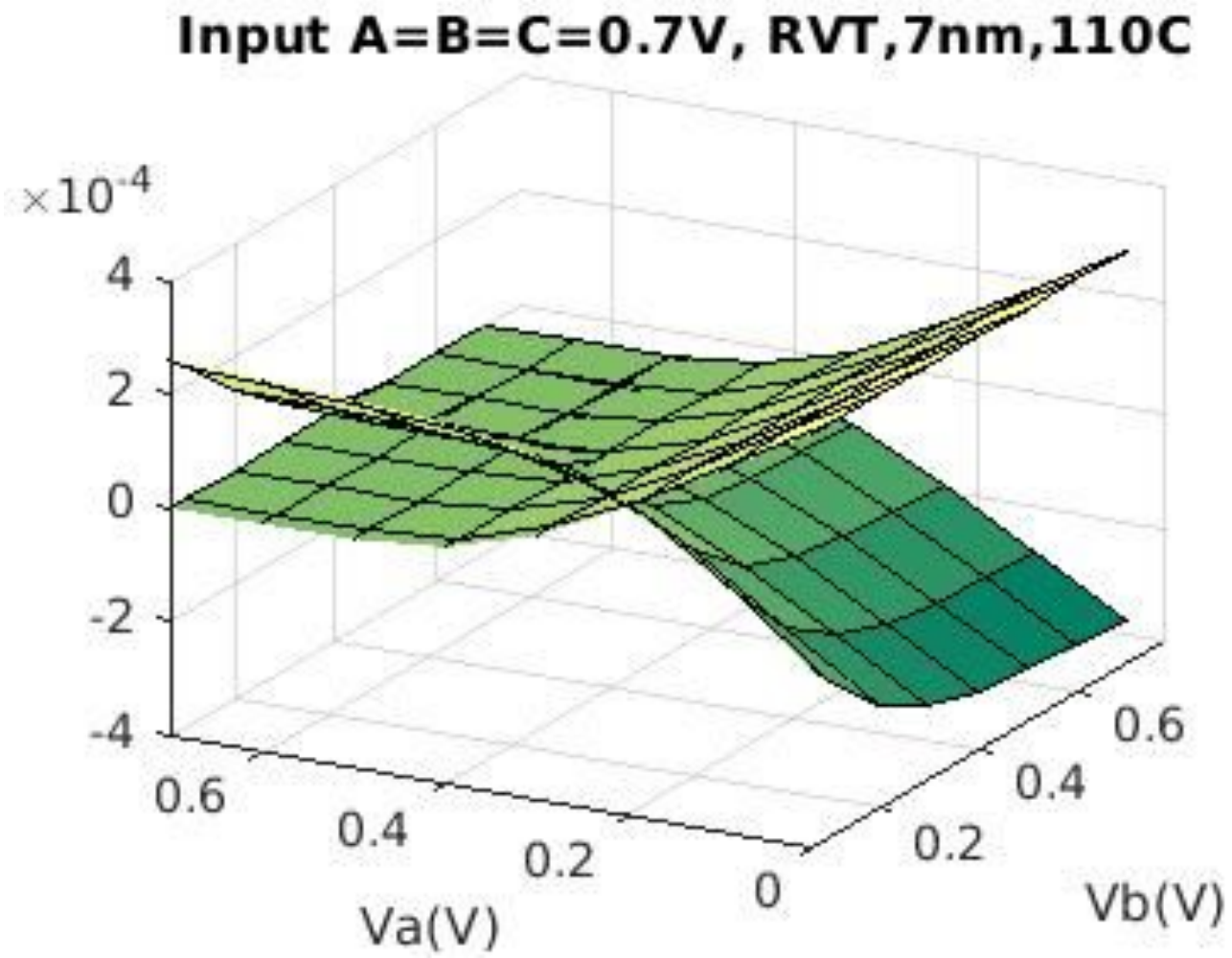
The Va, Vb are swept from 0 to 0.7V in steps of 0.1V

Vd=0.7V, Vs=0V



Case1: Inputs A=B=C=0.7V Load Line Analysis

The figure on the right shows the 3D plot of current vs Va, Vb which is plotted using Matlab

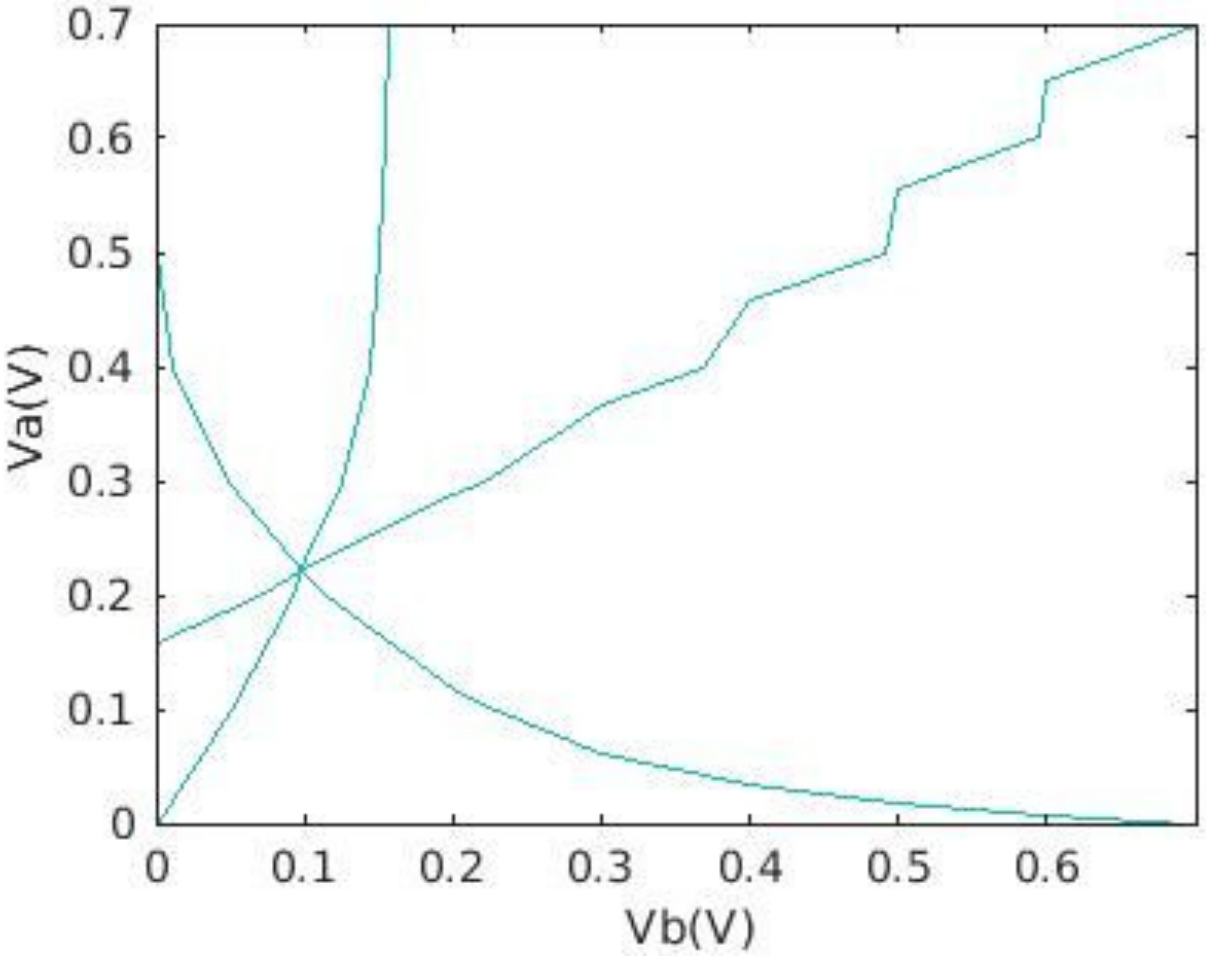


Case1: Inputs A=B=C=0.7V Load Line Analysis (cont.)

The figure on the right shows the intersection point of Va, Vb

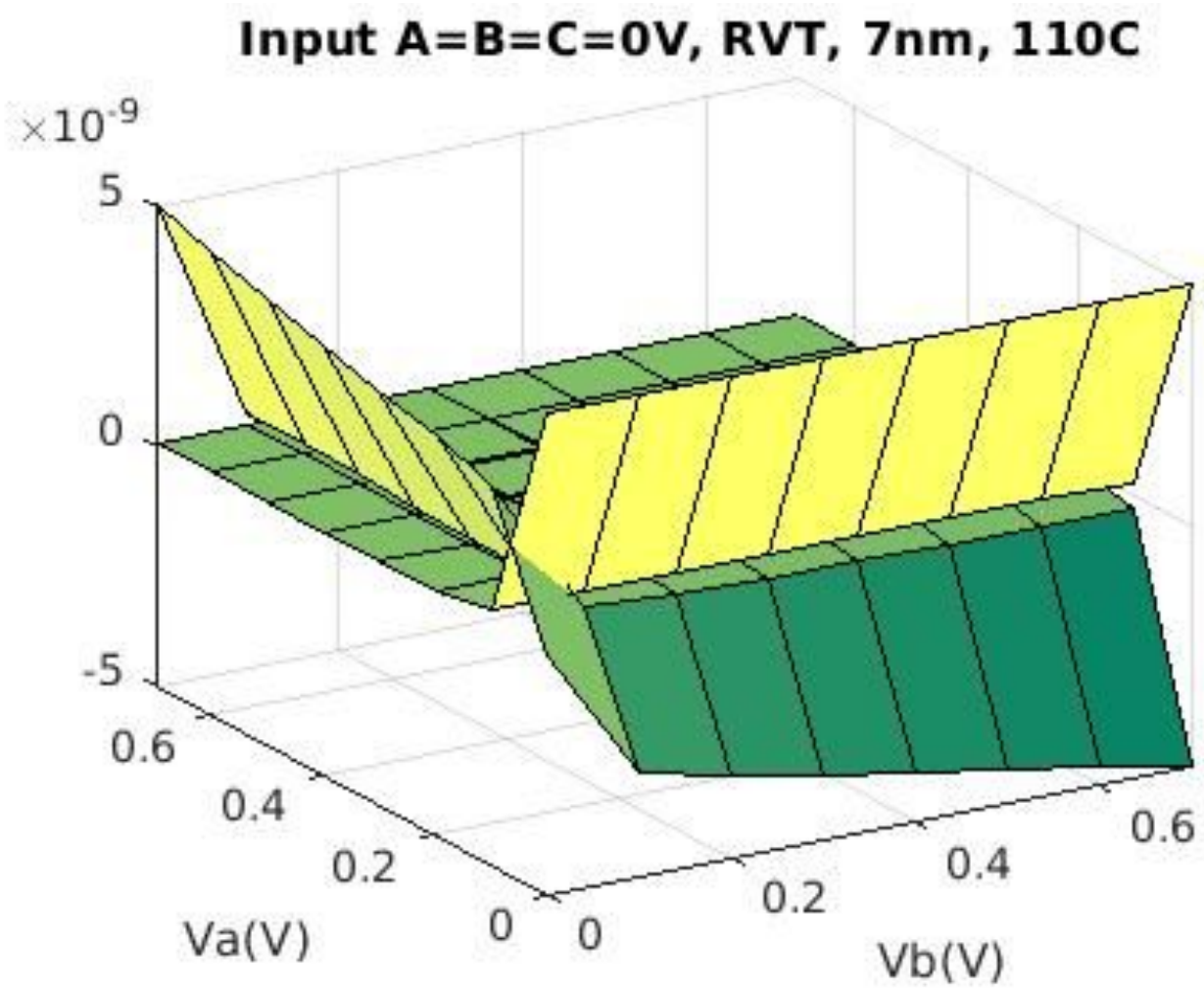
The point at which they intersect is Va=0.2V, Vb=0.1V, so this is the bias volatge.

The bias current is 4.3microA



Case1: Inputs A=B=C=0V Load Line Analysis

The figure on the right shows the 3D plot of current vs Va, Vb

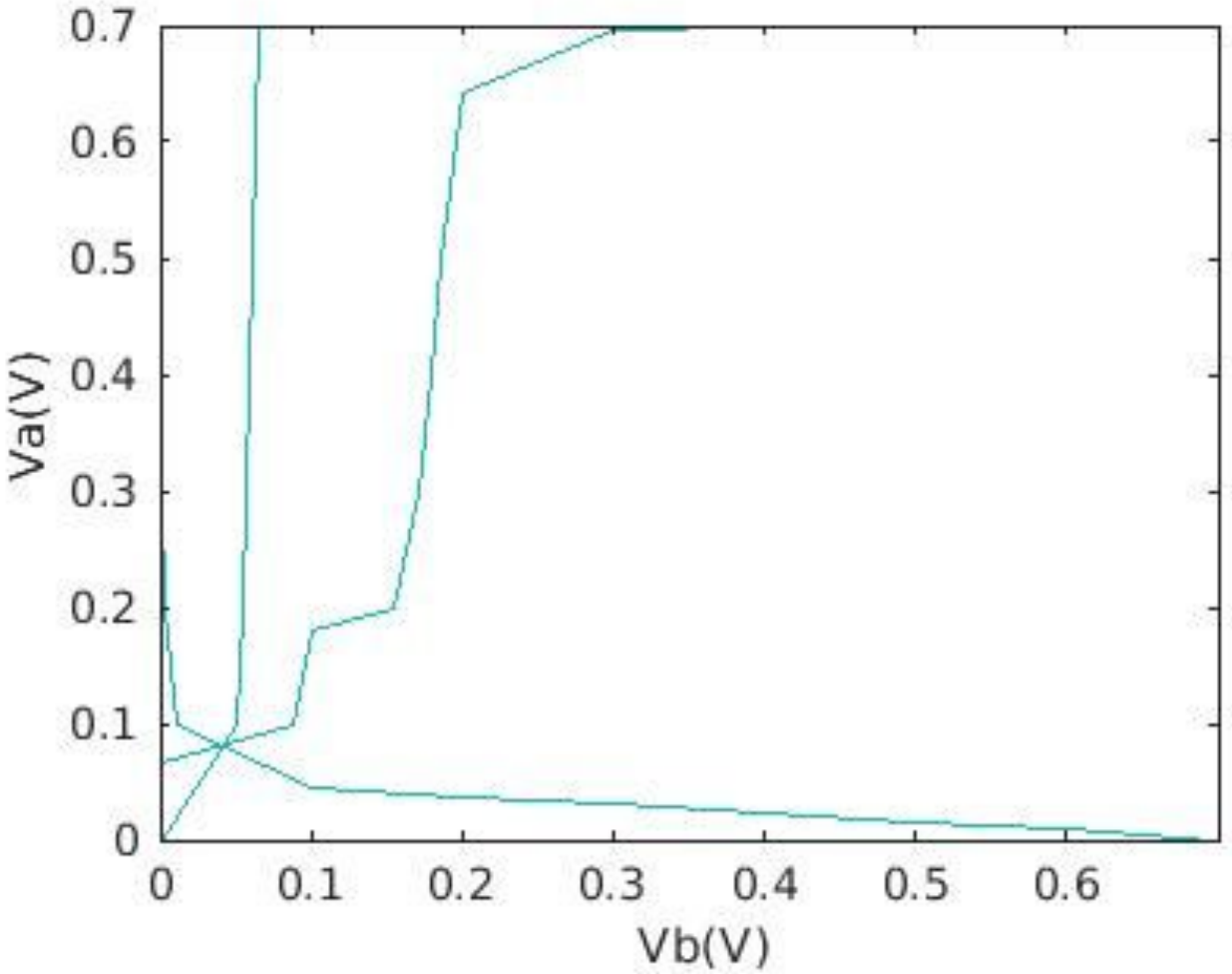


Case1: Inputs A=B=C=0V Load Line Analysis (cont.)

The figure on the right shows the intersection point of Va, Vb

The point at which they intersect is Va=0.1V, Vb=0.05V and this is the bias voltage

The bias current is 0.35nA



Matlab code for plotting the 3D load line analysis and intersection point

Matlab was used to plot the 3D graphs and surf is used to plot data, contour is used to find intersection

Code is attached in the zip file

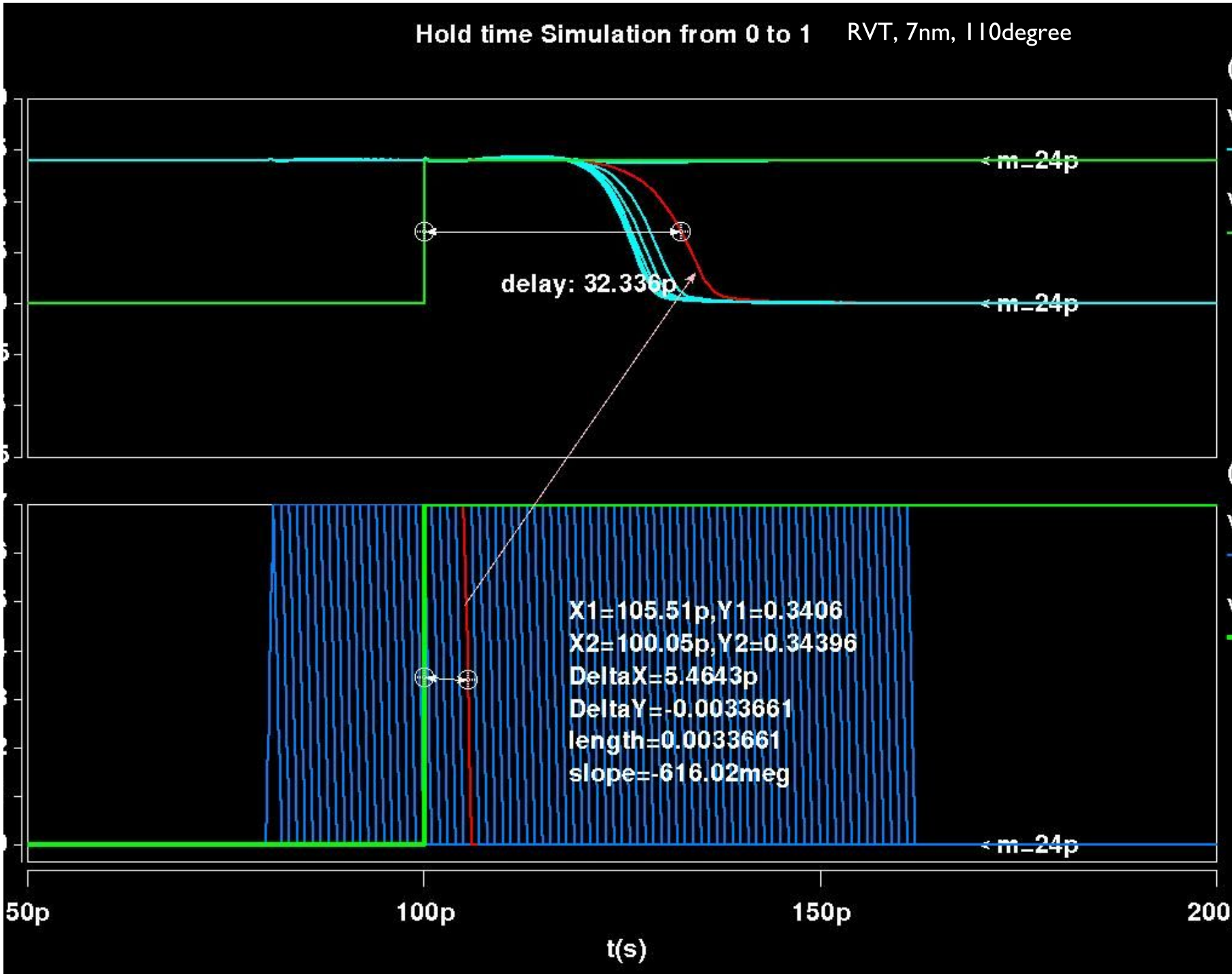
Attached simulation files and netlist

QUESTION 2 : Hold time 0 to1

The figure on the right shows the hold time simulation.

If the data changes before 5ps after clock edge then transition can't be captured

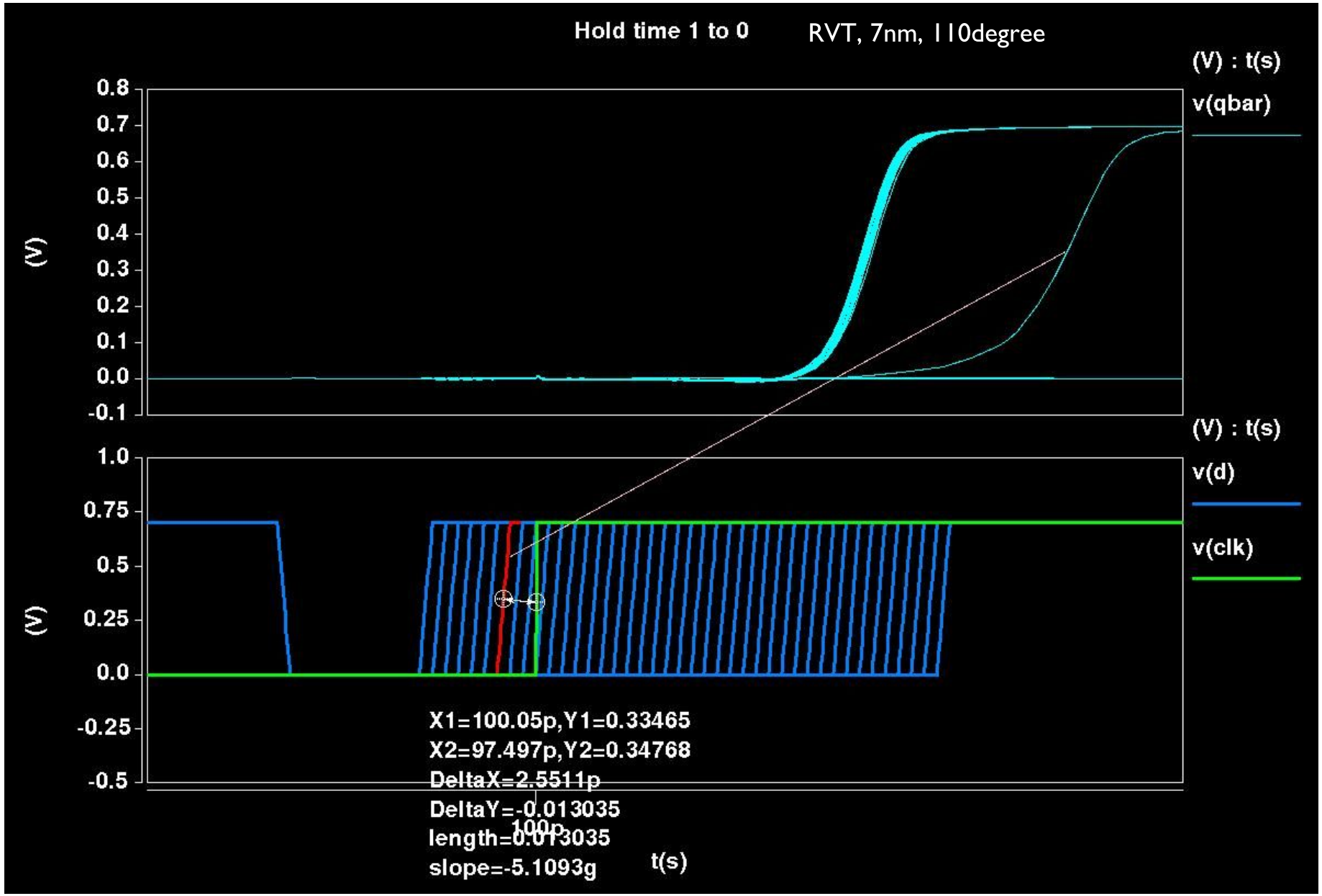
Therefore the data should be at-least kept in stable state approx 5ps after clock edge



Hold time 1 to 0

The figure in right shows the simulation of hold time for the transition 1 to 0.

The hold time in case of 1 to 0 is found to be before the clock edge.

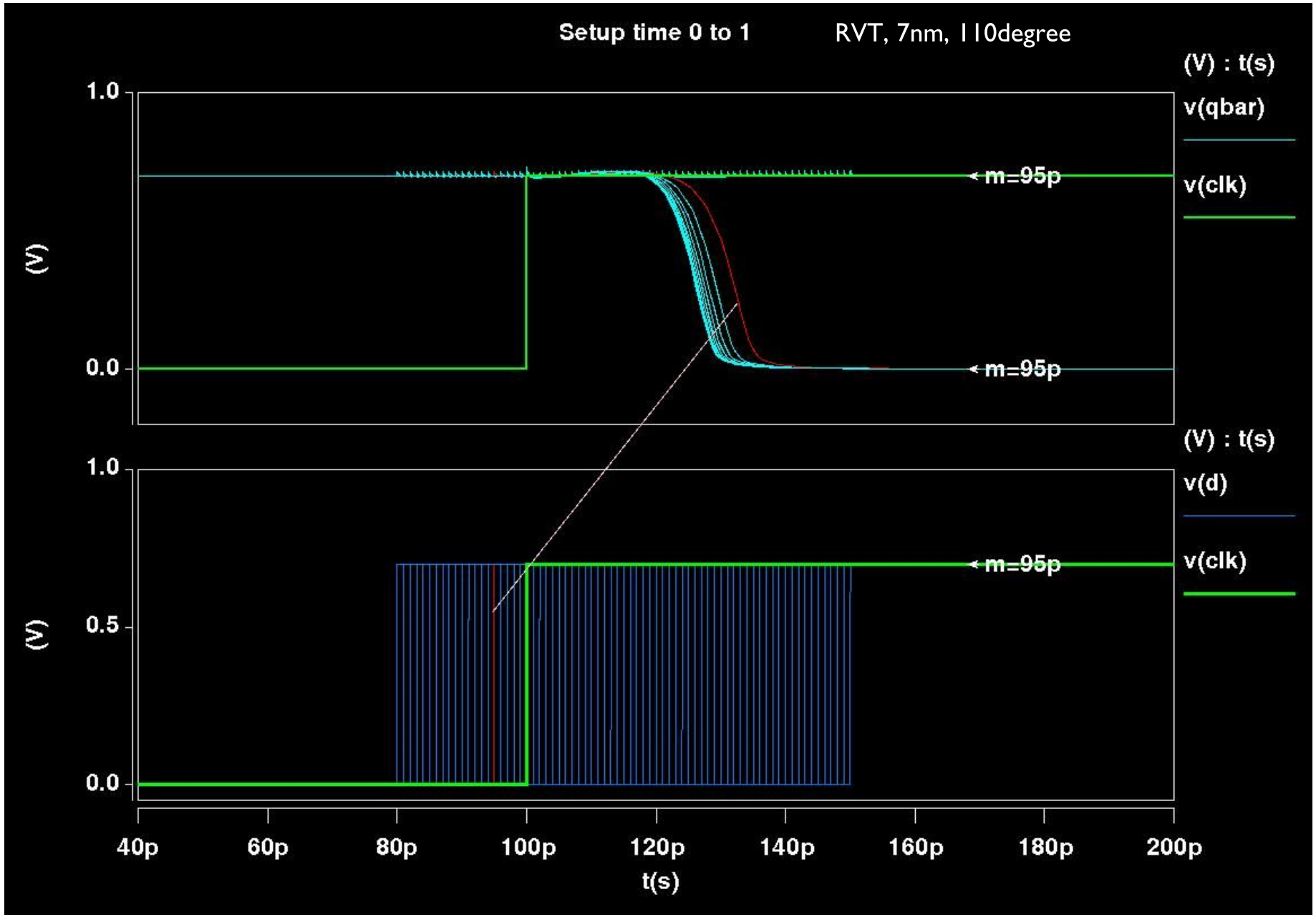


Setup time 0 to 1

The figure on the right shows the transition from 0 to 1 for a flip flop

It can be seen that if the input arrives after 95ps then the transition is not captured.

Therefore setup time is approx 100(clock edge) - 95ps =5ps

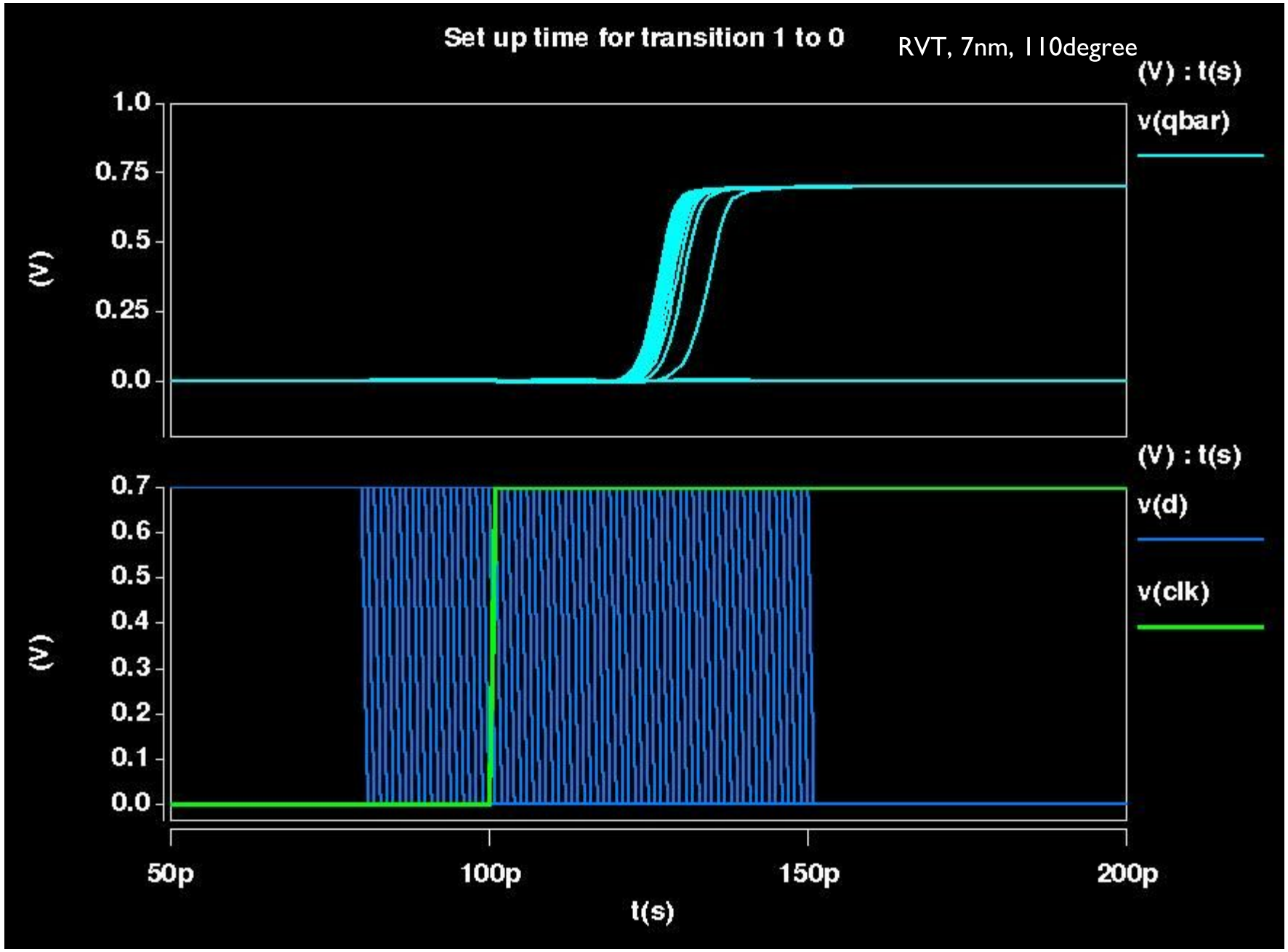


Setup 1 to 0

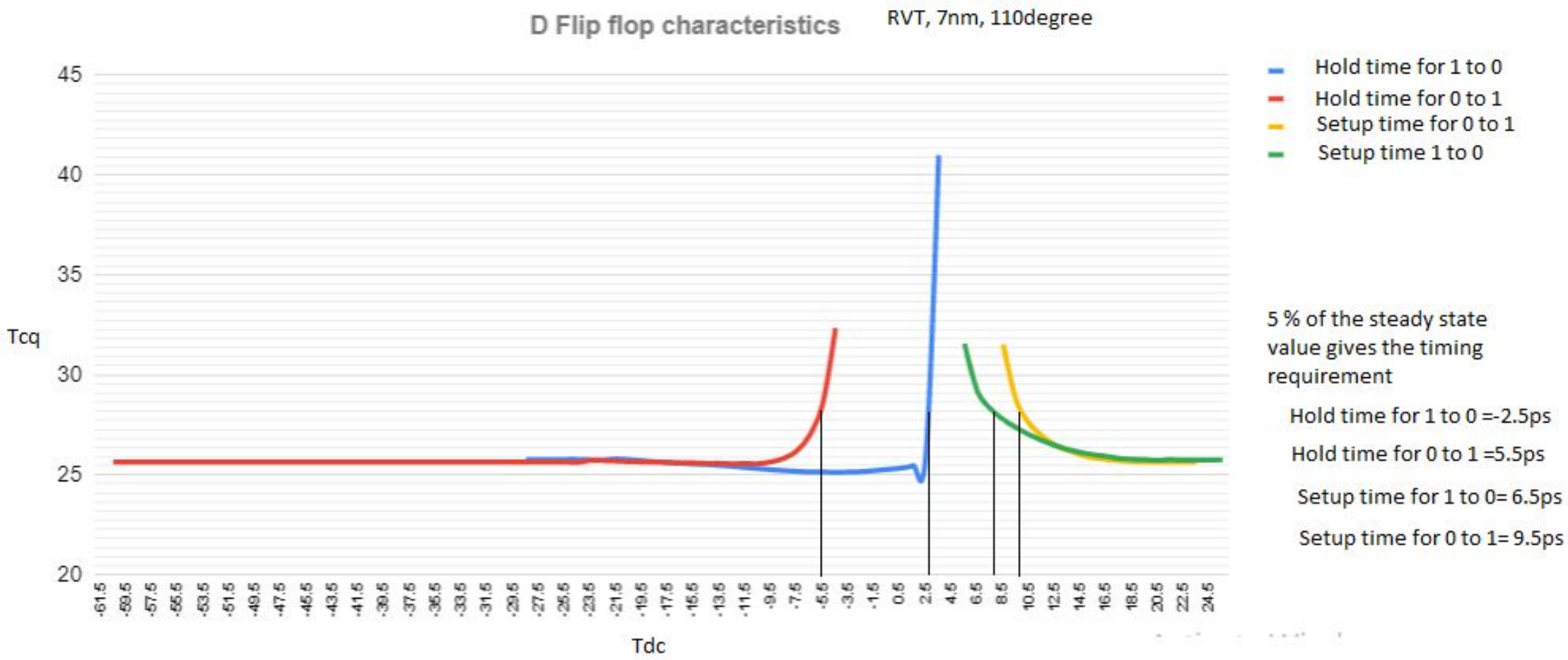
The figure on the right shows the transition from 1 to 0 for a flip flop

It can be seen that if the input arrives after a certain point then the transition cant be captured.

Therefore the input should arrive before the setup time



Tdc vs Tcq



5 % of the steady state value gives the timing requirement

Hold time for 1 to 0 =-2.5ps

Hold time for 0 to 1 =5.5ps

Setup time for 1 to 0= 6.5ps

Setup time for 0 to 1= 9.5ps

5% of the steady state values can be the allowed values

The worst case setup time measured is 9.5ps

The worst case hold time measured is 5.5ps

The data should be arriving at the flip flop at these intervals before the clock edge

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Question 3)

a) flip flop $T_c \geq t_{cq} + t_{pd} + t_{setup} + t_{skew}$

maximum propagation delay

$t_{pd} = T_c - t_{cq} - t_{setup} - t_{skew}$

$= 200 - 5 - 10 - 10$

$t_{pd} = 175\,ps$

b) two phased transparent latch

$t_c = 2t_{dq} + t_{pd1} + t_{pd2}$

$t_{pd} = t_{pd1} + t_{pd2} = t_c - 2t_{dq}$

$= 200 - 10 = 190\,ps$

$t_{pd} = 190\,ps$

Question 4)

a) flip flop $t_{cq} + t_{pd} > t_{skew} + t_{hold}$

$t_{pd} > t_{hold} + t_{skew} - t_{cq}$

$t_{pd} > 5 + 10 - 5$

$t_{pd} \geq 10\,ps$

$\Rightarrow$ min prog delay = 10ps

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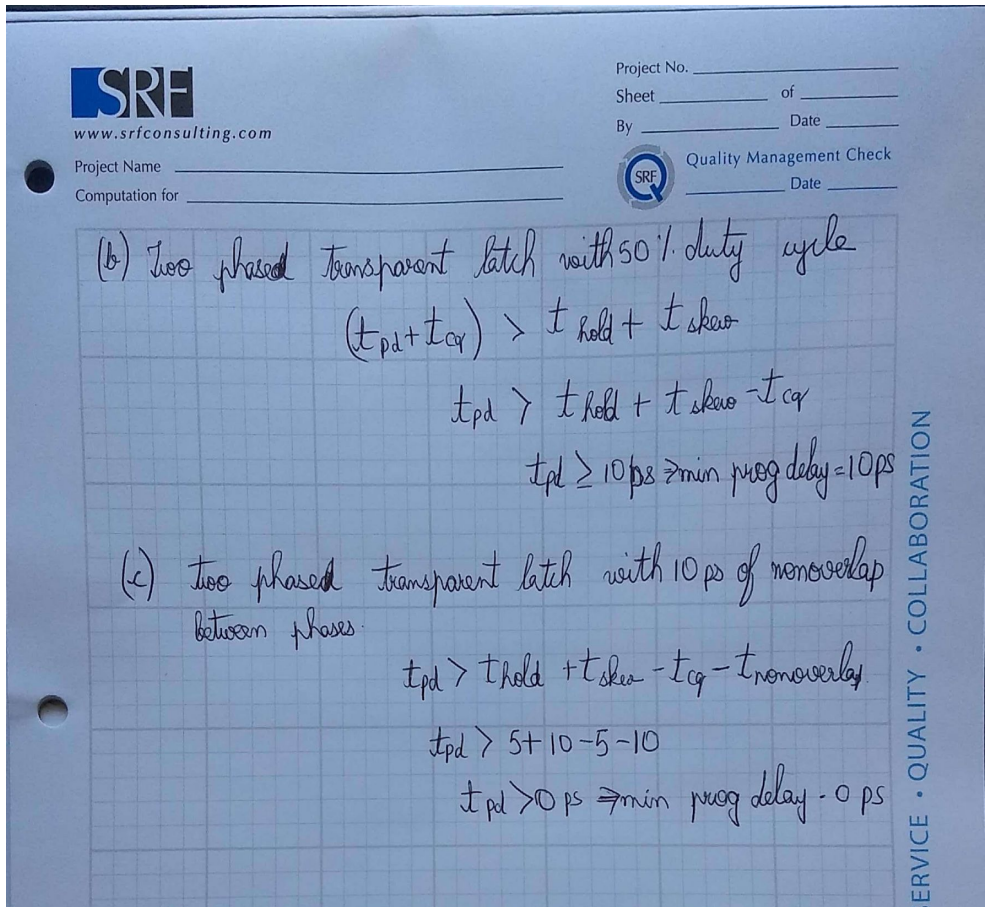

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(b) Two phased transparent latch with 50% duty cycle

$(t_{pd} + t_{cq}) > t_{hold} + t_{skew}$

$t_{pd} > t_{hold} + t_{skew} - t_{cq}$

$t_{pd} \geq 10\,ps \Rightarrow$ min prog delay = 10 ps

(c) Two phased transparent latch with 10 ps of nonoverlap between phases.

$t_{pd} > t_{hold} + t_{skew} - t_{cq} - t_{nonoverlap}$

$t_{pd} > 5 + 10 - 5 - 10$

$t_{pd} > 0\,ps \Rightarrow$ min prog delay - 0 ps

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