MPCA Lab Week 9

SEM 4 D1

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Task 1

Without Forwarding

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

FP_Add F1 F1 F1 Insert Instruction

Data Forwarding Remove Instruction

Help Reset Application

	Instruction	CPU Cycles 1	2	3	4	5	6	7	8	9	10	11	12
0	int_add (R1, R2, R3)	IF	ID	+|- (i)	MEM	WB							
1	int_sub (R4, R1, R5)		IF	ID	S	S	+|- (i)	MEM	WB				
2	fp_ld (F1, Offset, R1)			IF	S	S	ID	EX	MEM	WB			
3	fp_add (F5, F1, F1)						IF	ID	S	S	+|- (f)	MEM	WB

Step Execute All Instructions

Potential Hazards:

```
RAW: Instructions 0 and 1.  Register R1.
RAW: Instructions 0 and 2.  Register R1.
RAW: Instructions 2 and 3.  Register F1.
```

With Forwarding

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

FP_Add F1 F1 F1 Insert Instruction

Data Forwarding Remove Instruction

Help Reset Application

	Instruction	CPU Cycles 1	2	3	4	5	6	7	8	9	10	11	12
0	int_add (R1, R2, R3)	IF	ID	+|- (i)	MEM	WB							
1	int_sub (R4, R1, R5)		IF	ID	+|- (i)	MEM	WB						
2	fp_ld (F1, Offset, R1)			IF	ID	EX	MEM	WB					
3	fp_add (F5, F1, F1)				IF	ID	S	+|- (f)	MEM	WB			

Step Execute All Instructions

Potential Hazards:

```
RAW: Instructions 2 and 3.  Register F1.
```

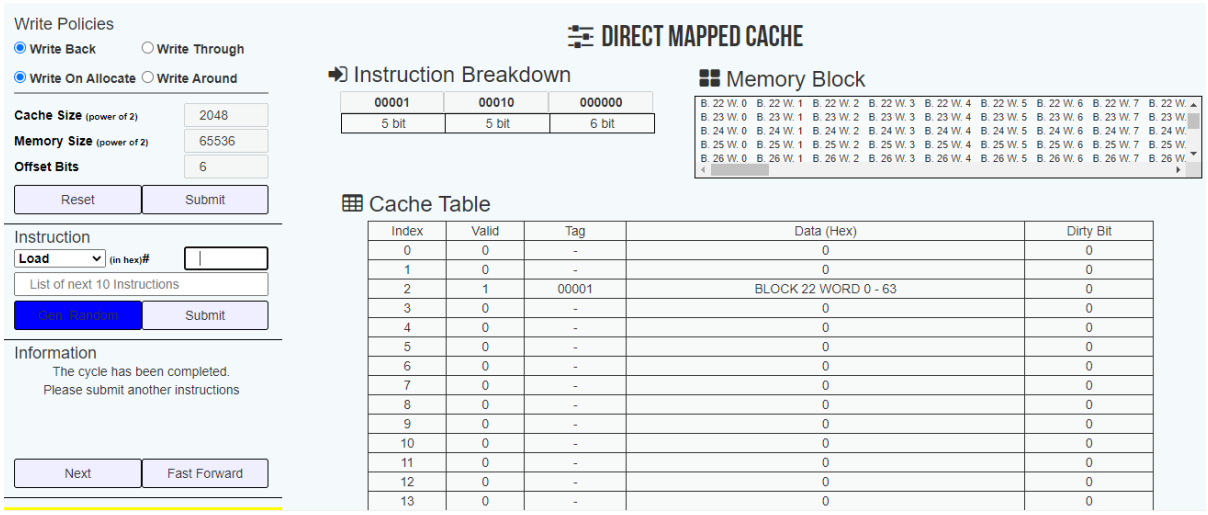
RAW Data dependency is present.

1>6 stall states have been introduced.

2>Stall cycles are reduced by 5 as with data forwarding only 1 stall is present.

3>Clock Cycles without forwarding:12 and with forwarding :9

Task 2



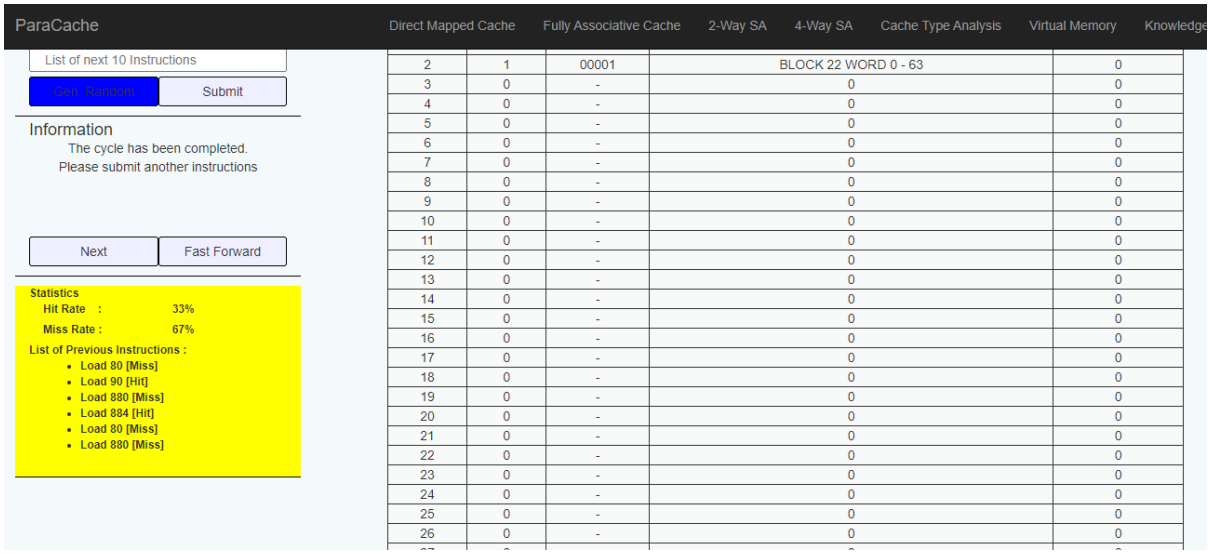
1>

a>No of bits for tag=5(65536/2048=32=2^5)

No of bits for word=6(64=2^6)

No of bits for block=5(2048/64=32=2^5)

b>



Hit Rate : 33%

Miss Rate: 67%

Dec(Hex) – Hit Or Miss

128(80)-Miss

144(90)-Hit

2176(880)-Miss

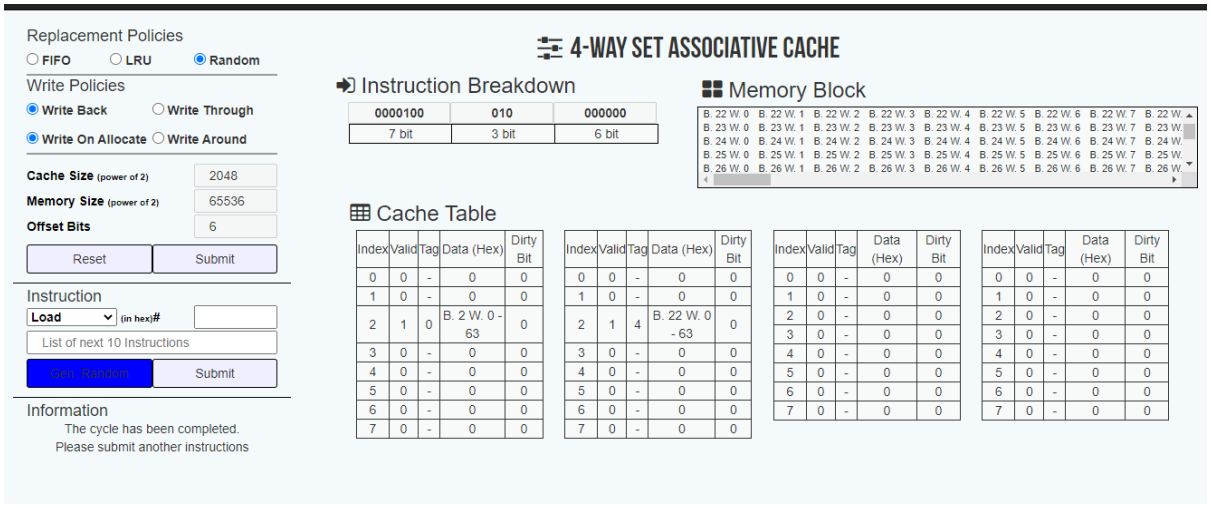
2180(884)-Hit

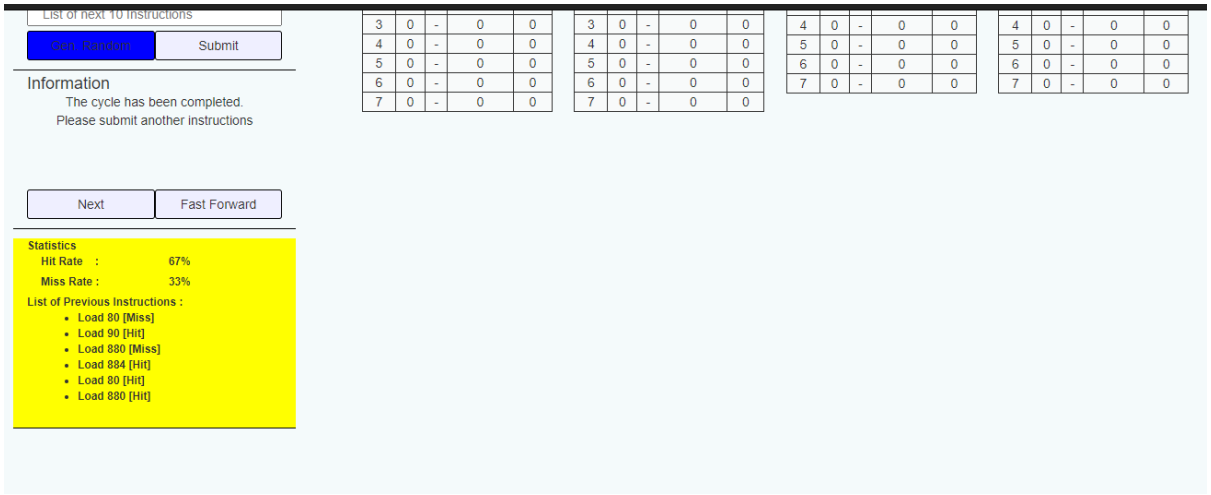
128(80)-Miss

2176(880)-Miss

2>

a> 4 Way Set Associative





Hit Rate:67%

Miss Rate:33%

Dec(Hex) – Hit Or Miss

128(80)-Miss

144(90)-Hit

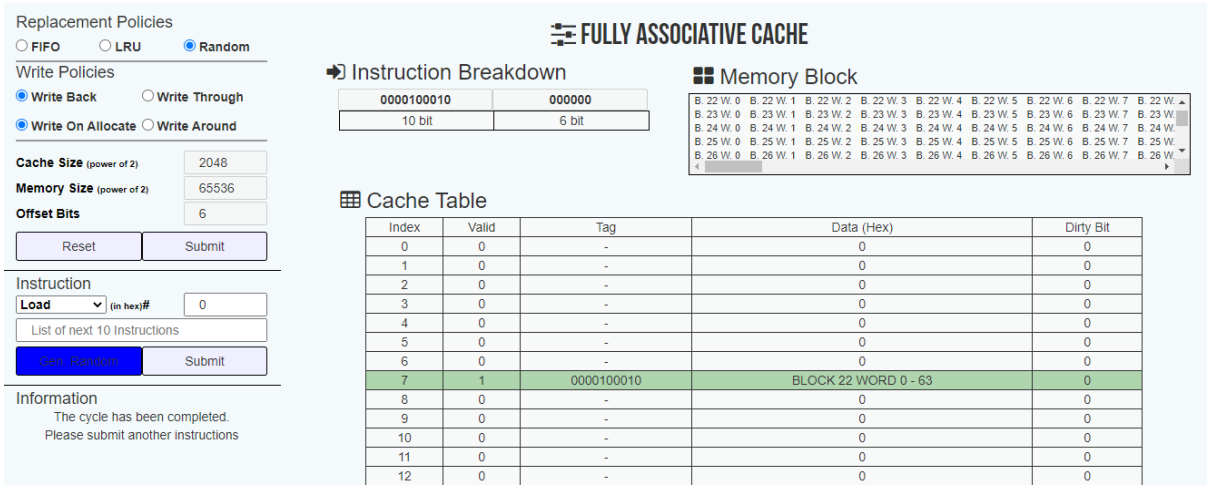
2176(880)-Miss

2180(884)-Hit

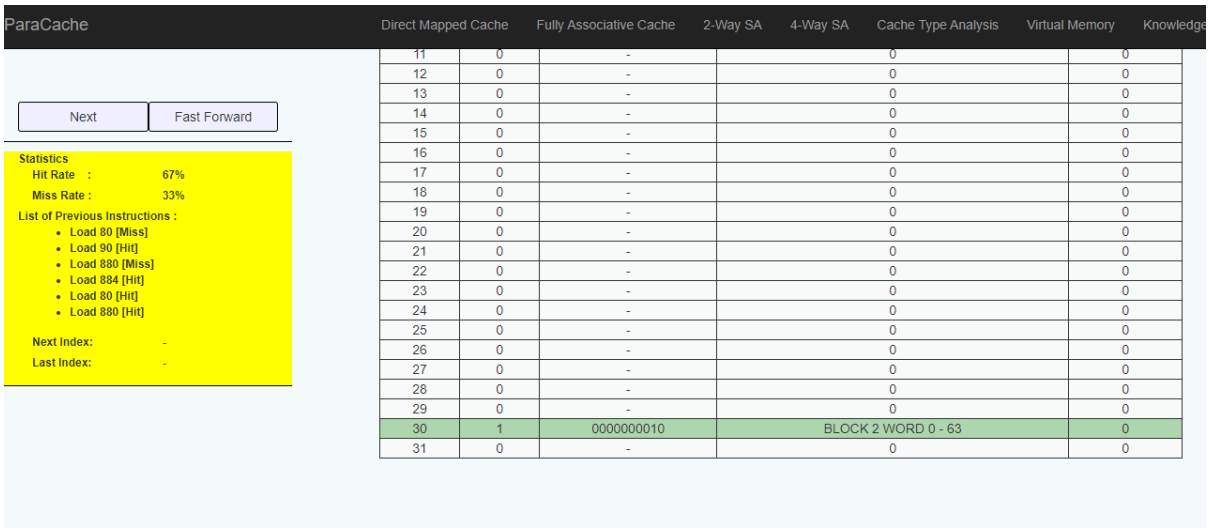
128(80)-Hit

2176(880)-Hit

b>Fully Associative



Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	1	0000100010	BLOCK 22 WORD 0 - 63	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0



11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	1	0000000010	BLOCK 2 WORD 0 - 63	0
31	0	-	0	0

Hit Rate:67%

Miss Rate:33%

Dec(Hex) – Hit Or Miss

128(80)-Miss

144(90)-Hit

2176(880)-Miss

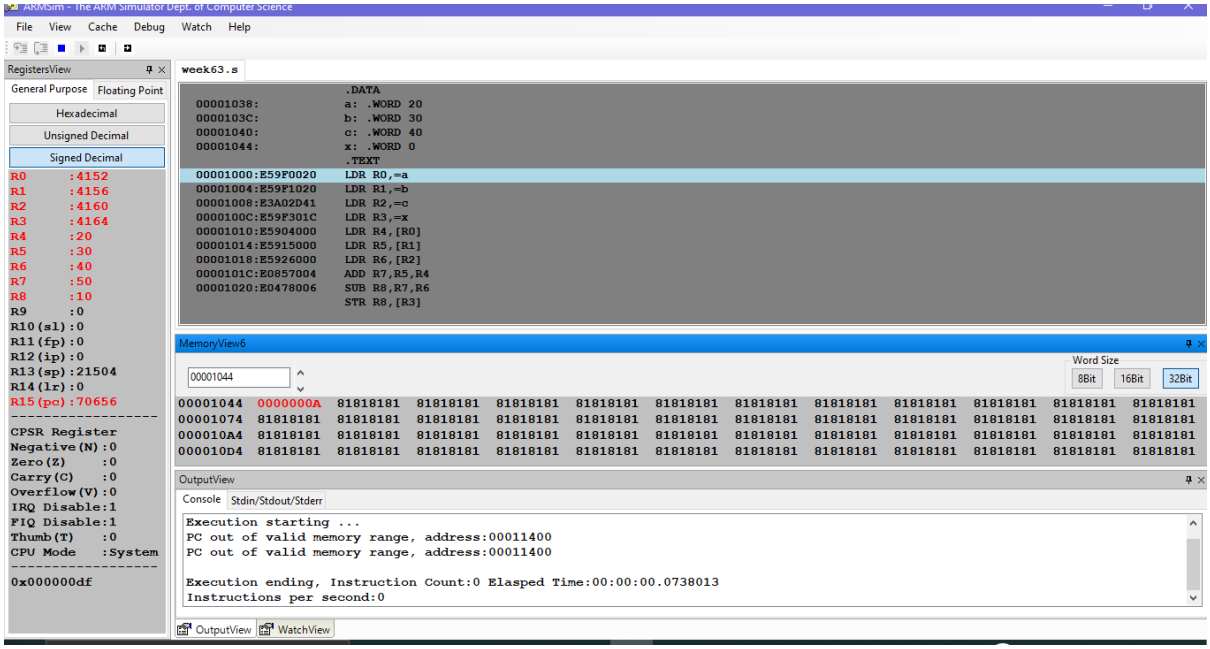
2180(884)-Hit

128(80)-Hit

2176(880)-Hit

Task 3(ARM SIM)

1>



Code

.DATA

a: .WORD 20

b: .WORD 30

c: .WORD 40

x: .WORD 0

.TEXT

LDR R0,=a

LDR R1,=b

LDR R2,=c

LDR R3,=x

LDR R4,[R0]

LDR R5,[R1]

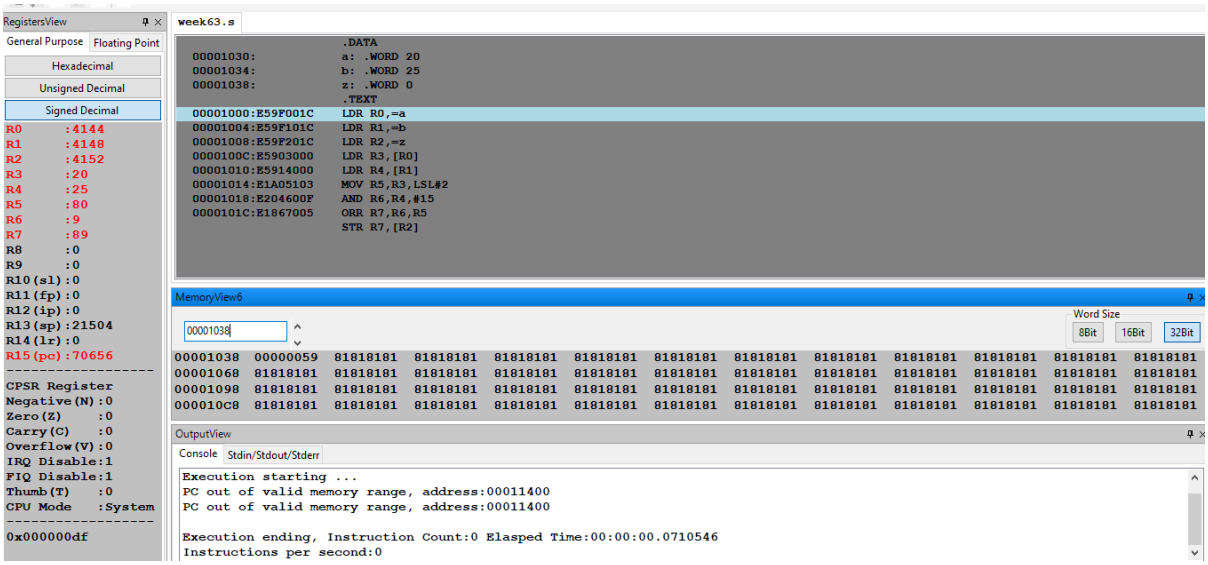
LDR R6,[R2]

ADD R7,R5,R4

SUB R8,R7,R6

STR R8,[R3]

2>



Code:

.DATA

a: .WORD 20

b: .WORD 25

z: .WORD 0

.TEXT

LDR R0,=a

LDR R1,=b

LDR R2,=z

LDR R3,[R0]

LDR R4,[R1]

MOV R5,R3,LSL#2

AND R6,R4,#15

ORR R7,R6,R5

STR R7,[R2]

Reason:

A=20 B=25 => A<<2=80 => B&15=9=>A|B=(80|9)=89=59(HEX)