

## MPCA Lab Week 9

### SEM 4 D1

Name: Kartik Soni

USN:PES1UG19CS212

### Task 1

#### Without Forwarding

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

FP\_Add ▾ F1 ▾ F1 ▾ F1 ▾ Insert Instruction  
☐ Data Forwarding Remove Instruction

Instruction	CPU Cycles											
	1	2	3	4	5	6	7	8	9	10	11	12
0 int_add (R1, R2, R3)	IF	ID	+- (I)	MEM	WB							
1 int_sub (R4, R1, R5)		IF	ID	S	S	+- (I)	MEM	WB				
2 fp_ld (F1, Offset, R1)			IF	S	S	ID	EX	MEM	WB			
3 fp_add (F5, F1, F1)						IF	ID	S	S	+- (f)	MEM	WB

Step

#### Potential Hazards:

RAW: Instructions 0 and 1. Register R1.  
 RAW: Instructions 0 and 2. Register R1.  
 RAW: Instructions 2 and 3. Register F1.

#### With Forwarding

Instruction	Execution Cycles
FP_Add/Sub	1
FP_Multiply	1
FP_Divide	1
INT_Divide	1

FP\_Add ▾ F1 ▾ F1 ▾ F1 ▾ Insert Instruction  
☒ Data Forwarding

Instruction	CPU Cycles											
	1	2	3	4	5	6	7	8	9	10	11	12
0 int_add (R1, R2, R3)	IF	ID	+- (I)	MEM	WB							
1 int_sub (R4, R1, R5)		IF	ID	+- (I)	MEM	WB						
2 fp_ld (F1, Offset, R1)			IF	ID	EX	MEM	WB					
3 fp_add (F5, F1, F1)				IF	ID	S	+- (f)	MEM	WB			

Step

#### Potential Hazards:

RAW: Instructions 2 and 3. Register F1.

RAW Data dependency is present.

1>6 stall states have been introduced.

2>Stall cycles are reduced by 5 as with data forwarding only 1 stall is present.

3>Clock Cycles without forwarding:12 and with forwarding :9

## Task 2

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

**DIRECT MAPPED CACHE**

➔ Instruction Breakdown

00001	00010	000000
5 bit	5 bit	6 bit

☒ Memory Block

B. 22 W. 0	B. 22 W. 1	B. 22 W. 2	B. 22 W. 3	B. 22 W. 4	B. 22 W. 5	B. 22 W. 6	B. 22 W. 7	B. 22 W. 8
B. 23 W. 0	B. 23 W. 1	B. 23 W. 2	B. 23 W. 3	B. 23 W. 4	B. 23 W. 5	B. 23 W. 6	B. 23 W. 7	B. 23 W. 8
B. 24 W. 0	B. 24 W. 1	B. 24 W. 2	B. 24 W. 3	B. 24 W. 4	B. 24 W. 5	B. 24 W. 6	B. 24 W. 7	B. 24 W. 8
B. 25 W. 0	B. 25 W. 1	B. 25 W. 2	B. 25 W. 3	B. 25 W. 4	B. 25 W. 5	B. 25 W. 6	B. 25 W. 7	B. 25 W. 8
B. 26 W. 0	B. 26 W. 1	B. 26 W. 2	B. 26 W. 3	B. 26 W. 4	B. 26 W. 5	B. 26 W. 6	B. 26 W. 7	B. 26 W. 8

☒ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	00001	BLOCK 22 WORD 0 - 63	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0

Instruction

Load

List of next 10 Instructions

Information

The cycle has been completed.  
Please submit another instructions

1>

a>No of bits for tag= $5(65536/2048=32=2^5)$

No of bits for word= $6(64=2^6)$

No of bits for block= $5(2048/64=32=2^5)$

b>

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge

List of next 10 Instructions

Information

The cycle has been completed.  
Please submit another instructions

Statistics

Hit Rate : 33%

Miss Rate : 67%

List of Previous Instructions :

- Load 80 [Miss]
- Load 90 [Hit]
- Load 880 [Miss]
- Load 884 [Hit]
- Load 80 [Miss]
- Load 880 [Miss]

2	1	00001	BLOCK 22 WORD 0 - 63	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0

Hit Rate : 33%

Miss Rate: 67%

Dec(Hex) – Hit Or Miss

128(80)-Miss

144(90)-Hit

2176(880)-Miss

2180(884)-Hit

128(80)-Miss

2176(880)-Miss

2>

a> 4 Way Set Associative

Replacement Policies

☐ FIFO ☐ LRU ☒ Random

Write Policies

☒ Write Back ☐ Write Through

☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

2048

Memory Size (power of 2)

65536

Offset Bits

6

Reset

Submit

Instruction

Load

(in hex#)

List of next 10 Instructions

Gen Random

Submit

Information

The cycle has been completed.  
Please submit another instructions

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

0000100	010	000000
7 bit	3 bit	6 bit

Memory Block

B. 22 W. 0	B. 22 W. 1	B. 22 W. 2	B. 22 W. 3	B. 22 W. 4	B. 22 W. 5	B. 22 W. 6	B. 22 W. 7	B. 22 W. 8
B. 23 W. 0	B. 23 W. 1	B. 23 W. 2	B. 23 W. 3	B. 23 W. 4	B. 23 W. 5	B. 23 W. 6	B. 23 W. 7	B. 23 W. 8
B. 24 W. 0	B. 24 W. 1	B. 24 W. 2	B. 24 W. 3	B. 24 W. 4	B. 24 W. 5	B. 24 W. 6	B. 24 W. 7	B. 24 W. 8
B. 25 W. 0	B. 25 W. 1	B. 25 W. 2	B. 25 W. 3	B. 25 W. 4	B. 25 W. 5	B. 25 W. 6	B. 25 W. 7	B. 25 W. 8
B. 26 W. 0	B. 26 W. 1	B. 26 W. 2	B. 26 W. 3	B. 26 W. 4	B. 26 W. 5	B. 26 W. 6	B. 26 W. 7	B. 26 W. 8

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	0	B. 2 W. 0 - 63	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	4	B. 22 W. 0 - 63	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0

List of next 10 Instructions

Gen Random

Submit

Information

The cycle has been completed.  
Please submit another instructions

Next

Fast Forward

Statistics

Hit Rate : 67%

Miss Rate : 33%

List of Previous Instructions :

- Load 80 [Miss]
- Load 90 [Hit]
- Load 880 [Miss]
- Load 884 [Hit]
- Load 80 [Hit]
- Load 880 [Hit]

Hit Rate:67%

Miss Rate:33%

Dec(Hex) – Hit Or Miss

128(80)-Miss

144(90)-Hit

2176(880)-Miss

2176(880)-Hit

### Replacement Policies

☐ FIFO
 ☐ LRU
 ☒ Random

### Write Policies

☒ Write Back
 ☐ Write Through

☒ Write On Allocate
 ☐ Write Around

**Cache Size** (power of 2)

**Memory Size** (power of 2)

**Offset Bits**

### Instruction

**Load**  (in hex)

### Information

The cycle has been completed.  
Please submit another instructions

## FULLY ASSOCIATIVE CACHE

### Instruction Breakdown

0000100010	0000000
10 bit	6 bit

### Memory Block

B. 22	W. 0	B. 22	W. 1	B. 22	W. 2	B. 22	W. 3	B. 22	W. 4	B. 22	W. 5	B. 22	W. 6	B. 22	W. 7	B. 22	W. 8
B. 23	W. 0	B. 23	W. 1	B. 23	W. 2	B. 23	W. 3	B. 23	W. 4	B. 23	W. 5	B. 23	W. 6	B. 23	W. 7	B. 23	W. 8
B. 24	W. 0	B. 24	W. 1	B. 24	W. 2	B. 24	W. 3	B. 24	W. 4	B. 24	W. 5	B. 24	W. 6	B. 24	W. 7	B. 24	W. 8
B. 25	W. 0	B. 25	W. 1	B. 25	W. 2	B. 25	W. 3	B. 25	W. 4	B. 25	W. 5	B. 25	W. 6	B. 25	W. 7	B. 25	W. 8
B. 26	W. 0	B. 26	W. 1	B. 26	W. 2	B. 26	W. 3	B. 26	W. 4	B. 26	W. 5	B. 26	W. 6	B. 26	W. 7	B. 26	W. 8

### Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	1	0000100010	BLOCK 22 WORD 0 - 63	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0

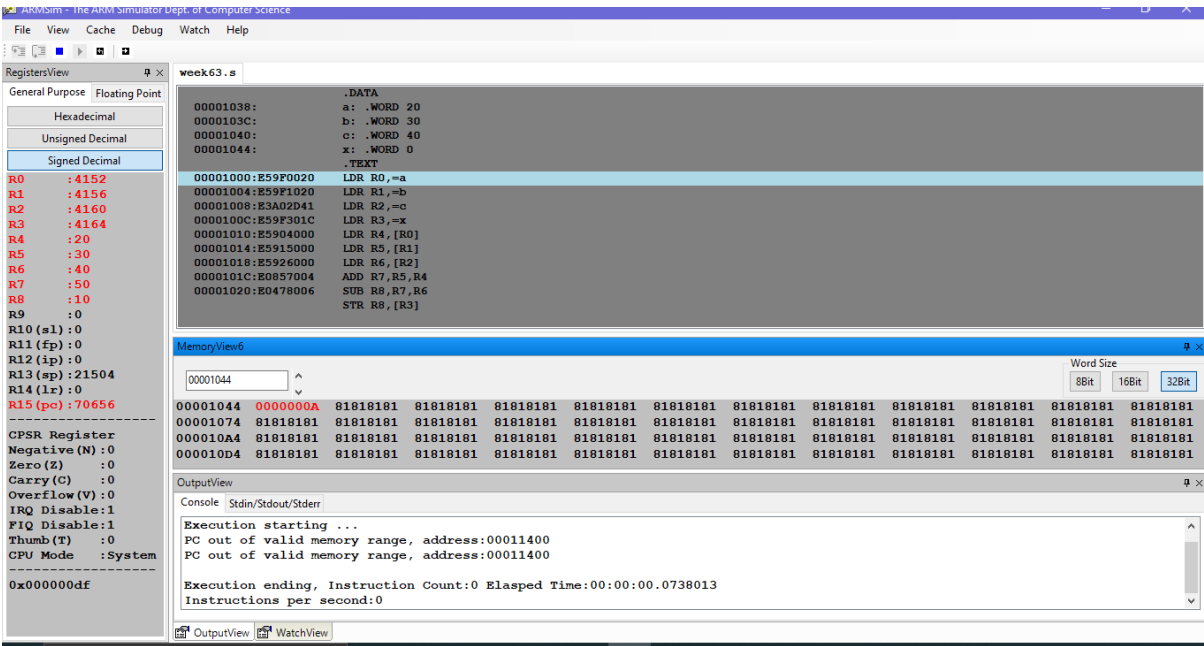
ParaCache	Direct Mapped Cache	Fully Associative Cache	2-Way SA	4-Way SA	Cache Type Analysis	Virtual Memory	Knowledge
	11	0	-		0		0
	12	0	-		0		0
	13	0	-		0		0
	14	0	-		0		0
	15	0	-		0		0
	16	0	-		0		0
	17	0	-		0		0
	18	0	-		0		0
	19	0	-		0		0
	20	0	-		0		0
	21	0	-		0		0
	22	0	-		0		0
	23	0	-		0		0
	24	0	-		0		0
	25	0	-		0		0
	26	0	-		0		0
	27	0	-		0		0
	28	0	-		0		0
	29	0	-		0		0
	30	1	0000000010		BLOCK 2 WORD 0 - 63		0
	31	0	-		0		0

128(80)-Hit

2176(880)-Hit

Task 3(ARM SIM)

1>



Code

.DATA

a: .WORD 20

b: .WORD 30

c: .WORD 40

x: .WORD 0

.TEXT

LDR R0,=a

LDR R1,=b

LDR R2,=c

LDR R3,=x

LDR R4,[R0]

LDR R5,[R1]

LDR R6,[R2]

ADD R7,R5,R4

SUB R8,R7,R6

STR R8,[R3]

2>

The screenshot shows a debugger interface with three main panes. The top pane, 'RegistersView', displays the state of 16 registers (R0-R15) and CPSR. R0-R14 are in 'Signed Decimal' mode, and R15 is in 'Floating Point' mode. R0 is 4144, R1 is 4148, R2 is 4152, R3 is 20, R4 is 25, R5 is 80, R6 is 9, R7 is 89, R8 is 0, R9 is 0, R10 is 0, R11 is 0, R12 is 0, R13 is 21504, R14 is 0, and R15 is 70656. The middle pane, 'MemoryView6', shows a memory dump starting at address 00001038. The bottom pane, 'OutputView', shows the execution log. The log indicates that execution started at address 00011400, ended at address 00011400, and that the instruction count was 0 and the elapsed time was 00:00:00.0710546 seconds.

Register	Value
R0	4144
R1	4148
R2	4152
R3	20
R4	25
R5	80
R6	9
R7	89
R8	0
R9	0
R10	0
R11	0
R12	0
R13	21504
R14	0
R15	70656

MemoryView6: 00001038 00000059 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

OutputView: Execution starting ...  
PC out of valid memory range, address:00011400  
PC out of valid memory range, address:00011400  
Execution ending, Instruction Count:0 Elapsed Time:00:00:00.0710546  
Instructions per second:0

Code:

.DATA

a: .WORD 20

b: .WORD 25

z: .WORD 0

.TEXT

LDR R0,=a

LDR R1,=b

LDR R2,=z

LDR R3,[R0]

LDR R4,[R1]

MOV R5,R3,LSL#2

AND R6,R4,#15

ORR R7,R6,R5

STR R7,[R2]

Reason:

$A=20$   $B=25 \Rightarrow A < 2=80 \Rightarrow B \& 15=9 \Rightarrow A | B=(80 | 9)=89=59$  (HEX)