

Microprocessor and Computer Architecture Laboratory

UE19CS256

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Week# ____4____ Program Number: ____1____

Write an ALP to add corresponding elements of an array.

I.ARM Assembly Code

.data

a: .word 10, 20, 30, 40, 50

b: .word 10, 20, 30, 40, 50

c: .word 0,0,0,0,0

.text

LDR r0,=a

LDR r1,=b

LDR r2,=c

mov r3,#1

loop:

ldr r4,[r0],#4

ldr r5,[r1],#4

add r6,r4,r5

str r6,[r2],#4

add r3,r3,#1

cmp r3,#5

ble loop

swi 0x011

II.Output

The screenshot displays a debugger interface with two main panels. The top panel, titled 'RegistersView', shows the state of various registers. The bottom panel, titled 'MemoryView3', shows a memory dump starting at address 00001064. The assembly code in the top panel includes instructions for loading, adding, storing, comparing, and branching, followed by a software interrupt instruction.

RegistersView

Register	Value
R0	:00001050
R1	:00001064
R2	:00001078
R3	:00000006
R4	:00000032
R5	:00000032
R6	:00000064
R7	:00000000
R8	:00000000
R9	:00000000
R10 (s1)	:00000000
R11 (fp)	:00000000
R12 (ip)	:00000000
R13 (sp)	:00000000
R14 (lr)	:00001030
R15 (pc)	:00000008

CPSR Register

Negative (N)	:0
Zero (Z)	:0
Carry (C)	:1
Overflow (V)	:0
IRQ Disable	:1
FIQ Disable	:1
Thumb (T)	:0
CPU Mode	:Supervisor

MemoryView3

Address	Value
00001064	00000014
00001068	00000028
0000106C	0000003C
00001070	00000050
00001074	00000064
00001078	81818181
0000107C	81818181
00001080	81818181
00001084	81818181
00001088	81818181
0000108C	81818181
00001090	81818181
00001094	81818181
00001098	81818181
0000109C	81818181
000010A0	81818181
000010A4	81818181
000010A8	81818181
000010AC	81818181
000010B0	81818181
000010B4	81818181
000010B8	81818181
000010BC	81818181
000010C0	81818181
000010C4	81818181
000010C8	81818181
000010CC	81818181
000010D0	81818181
000010D4	81818181
000010D8	81818181
000010DC	81818181
000010E0	81818181
000010E4	81818181
000010E8	81818181
000010EC	81818181
000010F0	81818181
000010F4	81818181
000010F8	81818181
000010FC	81818181
00001100	81818181
00001104	81818181
00001108	81818181
0000110C	81818181
00001110	81818181
00001114	81818181
00001118	81818181
0000111C	81818181
00001120	81818181
00001124	81818181
00001128	81818181
0000112C	81818181
00001130	81818181
00001134	81818181
00001138	81818181
0000113C	81818181
00001140	81818181
00001144	81818181
00001148	81818181
0000114C	81818181
00001150	81818181
00001154	81818181
00001158	81818181
0000115C	81818181
00001160	81818181
00001164	81818181
00001168	81818181
0000116C	81818181
00001170	81818181
00001174	81818181
00001178	81818181
0000117C	81818181
00001180	81818181
00001184	81818181
00001188	81818181
0000118C	81818181
00001190	81818181
00001194	81818181
00001198	81818181
0000119C	81818181
000011A0	81818181
000011A4	81818181
000011A8	81818181
000011AC	81818181
000011B0	81818181
000011B4	81818181
000011B8	81818181
000011BC	81818181
000011C0	81818181
000011C4	81818181
000011C8	81818181
000011CC	81818181
000011D0	81818181
000011D4	81818181
000011D8	81818181
000011DC	81818181
000011E0	81818181
000011E4	81818181
000011E8	81818181
000011EC	81818181
000011F0	81818181
000011F4	81818181
000011F8	81818181
000011FC	81818181
00001200	81818181
00001204	81818181
00001208	81818181
0000120C	81818181
00001210	81818181
00001214	81818181
00001218	81818181
0000121C	81818181
00001220	81818181
00001224	81818181
00001228	81818181
0000122C	81818181
00001230	81818181
00001234	81818181
00001238	81818181
0000123C	81818181
00001240	81818181
00001244	81818181
00001248	81818181
0000124C	81818181
00001250	81818181
00001254	81818181
00001258	81818181
0000125C	81818181
00001260	81818181
00001264	81818181
00001268	81818181
0000126C	81818181
00001270	81818181
00001274	81818181
00001278	81818181
0000127C	81818181
00001280	81818181
00001284	81818181
00001288	81818181
0000128C	81818181
00001290	81818181
00001294	81818181
00001298	81818181
0000129C	81818181
000012A0	81818181
000012A4	81818181
000012A8	81818181
000012AC	81818181
000012B0	81818181
000012B4	81818181
000012B8	81818181
000012BC	81818181
000012C0	81818181
000012C4	81818181
000012C8	81818181
000012CC	81818181
000012D0	81818181
000012D4	81818181
000012D8	81818181
000012DC	81818181
000012E0	81818181
000012E4	81818181
000012E8	81818181
000012EC	81818181
000012F0	81818181
000012F4	81818181
000012F8	81818181
000012FC	81818181
00001300	81818181
00001304	81818181
00001308	81818181
0000130C	81818181
00001310	81818181
00001314	81818181
00001318	81818181
0000131C	81818181
00001320	81818181
00001324	81818181
00001328	81818181
0000132C	81818181
00001330	81818181
00001334	81818181
00001338	81818181
0000133C	81818181
00001340	81818181
00001344	81818181
00001348	81818181
0000134C	81818181
00001350	81818181
00001354	81818181
00001358	81818181
0000135C	81818181
00001360	81818181
00001364	81818181
00001368	81818181
0000136C	81818181
00001370	81818181
00001374	81818181
00001378	81818181
0000137C	81818181
00001380	81818181
00001384	81818181
00001388	81818181
0000138C	81818181
00001390	81818181
00001394	81818181
00001398	81818181
0000139C	81818181
000013A0	81818181
000013A4	81818181
000013A8	81818181
000013AC	81818181
000013B0	81818181
000013B4	81818181
000013B8	81818181
000013BC	81818181
000013C0	81818181
000013C4	81818181
000013C8	81818181
000013CC	81818181
000013D0	81818181
000013D4	81818181
000013D8	81818181
000013DC	81818181
000013E0	81818181
000013E4	81818181
000013E8	81818181
000013EC	81818181
000013F0	81818181
000013F4	81818181
000013F8	81818181
000013FC	81818181
00001400	81818181
00001404	81818181
00001408	81818181
0000140C	81818181
00001410	81818181
00001414	81818181
00001418	81818181
0000141C	81818181
00001420	81818181
00001424	81818181
00001428	81818181
0000142C	81818181
00001430	81818181
00001434	81818181
00001438	81818181
0000143C	81818181
00001440	81818181
00001444	81818181
00001448	81818181
0000144C	81818181
00001450	81818181
00001454	81818181
00001458	81818181
0000145C	81818181
00001460	81818181
00001464	81818181
00001468	81818181
0000146C	81818181
00001470	81818181
00001474	81818181
00001478	81818181
0000147C	81818181
00001480	81818181
00001484	81818181
00001488	81818181
0000148C	81818181
00001490	81818181
00001494	81818181
00001498	81818181
0000149C	81818181
000014A0	81818181
000014A4	81818181
000014A8	81818181
000014AC	81818181
000014B0	81818181
000014B4	81818181
000014B8	81818181
000014BC	81818181
000014C0	81818181
000014C4	81818181
000014C8	81818181
000014CC	81818181
000014D0	81818181
000014D4	81818181
000014D8	81818181
000014DC	81818181
000014E0	81818181
000014E4	81818181
000014E8	81818181
000014EC	81818181
000014F0	81818181
000014F4	81818181
000014F8	81818181
000014FC	81818181
00001500	81818181
00001504	81818181
00001508	81818181
0000150C	81818181
00001510	81818181
00001514	81818181
00001518	81818181
0000151C	81818181
00001520	81818181
00001524	81818181
00001528	81818181
0000152C	81818181
00001530	81818181
00001534	81818181
00001538	81818181
0000153C	81818181
00001540	81818181
00001544	81818181
00001548	81818181
0000154C	81818181
00001550	81818181
00001554	81818181
00001558	81818181
0000155C	81818181
00001560	81818181
00001564	81818181
00001568	81818181
0000156C	81818181
00001570	81818181
00001574	81818181
00001578	81818181
0000157C	81818181
00001580	81818181
00001584	81818181
00001588	81818181
0000158C	81818181
00001590	81818181
00001594	81818181
00001598	81818181
0000159C	81818181
000015A0	81818181
000015A4	81818181
000015A8	81818181
000015AC	81818181
000015B0	81818181
000015B4	81818181
000015B8	81818181
000015BC	81818181
000015C0	81818181
000015C4	81818181
000015C8	81818181
000015CC	81818181
000015D0	81818181
000015D4	81818181
000015D8	81818181
000015DC	81818181
000015E0	81818181
000015E4	81818181
000015E8	81818181
000015EC	81818181
000015F0	81818181
000015F4	81818181
000015F8	81818181
000015FC	81818181
00001600	81818181
00001604	81818181
00001608	81818181
0000160C	81818181
00001610	81818181
00001614	81818181
00001618	81818181
0000161C	81818181
00001620	81818181
00001624	81818181
00001628	81818181
0000162C	81818181
00001630	81818181
00001634	81818181
00001638	81818181
0000163C	81818181
00001640	81818181
00001644	81818181
00001648	81818181

Week# ____4____ Program Number: ____2____

Write an ALP to find the product of corresponding elements of an array.

I.ARM Assembly Code

.data

a: .word 10, 20, 30, 40, 50

b: .word 10, 20, 30, 40, 50

c: .word 0,0,0,0,0

.text

LDR r0,=a

LDR r1,=b

LDR r2,=c

mov r3,#1

loop:

ldr r4,[r0],#4

ldr r5,[r1],#4

mul r6,r4,r5

str r6,[r2],#4

add r3,r3,#1

cmp r3,#5

ble loop

swi 0x011

II.Output

The screenshot displays a debugger window with three main panes. The top pane, 'RegistersView', shows the state of various registers. The middle pane, 'MemoryView3', displays a memory dump. The bottom pane, 'OutputView', shows the execution log.

RegistersView

Register	Value
R0	00001050
R1	00001064
R2	00001078
R3	00000006
R4	00000032
R5	00000032
R6	000009c4
R7	00000000
R8	00000000
R9	00000000
R10 (sl)	00000000
R11 (fp)	00000000
R12 (ip)	00000000
R13 (sp)	00000000
R14 (lr)	00001030
R15 (pc)	00000008

CPSR Register

Negative (N): 0
Zero (Z): 0
Carry (C): 1
Overflow (V): 0
IRQ Disable: 1
FIQ Disable: 1
Thumb (T): 0
CPU Mode: Supervisor

MemoryView3

Word Size: 8bit, 16bit, 32bit

Address	Value
00001064	00000064
00001090	81818181
000010BC	81818181
000010E8	81818181

OutputView

Execution ending, Instruction Count:0 Elapsed Time:00:00:00.2061470
Instructions per second:0

Week# ____4____ Program Number: ____3a____

Write an ALP to perform Convolution operation
using MUL instruction (Addition of multiplication
of respective numbers of loc A and loc B)

I.ARM Assembly Code

.data

a: .word 10, 20, 30, 40, 50

b: .word 10, 20, 30, 40, 50

c: .word 0

.text

LDR r0,=a

LDR r1,=b

LDR r2,=c

mov r3,#5

loop:

ldr r4,[r0],#4

ldr r5,[r1],#4

mul r6,r4,r5

add r7,r7,r6

subs r3,r3,#1

bne loop

str r7,[r2]

swi 0x011

II.Output

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 00001050

R1 : 00001064

R2 : 00001064

R3 : 00000000

R4 : 00000032

R5 : 00000032

R6 : 000009c4

R7 : 0000157c

R8 : 00000000

R9 : 00000000

R10 (sl) : 00000000

R11 (fp) : 00000000

R12 (ip) : 00000000

R13 (sp) : 00000000

R14 (lr) : 00001030

R15 (pc) : 00000008

CPSR Register

Negative (N) : 0

Zero (Z) : 1

Carry (C) : 1

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : Supervisor

0x600000d3

week4_3b.s

.data

0000103C: a: .word 10, 20, 30, 40, 50

00001050: b: .word 10, 20, 30, 40, 50

00001064: c: .word 0

.text

00001000:E59F0028 LDR r0,=a

00001004:E59F1028 LDR r1,=b

00001008:E59F2028 LDR r2,=c

0000100C:E3A03005 mov r3,#5

00001010: loop:

00001010:E4904004 ldr r4,[r0],#4

00001014:E4915004 ldr r5,[r1],#4

00001018:E0060594 mul r6,r4,r5

0000101C:E0877006 add r7,r7,r6

00001020:E2533001 subs r3,r3,#1

00001024:1AFFFFF9 bne loop

00001028:E5827000 str r7,[r2]

swi 0x011

MemoryView3

1064

00001064 0000157C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

00001090 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

000010BC 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

000010E8 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181

OutputView

Console Stdin/Stdout/Stderr

Execution ending, Instruction Count:0 Elapsed Time:00:00:00.2040855

Instructions per second:0

Week# ____ 4 ____ Program Number: ____ 3b ____

Write an ALP to perform Convolution using
MLA instruction (Addition of multiplication of
respective numbers of loc A and loc B).

I.ARM Assembly Code

.data

a: .word 10, 20, 30, 40, 50

b: .word 10, 20, 30, 40, 50

c: .word 0

.text

LDR r0,=a

LDR r1,=b

LDR r2,=c

mov r3,#5

loop:

ldr r4,[r0],#4

ldr r5,[r1],#4

mla r7,r4,r5,r7

subs r3,r3,#1

bne loop

str r7,[r2]

swi 0x011

II. Output

The screenshot displays the ARMsim interface with the following components:

- RegistersView:** Shows the state of 16 registers (R0-R15) and the CPSR register. R0-R15 are in hexadecimal format. CPSR shows flags: Negative (N): 0, Zero (Z): 1, Carry (C): 1, Overflow (V): 0, IRQ Disable: 1, FIQ Disable: 1, Thumb (T): 0, CPU Mode: Supervisor, and PC: 0x600000d3.
- Code View:** Displays assembly code for 'week4_3b.s'. It includes data section (a, b, c) and text section (loop, main). The main function calls 'swi 0x011'.
- MemoryView:** Shows memory contents starting at address 1060. The memory is filled with 0x81818181 values.
- OutputView:** Shows the console output: 'Execution ending, Instruction Count:0 Elapsed Time:00:00:00.2002148' and 'Instructions per second:0'.

Week# ____4____ Program Number: ____4____

Consider an 2D array. Write an ALP using ARM7TDMI-ISA, to retrieve / access any element from the array.

I.ARM Assembly Code

.data

a: .byte 1, 2, 3, 4, 5,6,7,8,9

.text

LDR r0,=a

mov r1,#0;row

mov r2,#0;col

mov r3,#3;no of elements per row

mla r4,r1,r3,r2

ldrb r5,[r0,r4]

