Layout, Extraction and Simulation Project

4-bit Ripple Carry Adder

Principles of VLSI Circuit Design
EEEN-5333
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By-
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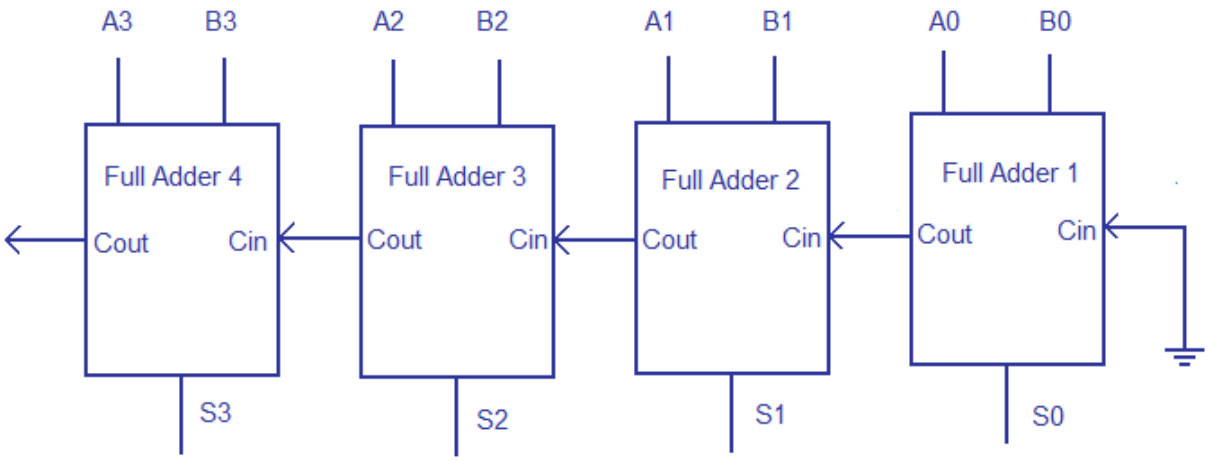
Abstract

This report consists of detailed implementation of a 4-bit Ripple Carry Adder circuit. The Magic layouts and spice simulation results are given. Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output.

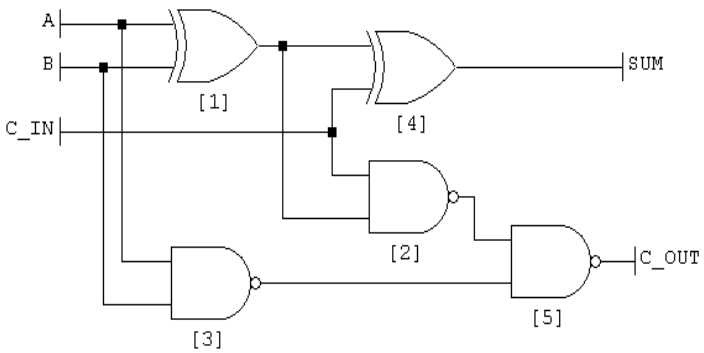
4-bit Ripple Carry Adder

A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded, with the carry output from each full adder connected to the carry input of the next full adder in the chain. The interconnection of four full adder (FA) circuits provide a 4-bit ripple carry adder.



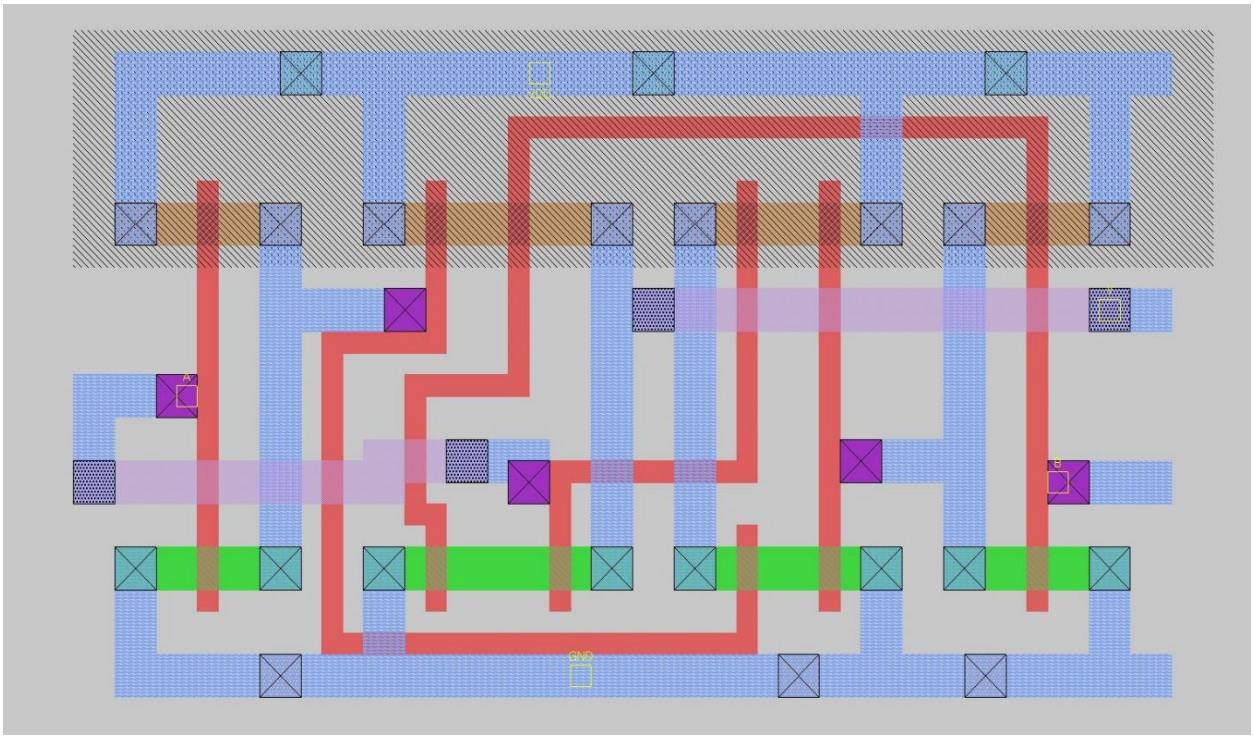
A one-bit full adder is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs (a, b and cin) two outputs. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin) bit.

Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

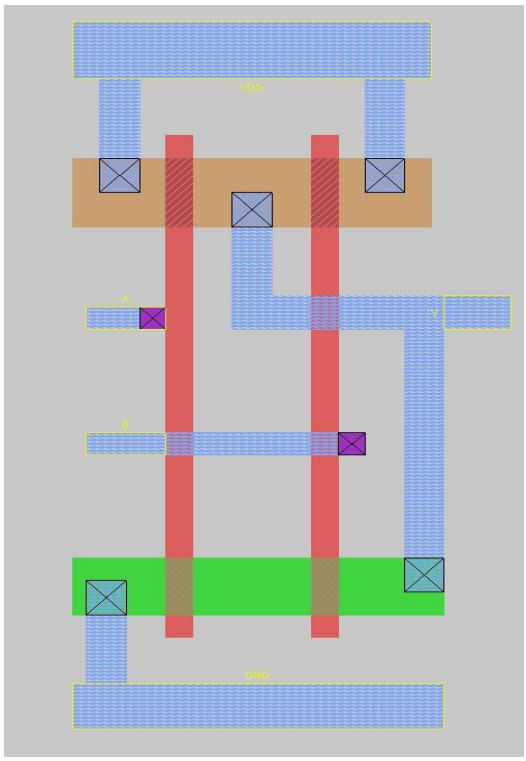


Magic layouts

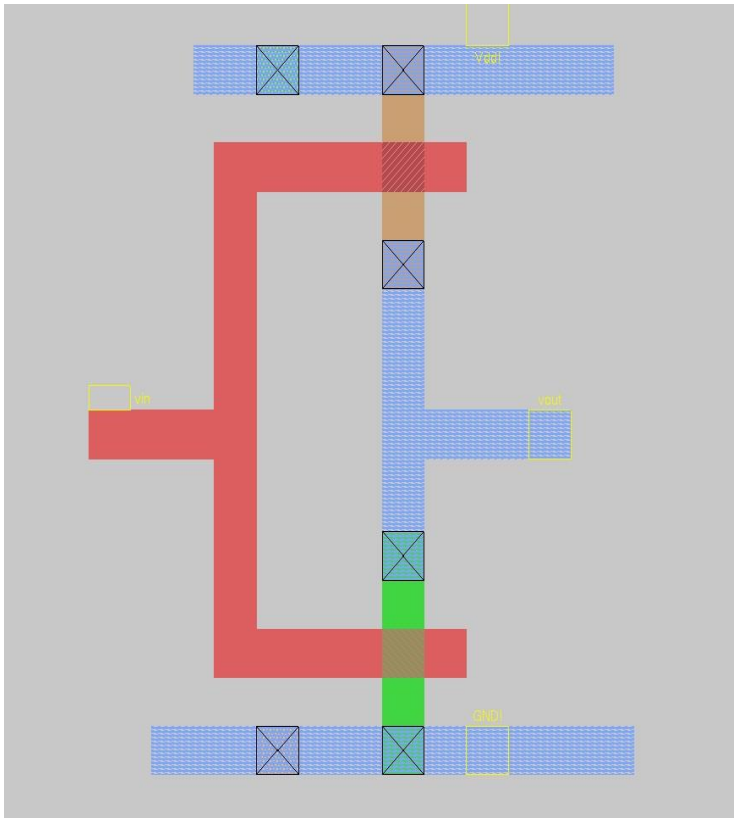
1) **2 input XOR**



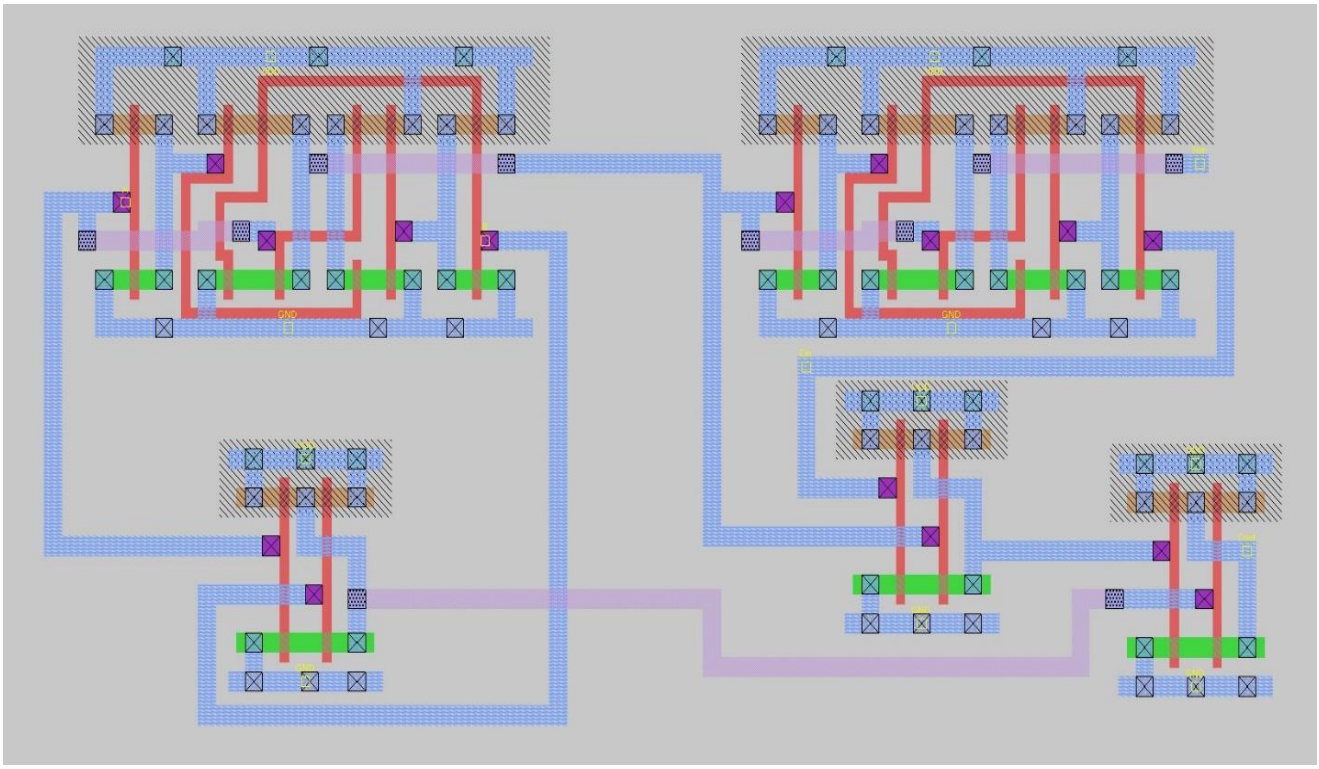
2) 2 input NAND



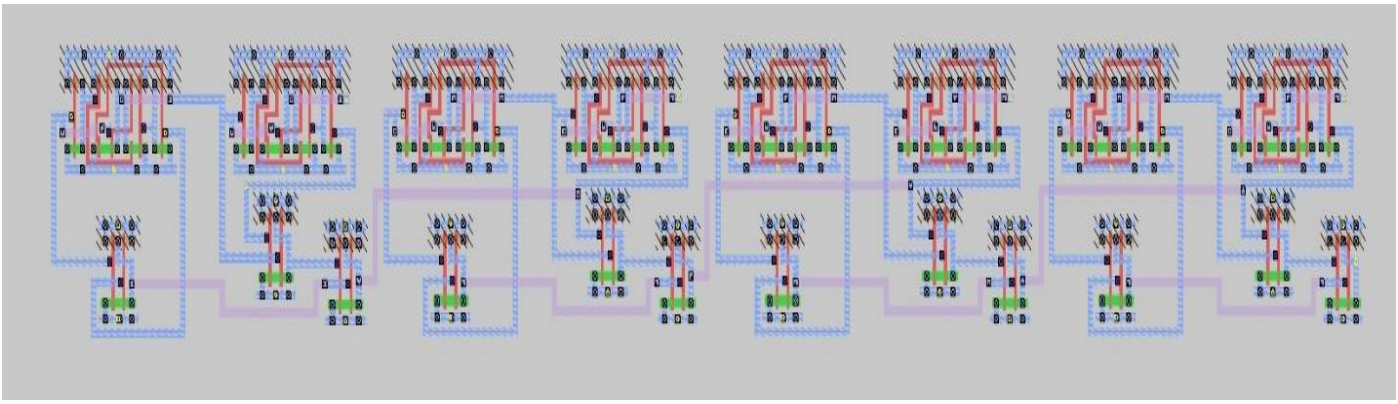
3) Inverter



4) 1-bit Full Adder

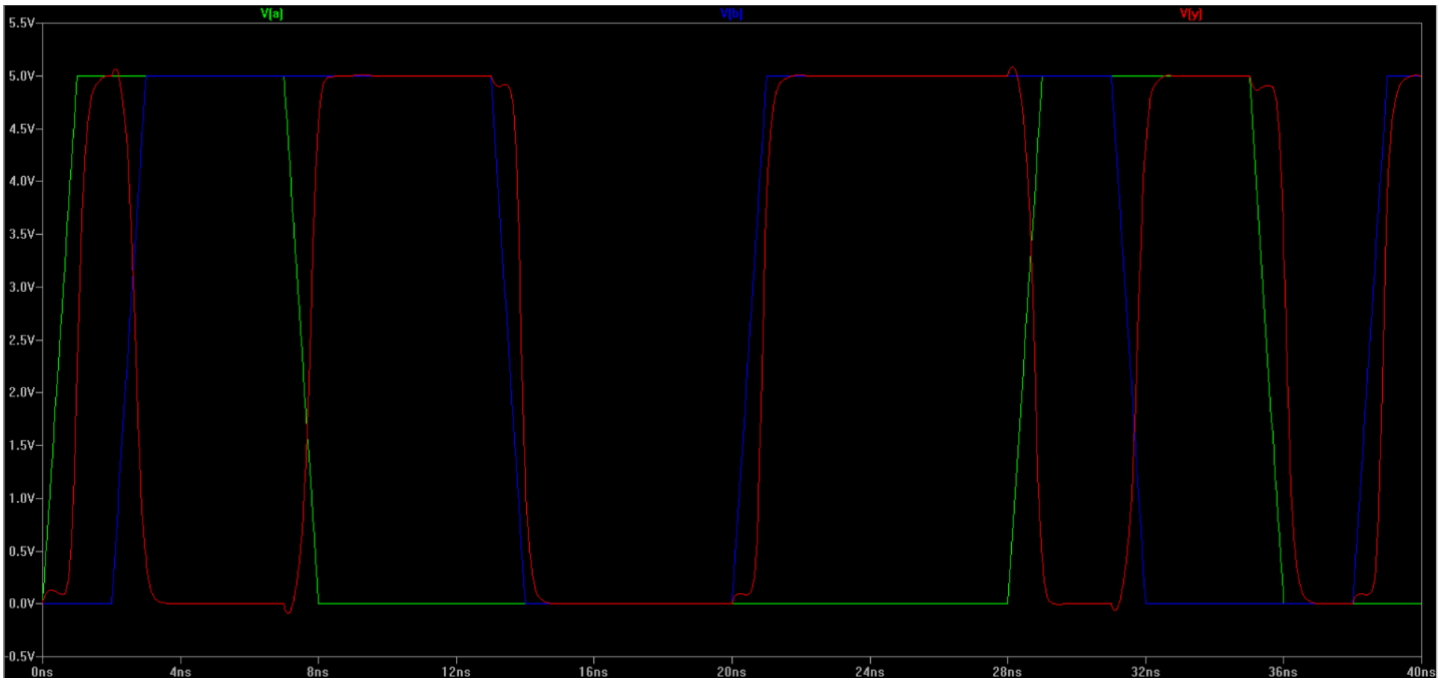


5) 4-bit ripple carry adder

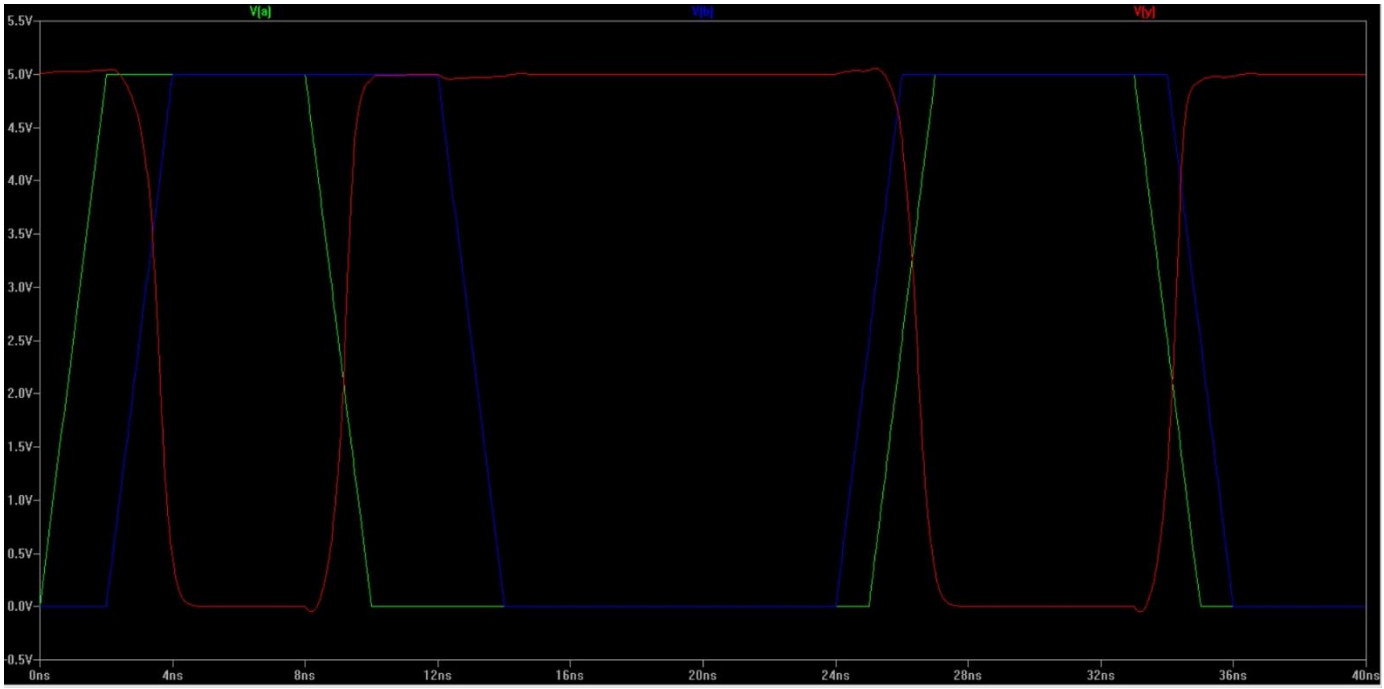


Spice Simulation Results

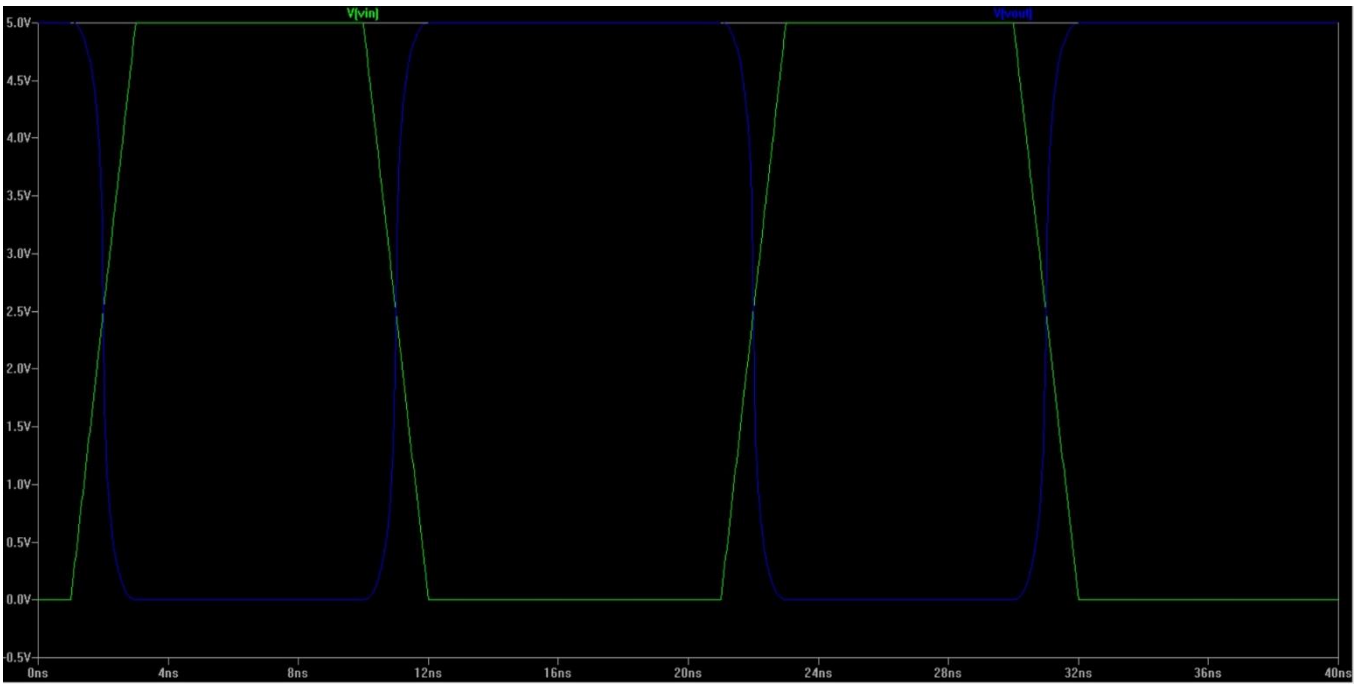
1) 2 input XOR



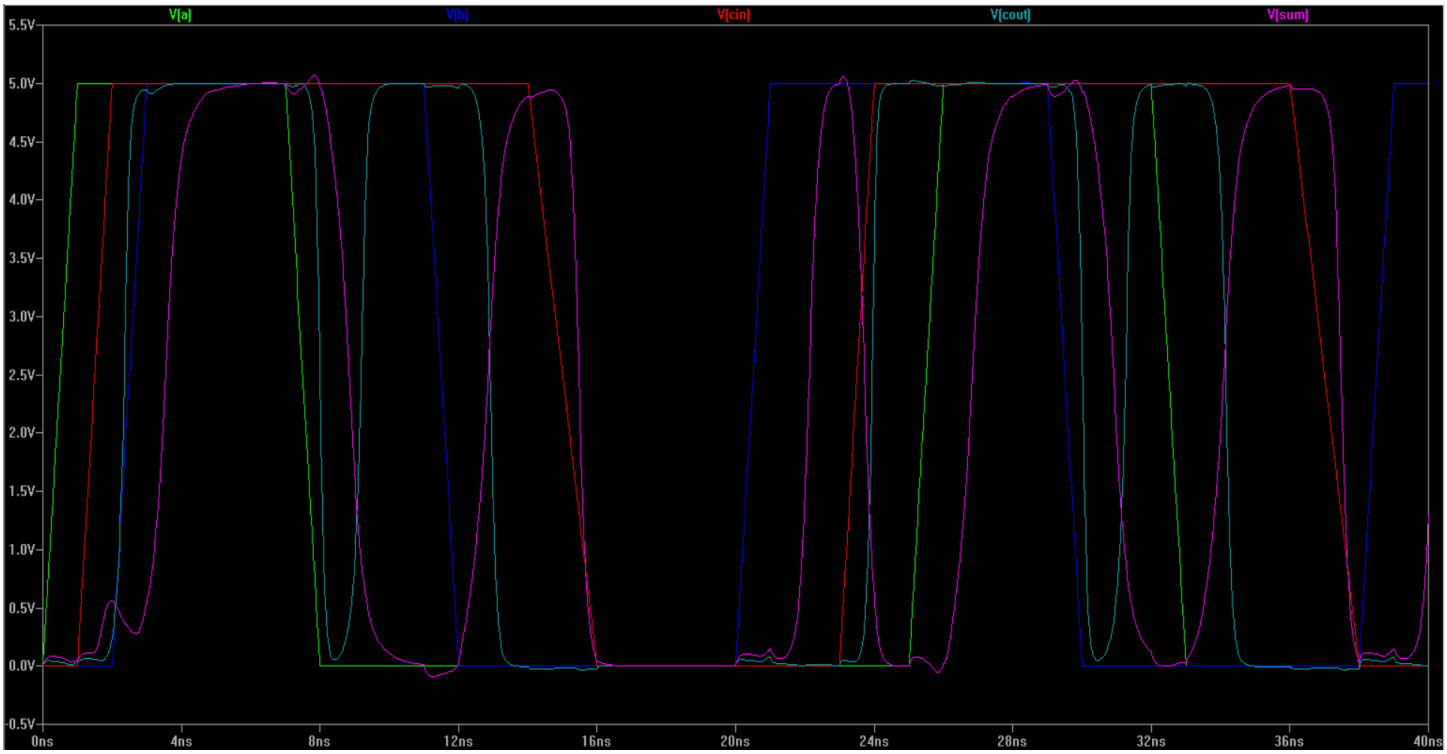
2) 2 input NAND



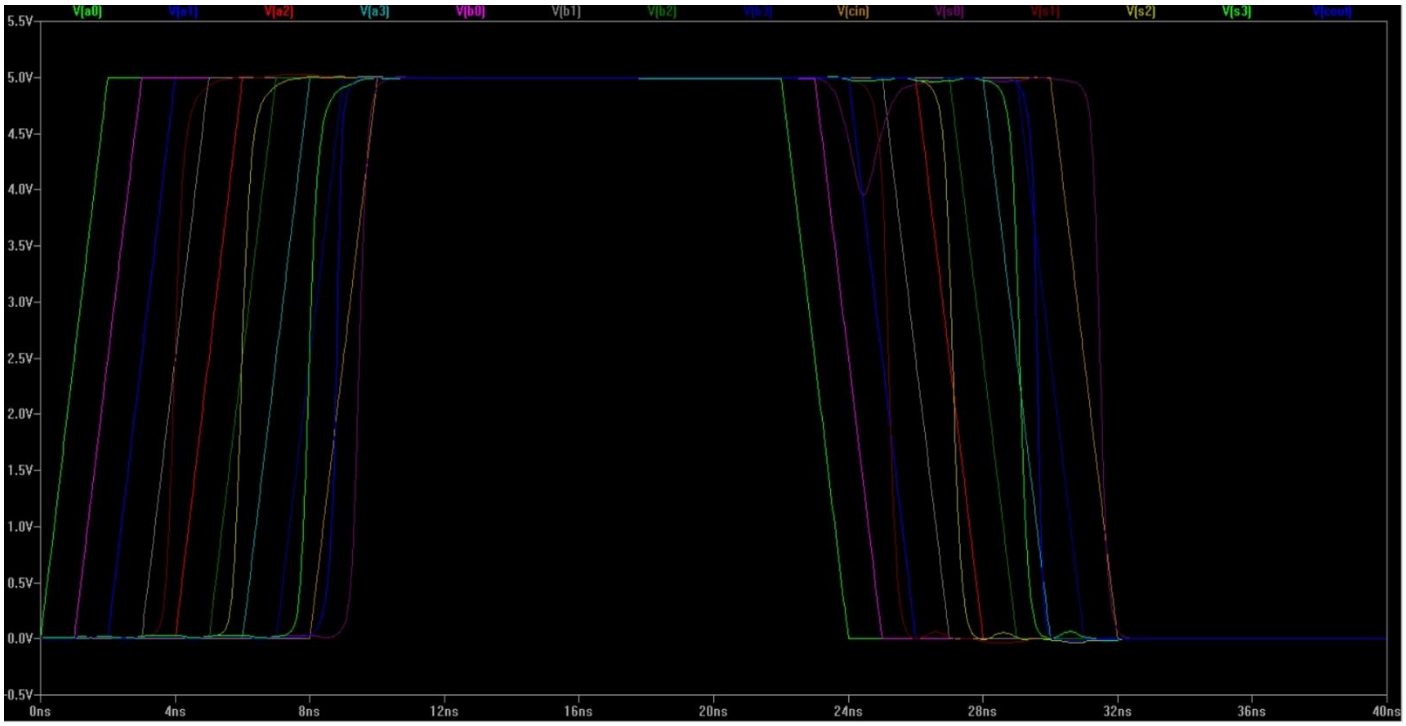
3) Inverter

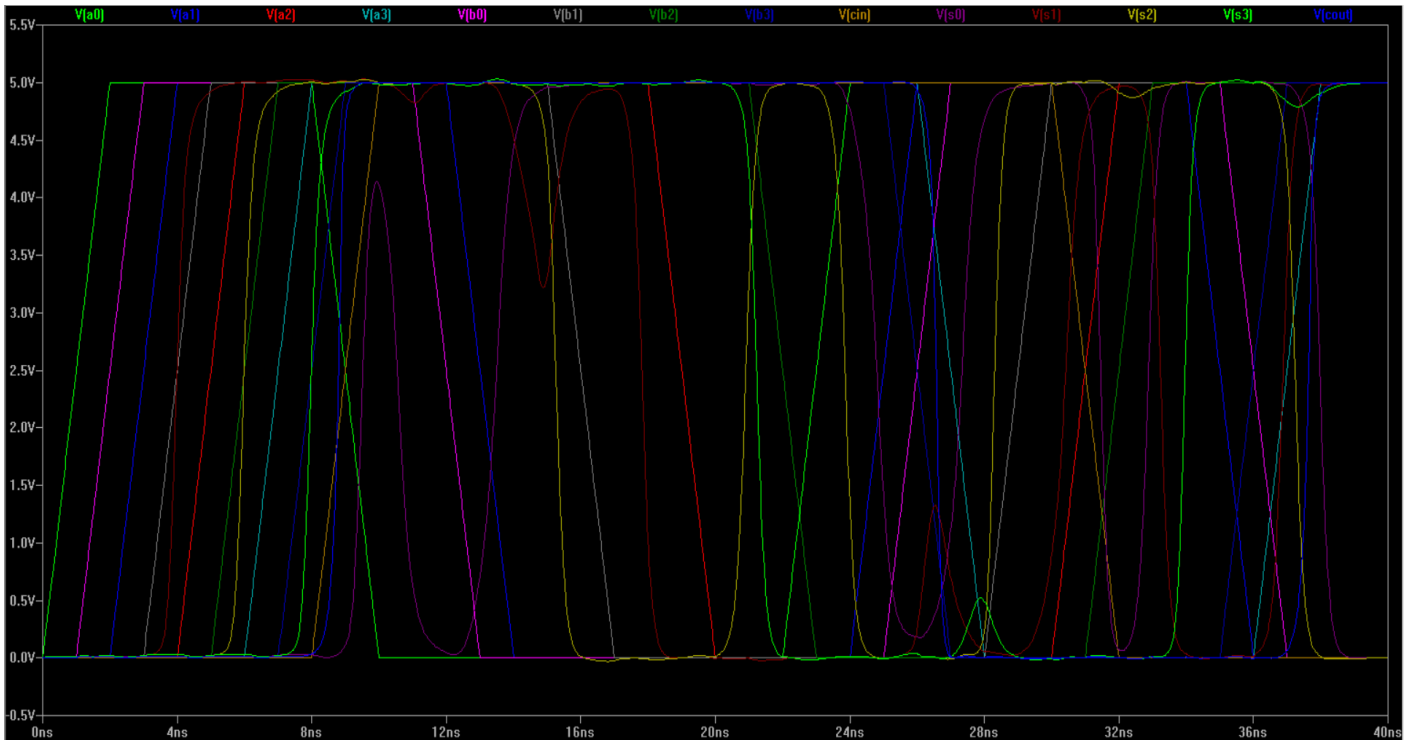


4) 1 bit full adder



5) 4-bit Ripple Carry Adder





Layout Parameters

Parameters	Values
Average Delay	17.88ns
Average Power	2.75mW
Layout Area	12.6mm (lamda= 0.25um)

Conclusion

The full adder circuit is realized using gates like xor, nand and inverter. Using the full adder thus formed, a 4-bit ripple carry adder is created. The layouts for each of these circuits is designed using Magic and its working is tested and verified by observing the simulation results in LTSpice IV simulator. Propagation delays is observed in output waveforms and is calculated and recorded.