VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

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SCHOOL OF ELECTRICAL ENGINEERING

CAT – II

Fall Semester 2018 – 19

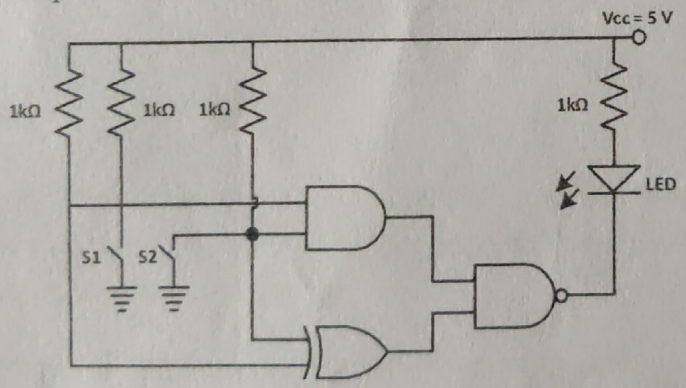
Class Nbrs.	: 0602, 0662 & 0645		
Course Code	: EEE 1001	**Date of Exam**	:
Course Title	: Basic Electrical and Electronics Engineering	**Max. Marks**	: 50
Faculty	: N. Arun, R. Raja Singh, R. M. Brisilla	**Duration**	:1 ½ hours

Answer all the questions

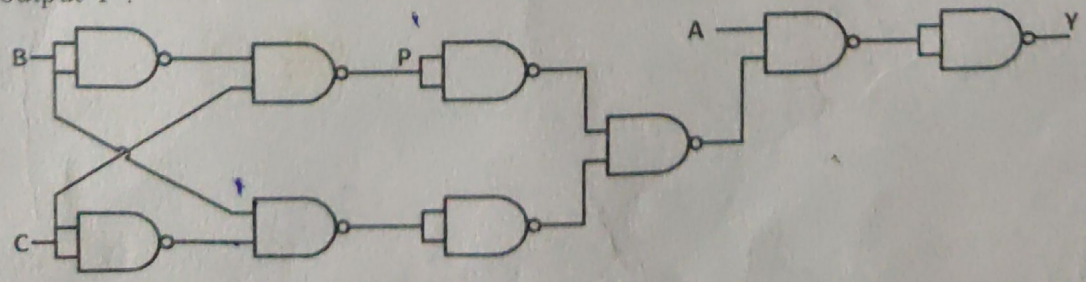
1 A circuit consisting of a single resistor 'R' and an inductor 'L' in series is driven by 25 V rms, 50 Hz sinusoidal voltage source. A capacitor is to be placed in parallel with the source to improve the power factor. Given that the average power dissipated in the R is 100 W and that the reactive power delivered to L is 75 Var. What value of 'C' will yield a 0.9 power factor lagging as seen by the source? **[10]**

2. A three phase wiring system to be constructed for a residential house with necessary appliances. There are 2 bedrooms with attached bathroom, one hall and one kitchen in the house. Assuming approximate power rating of the appliances draw the circuit diagram with equal load sharing among the phases and draw the phasor diagram of the corresponding circuit. Also draw the wiring diagram of any three appliances. Assume relevant data. **[10]**

3. Find the state of the LED (ON/OFF) with respective to switch S1 and S2 position and prove the same through the truth table. **[5]**



4. If the point P got strucked to the binary state high (positive logic), what will be the output Y ? **[5]**



5. Map the given expression and write down the minterm for the following output. [10]
$W = R + \overline{P}Q + \overline{R}S$

6. Compute the following; [10]

a. $(00100101)_2 - (35)_{10} = (\_\_\_\_\_)_2$

b. $(4053.231)_{10} = (\_\_\_\_\_)_2$

c. $(A3F)_{16} - (135)_8 = (\_\_\_\_\_)_{10}$

d. $(101010.1010)_2 = (\_\_\_\_\_)_{10}$

e. $(A3)_{16} - (111,111,1)_2 = (\_\_\_\_\_)_8$