Questions from Test 1

One question on concurrency from Test 1 will be repeated verbatim in Test 2.

Memory management

(1) Show the typical memory hierarchy of a computer system. Explain the tradeoffs between latency (access times), capacity, and persistence, across different levels of memory hierarchy.

(2) What is a page table?

(3) How many page tables are maintained by an operating system?

(4) If there were no TLB, how would memory accesses be affected?

(5) What are the following? What do they do? Where are they located?

A. Memory Management Unit (MMU)
B. Translation Lookaside Buffer (TLB)
C. Page tables
D. Swap device

(6) Where are MMU, Page Table and TLB located?

(7) What is a page fault and a TLB miss? Which system component resolves each of them?

(8) Which statements are true? If a statement is false, then correct it.

A. A page table is an array of physical memory pages
B. Page table entries dictate whether a process can read, write, or execute the contents of a physical page.
C. A page table maps physical page numbers to virtual page numbers
D. Page table entries can be used to track which memory pages are infrequently accessed.

(9) How is a virtual address converted to a physical address in a virtual memory system? Explain the roles of MMU, TLB, and Page Tables.

(10) If you increase or decrease the page size in a system, how (and why) will it affect ***(a)*** the size of the page tables, and ***(b)*** the TLB miss ratio?

(11) What's TLB Coverage? Why is TLB coverage important? How can one increase the TLB coverage?

(12) In memory management, what is meant by relocation and protection? Why are they needed?

(13) Consider a machine with B-bit architecture (i.e. virtual address and physical address are B bits long). Size of a page is P bytes.

A. What is the size (in bytes) of the virtual address space of a process?
B. How many bits in an address represent the byte offset into a page?
C. How many bits in an address are needed to determine the page number ?
D. How many page-table entries does a process' page-table contain?

(14) A machine has a 32-bit address space and an 4KB page. The page table is entirely in

hardware. Each page-table entry is 4 bytes in size. When a process starts, the page table is copied to the hardware from memory, at the rate of one byte every 25 nano-second. If each process has a CPU burst of 200 msec (including the time to load the page table), what fraction of the CPU time is devoted to loading the page tables? (Assume that each process uses its entire virtual address space during execution.)

(15) Consider a machine having a 32-bit virtual address and 8KB page size.

A. What is the size (in bytes) of the virtual address space of a process?
B. How many bits in the 32-bit virtual address represent the byte offset into a page?
C. How many bits in the 32-bit address are needed to determine the page number ?
D. How many page-table entries does a process' page-table contain?

2. **[10 pts]** Consider a machine having a 64-bit virtual address and 16KB page size.

A. What is the size (in bytes) of the virtual address space of a process?
B. How many bits in the virtual address represent the byte offset into a page?
C. How many bits in the virtual address are needed to determine the page number ?
D. How many page-table entries does a process' page-table contain?

(16) For each of the following decimal virtual addresses, compute the virtual page number and offset for a 4-KB page, an 8 KB page, and a 16KB page: 20000, 32768, 60000.

(17) A computer with a 32-bit address uses a two-level page table. Virtual addresses are split into a 9-bit top-level page table field, an 10-bit second-level page table field, and an offset. How large are the pages and how many pages are there in the address space?

(18) Which system components handle TLB misses and page-faults, and how, in a machine with

(a) architected page-table?
(b) architected TLB?

(19) What is meant by "Internal" fragmentation?

(20) What is "External" fragmentation of memory? How can it be resolved?

(21) Suppose that "page table pages are paged", meaning that (some or all of) the memory allocated to hold page tables can be paged-in and out of the main memory by the operating system. Suppose further that you have two-level page-tables, i.e. a first-level page-directory which tracks the second-level page table blocks.

(a) Which parts of the page-table can be paged (moved in and out of main memory)?
(b) Where are the memory address translations (i.e. page table entries) for the "paged page-table"?
(c) Can the memory used for your answer in (b) be paged? Why? Or Why not?

(22) Consider two processes that set up one page of shared memory for inter-process communication with each other. Given what you know about virtual memory management, explain how the OS would set up this shared memory page at the level of page tables?

(23) Suppose that the Operating System wanted to track (or intercept) every write performed to a specific memory page by a user-level process. Explain how the OS would achieve this goal?

(24) How does TLB Coverage and TLB miss ratio vary with the size of a page?

(25) Consider a virtual memory system running on an architected page-table hardware supporting two-level page tables. Page tables are not locked in memory and may be swapped to disk. An lw (load word) instruction reads one data word from memory; the address is the sum of the value in a register and an immediate constant stored in the instruction itself. Neither machine instructions nor page-table entries nor data words can cross a page boundary. In the worst case, how many page faults could be generated as a result of the fetch, decode, and execution of an lw instruction? Explain why?

(26) Considering memory protection, explain how the operating system ensures that user-level processes don't access kernel-level memory?

(27) How can the operating system track
A. Dirty (or updated) memory pages for the purpose of eviction?
B. Every memory write performed by a process to specific memory pages?

(28) What are superpages? Why are they useful? What are the constraints on their sizes, placement, and page attributes (protection, reference, and dirty bits)?

(29) Superpages
A. What are the advantages and disadvantages of superpages?
B. How many TLB entries and page table entries are there for each superpage?
C. What are the restrictions on superpage size, allocation, and placement?

(30) If a superpage has a size equal to 4 base pages, how many TLB entries are occupied by the superpage? How many page table entries are occupied by the same superpage? Explain why.

Page Replacement Algorithms

(31) What is hysteresis? Explain how the page-out/page-in mechanism in the OS uses hysteresis and why?

OR

How does the swap daemon (paging mechanism) avoid rapid oscillations in paging activity when memory pressure increases?

(32) Under what condition does thrashing occur in memory management? How can the OS resolve thrashing?

(33) What is the purpose of “Referenced” and “Modified” (“Dirty”) bits in the page table entry? How are they manipulated by the (a) hardware, and (b) operating system?

(34) Describe Optimal Page Replacement (OPR) algorithm. Why is it called "Optimal"? Why is it not practical to implement OPR?

(35) Explain the Least Recently Used (LRU) page replacement algorithm.

(36) Why is LRU a good approximation of Optimal Page Replacement (OPR)?

(37) OPR (Optimal Page Replacement) and LRU (Least Recently Used)

(a) Why is it impossible to implement OPR?

(b) Why is it hard to implement LRU?

(38) What is a “working set”? Why is it so important?

(39) Explain how the following page replacement algorithms work: (a) Clock, (b) WSClock (c) Second Chance.

(40) How does the Second Chance page replacement algorithm improve upon the FIFO page replacement algorithm?

(41) How does Clock page replacement algorithm improve upon the Second Chance page replacement algorithm?

(42) Briefly explain how the following page replacement algorithms work:

(a) FIFO (First In First Out)

(b) Second Chance

(c) Clock.

Segmentation

(43) How are relocation and protection implemented in Pentium architecture? Consider the roles of both segmentation and paging.

(44) How is segmentation different from paging? Why was each technique invented?

(45) Using either Multics or Pentium architecture as an example, explain how segmentation is used in enforcing protection?

(46) How is a virtual address converted to a physical address, considering both segmentation and paging in (a) Multics and (b) Pentium architectures?

(47) In paged-segmentation implementations: Multics has one page table per segment, whereas Pentium has one page table for multiple segments. Why the difference? Which one is better? Why?

(1) OR (a) How many page tables are there per segment in Multics and Pentium. (b) Which one (Multics/Pentium) is better? Why?

(48) What problem does segmentation solve that paging doesn't solve? What problem does paging solve that segmentation doesn't solve?

(49) Which of the following memory designs can cause internal fragmentation only, external fragmentation only, both, or neither? Briefly explain why.

A. Pure paging
B. Pure segmentation
C. Paging with Segmentation
D. Using superpages of the same size (no base pages or any other superpage size)
E. Using a mix of superpages of different sizes