Q.1. A block set associative cache consists of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks each consists of 128 words of 16-bit length.

i) How many bits have there in main memory address?

ii) How many bits are there in cache memory address (TAG, SET & WORD fields)?

→ i) main memory size = 4096 blocks × 128 word.
$= 2^{12} \times 2^7$
$= 2^{19}$ = 19 bits.

∴ main memory address lines required is equal to 19.

ii) Cache memory has 64 blocks divided into 4 blocks sets, thus each set has 16 blocks.

∴ $16 = 2^4$ address lines

Block offset = 4 as.

Block size = $128 = 2^{4+4}$

Tag = Remaining lines.
= 19 − 4 − 7

Tag = 8 address lines.

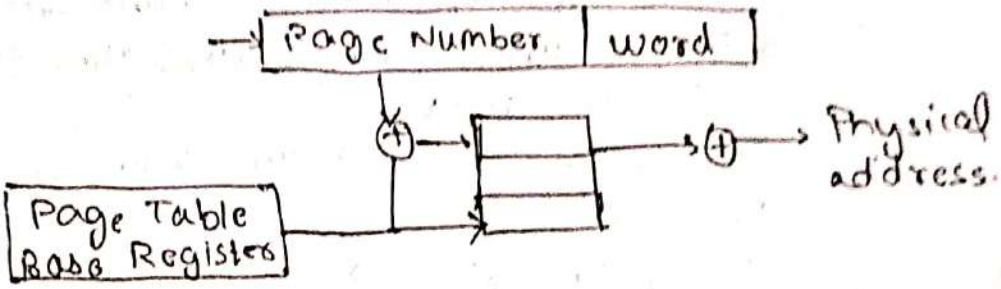
Tag = 8 bits.

7	4	1
Tag	Line no	Block offset

Q.1b] Explain how virtual address is translated to physical address with suitable example.

→ 1] The memory management unit or the paging unit is responsible to convert the virtual or linear address to physical address.

2] The address translation takes place as follows.



3] The address given by the processor i.e the linear or virtual address into the page number & the word number in that page.

4] The page number is checked for its presence in the main memory by comparing the entry for each page in the page table. If the page is present the word required is read from page in main memory.

5] If the page required by the processor is not in the main memory, the page fault occurs & the required page is loaded into the main memory by a special routine called as page fault routine. This technique is called as demand paging i.e the page is brought from essential memory to main memory only when required.

Q.2 Compare Interupt-driven I/O & DMA

→ Interrupt driven I/O.

1] Interrupt driven I/O means CPU issues commands to the I/O module then processed with its normal work until interrupted by I/O device on compulsion of its work.

2] The problem with the programmed I/O is the processor has to wait a long time for the I/O module of concern to be ready for either reception or transmission of more data.

3] The processor while waiting must repeatedly interrogate the status of I/O module, As a result the level of performance of entire system is degraded.

4] The processor issues an I/O command to a module & then go on to do some other useful work. The I/O module will then interrupt processor to request, when it is ready to exchange data with processor.

Q.3 Very-long instructor word (VLIW) architecture are a suitable alternative for exploiting instruction-level parallelism (ILP) in program, justify this statements with a suitable example.

→ i] Very-long instruction word (VLIW) architecture are a suitable alternative for exploiting instruction-level parallelism (ILP) in program, That is, for executing more than one basic (primitive) instruction at a time.

2] These processors contains multiple functional units, fetch from the instruction cache a VLIW containing several primitive instruction & dispatch entire VLIW for parallel execution.

3] These capabilities are exploited for parallel execution. Which generate code that has grouped together independent primitive instructions

executable in parallel.

4] The processors have relatively simple control logic because they do not perform any dynamic scheduling nor redoney of operation.

5] VLIW has been described as a natural successor to RISC, because its moves complexity from hardware to compiler allowing simpler faster processors.

6] The objective of VLIW is to eliminate the complicated instruction scheduling & parallel dispatch that occurs in most modern microprocessor in theory, a VLIW processor.

DMA.

1] Direct memory access means CPU grants I/O module authority to read from or write to memory without involvements.

2] The previous ways I/O suffers from 2 inherent drawbacks.
a] The I/O transfer rate is limited by the speed with which processor can test & service a device.
b] The processor is tied up in managing an I/O transfer; a number of instructions must be executed for each I/O transfer.

3] When large volume of each data are to be moved, DMA is a more efficient technique.

4] The processor continues with other work it has delegated this I/O operation to the DMA module & that module will take care of it.

5] In programmed I/O CPU takes care of whether the device is ready or not. Data maybe lost. It is meaningful to allow device to put the data directly to memory. This is called DMA.