EE 599 Lab 2

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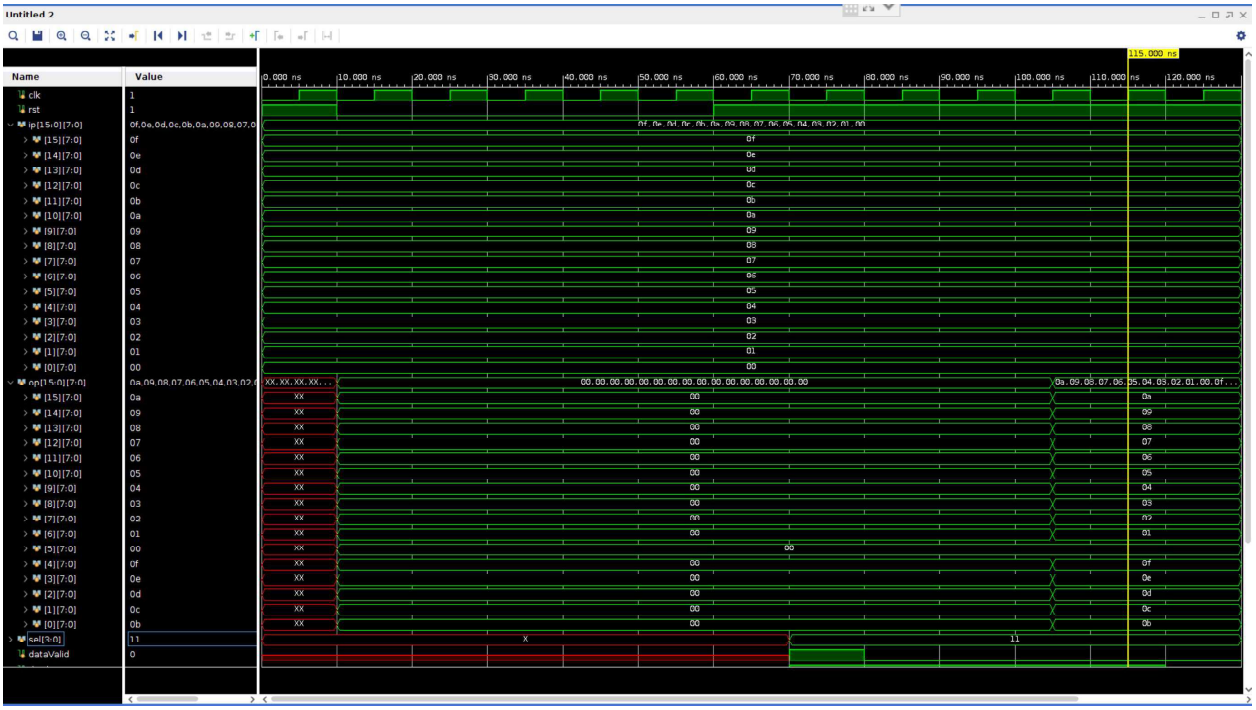
1. BARREL SHIFTER

Simulation

Original sequence $ip = \{f, e, d, c, b, a, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0\}$

Rotate by $sel = 11$

Output = $\{a, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, f, e, d, c, b, \}$



a. *16-element shifter*

Timing Report – min clock period = 2.25 ns

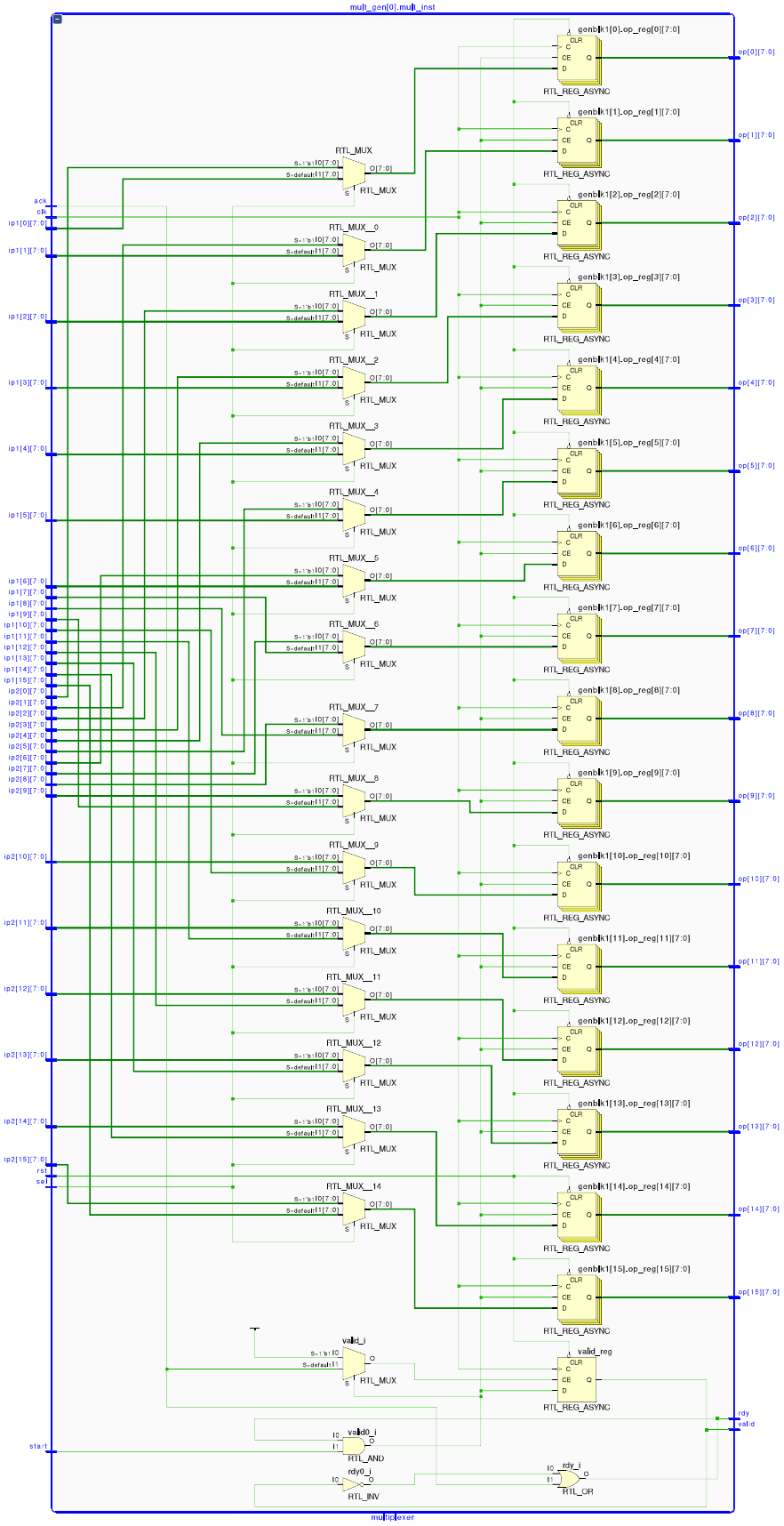
Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped
1	clk	2.000	0.000	1.000	☐	[get_ports clk]	<unsaved c(	

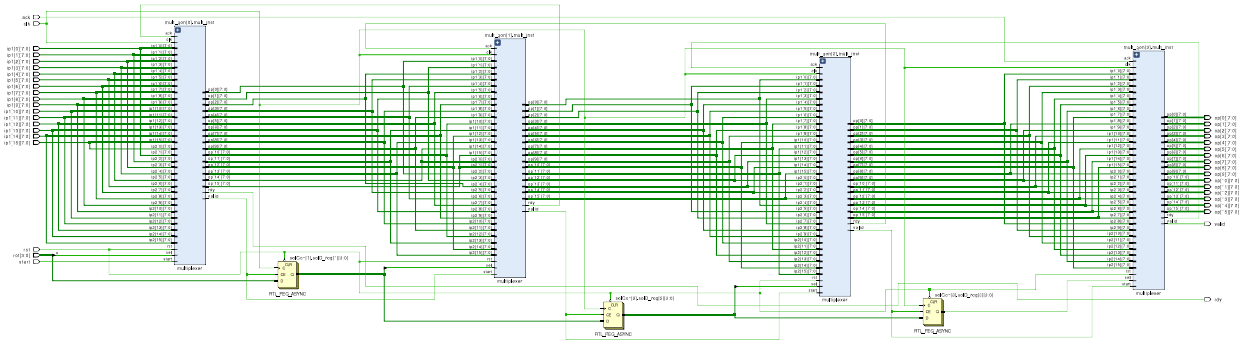
Double click to create a Create Clock constraint

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-0.245 ns	Worst Hold Slack (WHS):	0.130 ns	Worst Pulse Width Slack (WPWS):	0.408 ns
Total Negative Slack (TNS):	-56.584 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	384	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	906	Total Number of Endpoints:	906	Total Number of Endpoints:	523

Timing constraints are not met.

Netlist (complete design and single layer in the shifter network):


mult_gen[0].mult_inst
genblk1[0].op_reg[0][7:0]
RTL_REG_ASYNC
op[0][7:0]
genblk1[1].op_reg[1][7:0]
op[1][7:0]
genblk1[2].op_reg[2][7:0]
op[2][7:0]
genblk1[3].op_reg[3][7:0]
op[3][7:0]
genblk1[4].op_reg[4][7:0]
op[4][7:0]
genblk1[5].op_reg[5][7:0]
op[5][7:0]
genblk1[6].op_reg[6][7:0]
op[6][7:0]
genblk1[7].op_reg[7][7:0]
op[7][7:0]
genblk1[8].op_reg[8][7:0]
op[8][7:0]
genblk1[9].op_reg[9][7:0]
op[9][7:0]
genblk1[10].op_reg[10][7:0]
op[10][7:0]
genblk1[11].op_reg[11][7:0]
op[11][7:0]
genblk1[12].op_reg[12][7:0]
op[12][7:0]
genblk1[13].op_reg[13][7:0]
op[13][7:0]
genblk1[14].op_reg[14][7:0]
op[14][7:0]
genblk1[15].op_reg[15][7:0]
op[15][7:0]
RTL_MUX
RTL_MUX_0
RTL_MUX_1
RTL_MUX_2
RTL_MUX_3
RTL_MUX_4
RTL_MUX_5
RTL_MUX_6
RTL_MUX_7
RTL_MUX_8
RTL_MUX_9
RTL_MUX_10
RTL_MUX_11
RTL_MUX_12
RTL_MUX_13
RTL_MUX_14
ack
clk
ip1[0][7:0]
ip1[1][7:0]
ip1[2][7:0]
ip1[3][7:0]
ip1[4][7:0]
ip1[5][7:0]
ip1[6][7:0]
ip1[7][7:0]
ip1[8][7:0]
ip1[9][7:0]
ip1[10][7:0]
ip1[11][7:0]
ip1[12][7:0]
ip1[13][7:0]
ip1[14][7:0]
ip1[15][7:0]
ip2[0][7:0]
ip2[1][7:0]
ip2[2][7:0]
ip2[3][7:0]
ip2[4][7:0]
ip2[5][7:0]
ip2[6][7:0]
ip2[7][7:0]
ip2[8][7:0]
ip2[9][7:0]
ip2[10][7:0]
ip2[11][7:0]
ip2[12][7:0]
ip2[13][7:0]
ip2[14][7:0]
ip2[15][7:0]
rst
sel
valid_i
valid_reg
valid
rdy
start
valid0_i
RTL_AND
rdy0_i
RTL_INV
rdy_i
RTL_OR
multiplexer



Utilization: 1.85% LUTs used

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
barrel	267	522	266	1
mult_gen[0].mult_inst (multiplexer)	66	129	0	0
mult_gen[1].mult_inst (multiplexer_0)	67	129	0	0
mult_gen[2].mult_inst (multiplexer_1)	67	129	0	0
mult_gen[3].mult_inst (multiplexer_2)	67	129	0	0

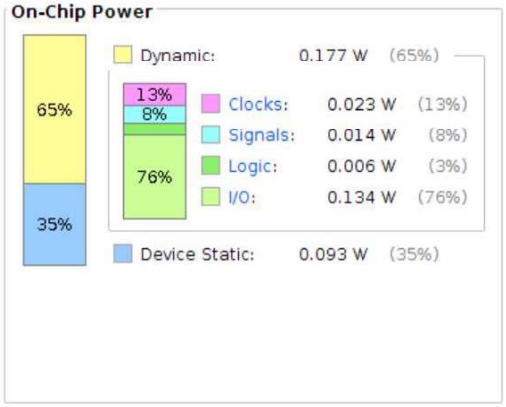
Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
barrel	1.85%	1.81%	492.59%	3.13%
mult_gen[0].mult_inst (multiplexer)	0.46%	0.45%	0.00%	0.00%
mult_gen[1].mult_inst (multiplexer_0)	0.47%	0.45%	0.00%	0.00%
mult_gen[2].mult_inst (multiplexer_1)	0.47%	0.45%	0.00%	0.00%
mult_gen[3].mult_inst (multiplexer_2)	0.47%	0.45%	0.00%	0.00%

Power: Total = 0.27 W, dynamic = 0.18 W

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.27 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.1°C**
Thermal Margin:	71.9°C (6.0 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



b. *64-element shifter*

Timing Summary: Min clock period = 2.8 ns

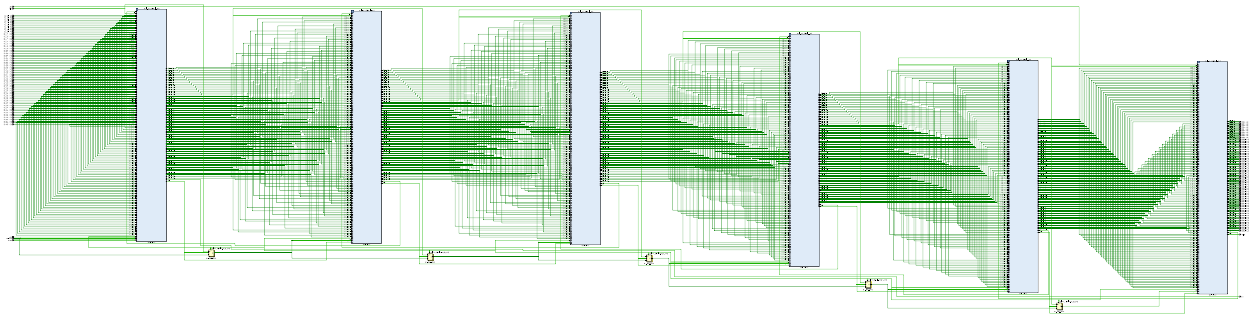
Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Sc
1	clk	2.300	0.000	1.150	☐	[get_ports clk]	<unsaved cc	

Double click to create a Create Clock constraint

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-0.469 ns	Worst Hold Slack (WHS):	0.127 ns	Worst Pulse Width Slack (WPWS):	0.650 ns
Total Negative Slack (TNS):	-480.620 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	1024	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	5669	Total Number of Endpoints:	5669	Total Number of Endpoints:	3103

Timing constraints are not met.

Netlist:



Utilization: 10.8% slice LUTs used

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
barrel	1557	3102	1036	1

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
barrel	10.81%	10.77%	1918.52%	3.13%

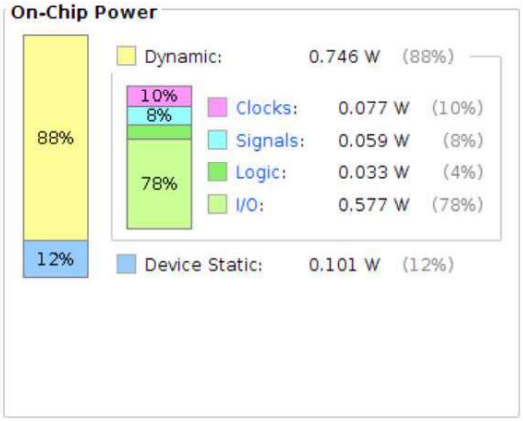
Power: 0.85W, dynamic = 0.75W

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.846 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**34.8°C**
Thermal Margin:	65.2°C (5.4 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Utilization: 10.8% slice LUTs used

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
> N barrel	1557	3102	1036	1

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
> N barrel	10.81%	10.77%	1918.52%	3.13%

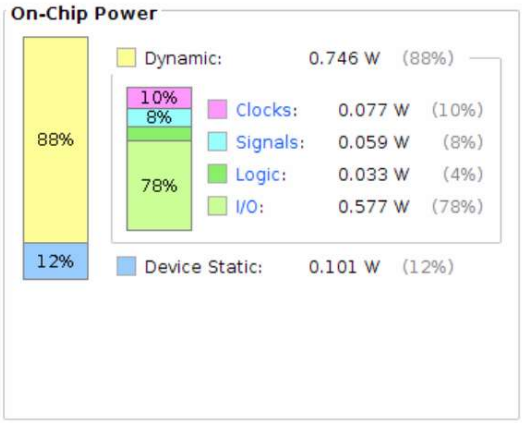
Power: 0.85W, dynamic = 0.75W

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.846 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**34.8°C**
Thermal Margin:	65.2°C (5.4 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



2. SYSTOLIC ARRAY

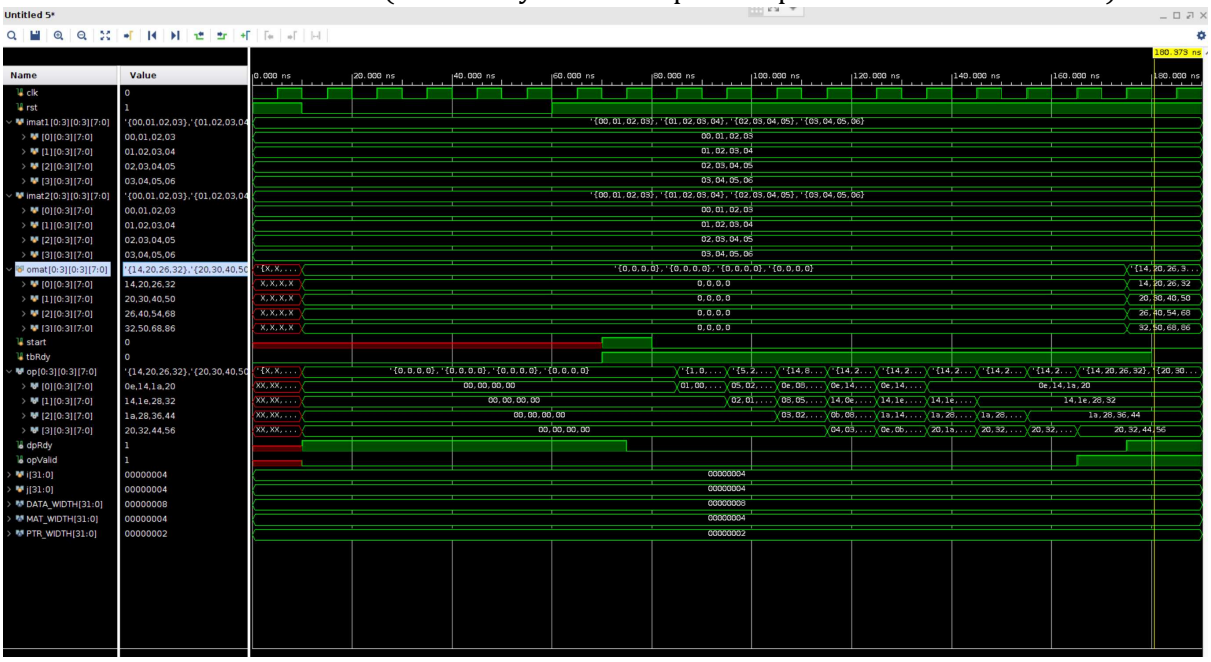
a. Matrix size = 4×4

Clocks required to multiply two $n \times n$ matrices = $3n - 2$

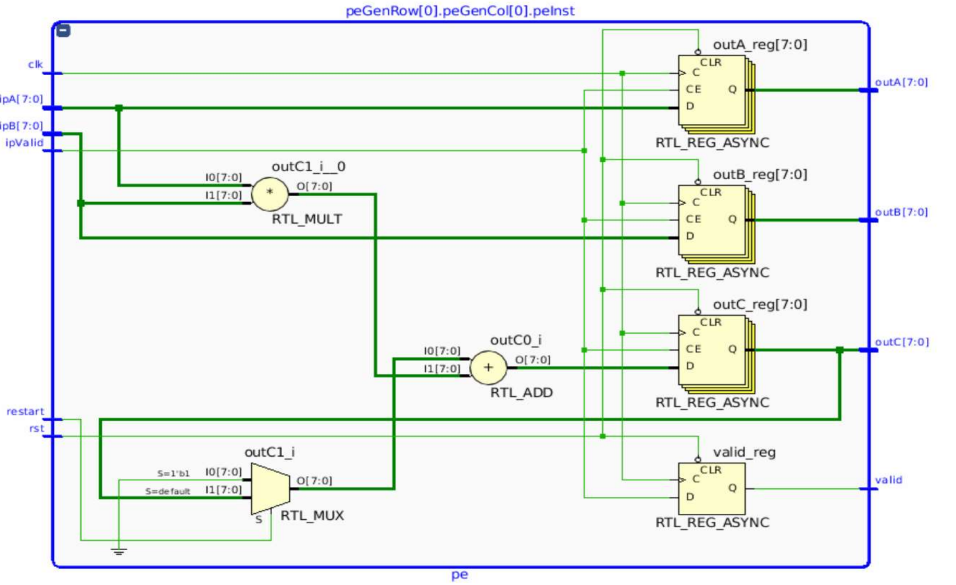
Input and output matrix values at the end of computation can be seen at the top left of the waveform below.

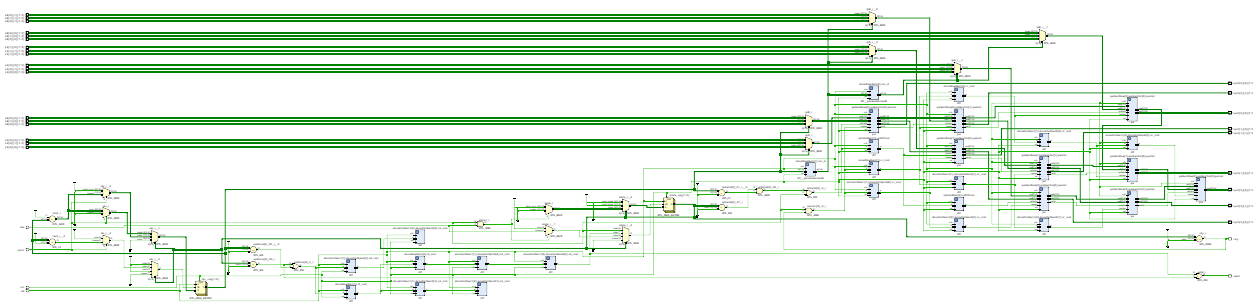
$$ipA = \begin{bmatrix} 0 & 1 & 2 & 3 \\ 1 & 2 & 3 & 4 \\ 2 & 3 & 4 & 5 \\ 3 & 4 & 5 & 6 \end{bmatrix},\ ipB = \begin{bmatrix} 0 & 1 & 2 & 3 \\ 1 & 2 & 3 & 4 \\ 2 & 3 & 4 & 5 \\ 3 & 4 & 5 & 6 \end{bmatrix},\ omat = \begin{bmatrix} 14 & 20 & 26 & 32 \\ 20 & 30 & 40 & 50 \\ 26 & 40 & 54 & 68 \\ 32 & 50 & 68 & 86 \end{bmatrix}$$

Simulation waveform: (takes 10 cycles to compute output – from 65 ns to 165 ns)



Schematics (for 3×3 matrix multiplier for clarity):





Utilization Report:

Name	Slice LUTs	Slice Registers	F7 Muxes	F8 Muxes	Bonded IOB (54)	BUFGCTRL (32)
> N sysArr	81.87%	20.99%	5.82%	5.82%	11388.89	3.13%

Hierarchy

Name	Slice LUTs	Slice Registers	F7 Muxes	F8 Muxes	Bonded IOB (54)	BUFGCTRL (32)
> N sysArr	11789	6046	512	256	6150	1

Timing Report: Min clock period = 6ns

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File
1	clk	5.000	0.000	2.500	☐	[get_ports clk]	<unsaved cc
Double click to create a Create Clock constraint							

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-0.964 ns	Worst Hold Slack (WHS):	0.134 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	-36.071 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	94	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	11939	Total Number of Endpoints:	11939	Total Number of Endpoints:	6047

Timing constraints are not met.

Power Consumption: 2.65 W, dynamic power = 2.52W

Most of the power is in I/O though. Large amount of IO (three 16×16 matrices) is also affecting the synthesis results.

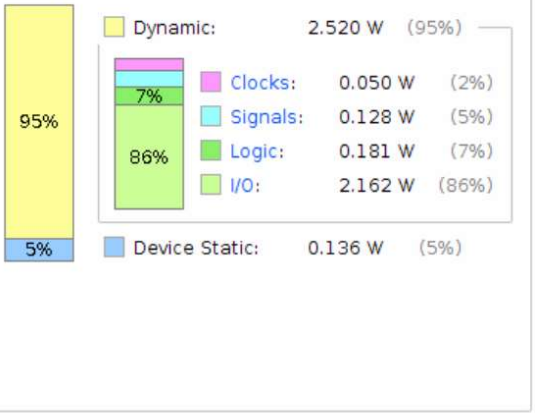
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.655 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**55.6°C**
Thermal Margin:	44.4°C (3.7 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



b. 32×32 matrix multiplication

Utilization: design doesn't fit on this fpga

Name	Slice LUTs	Slice Registers	F7 Muxes	Bonded IOB (54)	BUFGCTRL (32)
sysArr	48621	25247	2048	24582	1

Name	Slice LUTs	Slice Registers	F7 Muxes	Bonded IOB (54)	BUFGCTRL (32)
sysArr	337.65%	87.66%	23.27%	45522.22%	3.13%

Timing Report: Min clock period = 6.7ns

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File
1	clk	6.000	0.000	3.000	☐	[get_ports clk]	<unsaved cc
Double click to create a Create Clock constraint							

Setup

Worst Negative Slack (WNS):	-0.716 ns
Total Negative Slack (TNS):	-38.261 ns
Number of Failing Endpoints:	127
Total Number of Endpoints:	49317

Hold

Worst Hold Slack (WHS):	0.140 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	49317

Pulse Width

Worst Pulse Width Slack (WPWS):	2.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	25248

Timing constraints are not met.

Power: Didn't model successfully

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**10.868 W (Junction temp exceeded!)**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**125.0°C**
Thermal Margin:	-50.3°C (-3.9 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power