Lab 1 Report

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Code: https://github.com/kartiklakhotia/EE599_klakhoti_9258459798

1. **Dense Matrix-Matrix Multiplication**

   Implemented using $rdy/valid$ protocol. Every multiplier/adder can be fed a new input when $rdy == 1$ and the output can be read when $valid == 1$.

   The $rdy/valid$ signals for the entire dot product computer are derived from the $rdy$ signal of $0^{th}$ stage multipliers and $valid$ signal of final stage adder.

   For $n$ input multiplication, we need $n$ multipliers.

   Adders in $r^{th}$ stage = $\frac{n}{2^r}$

   For $k$ bit inputs, bits needed to represent output = $2k + \log_2 n$

   Total # adders = $n - 1$

   Clocks required to produce first output = $\log_2 n$

   Clocks required to multiply two $n \times n$ matrices = $n^2 + \log_2 n$

   Input and output matrix values at the end of computation can be seen at the top left of the waveform below.

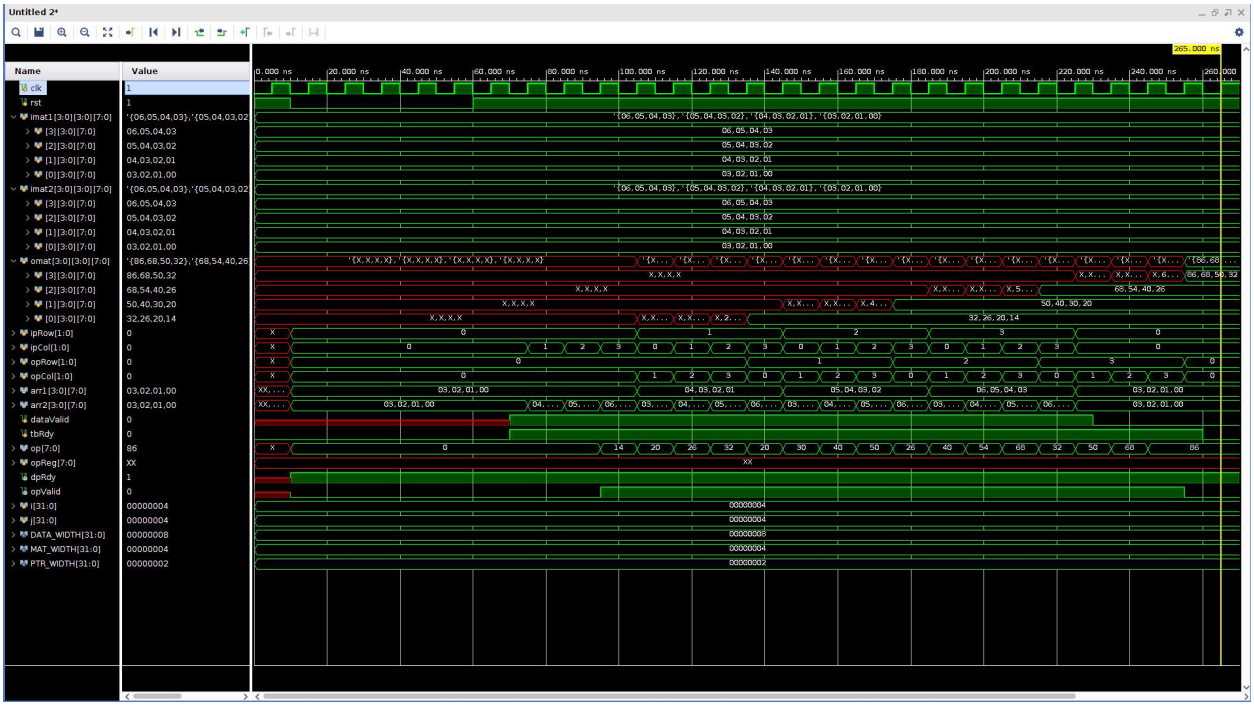
   Inputs:

   a. $imat1 = \begin{bmatrix} 0 & 1 & 2 & 3 \\ 1 & 2 & 3 & 4 \\ 2 & 3 & 4 & 5 \\ 3 & 4 & 5 & 6 \end{bmatrix}$, $imat2 = \begin{bmatrix} 0 & 1 & 2 & 3 \\ 1 & 2 & 3 & 4 \\ 2 & 3 & 4 & 5 \\ 3 & 4 & 5 & 6 \end{bmatrix}$

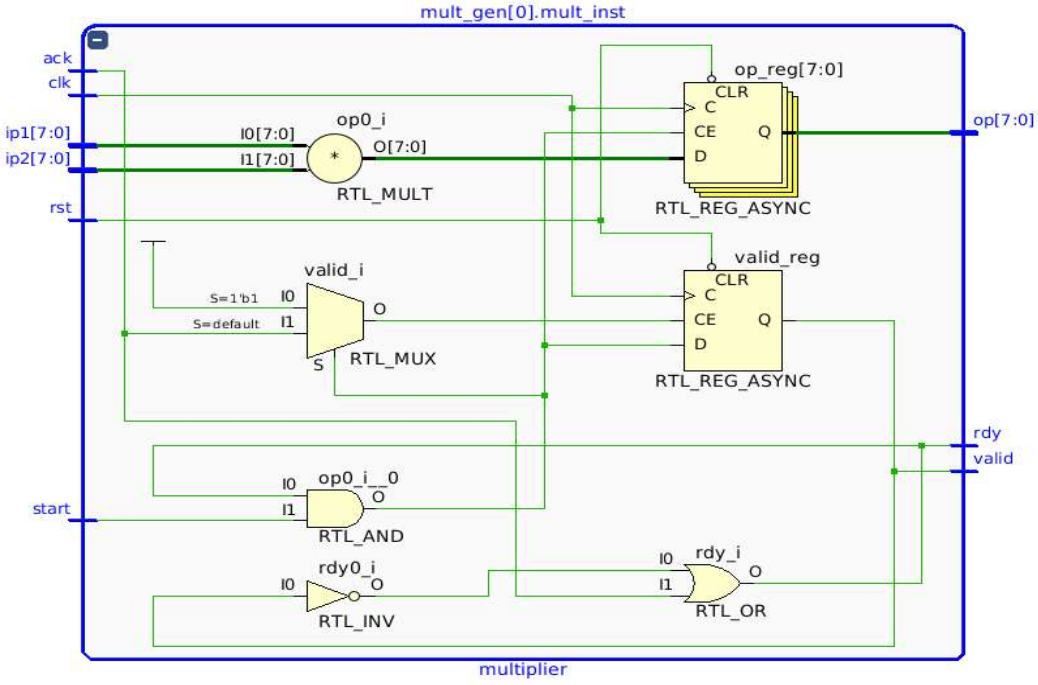
   Output:

2. $omat = imat1 * imat2 = \begin{bmatrix} 14 & 20 & 26 & 32 \\ 20 & 30 & 40 & 50 \\ 26 & 40 & 54 & 68 \\ 32 & 50 & 68 & 86 \end{bmatrix}$

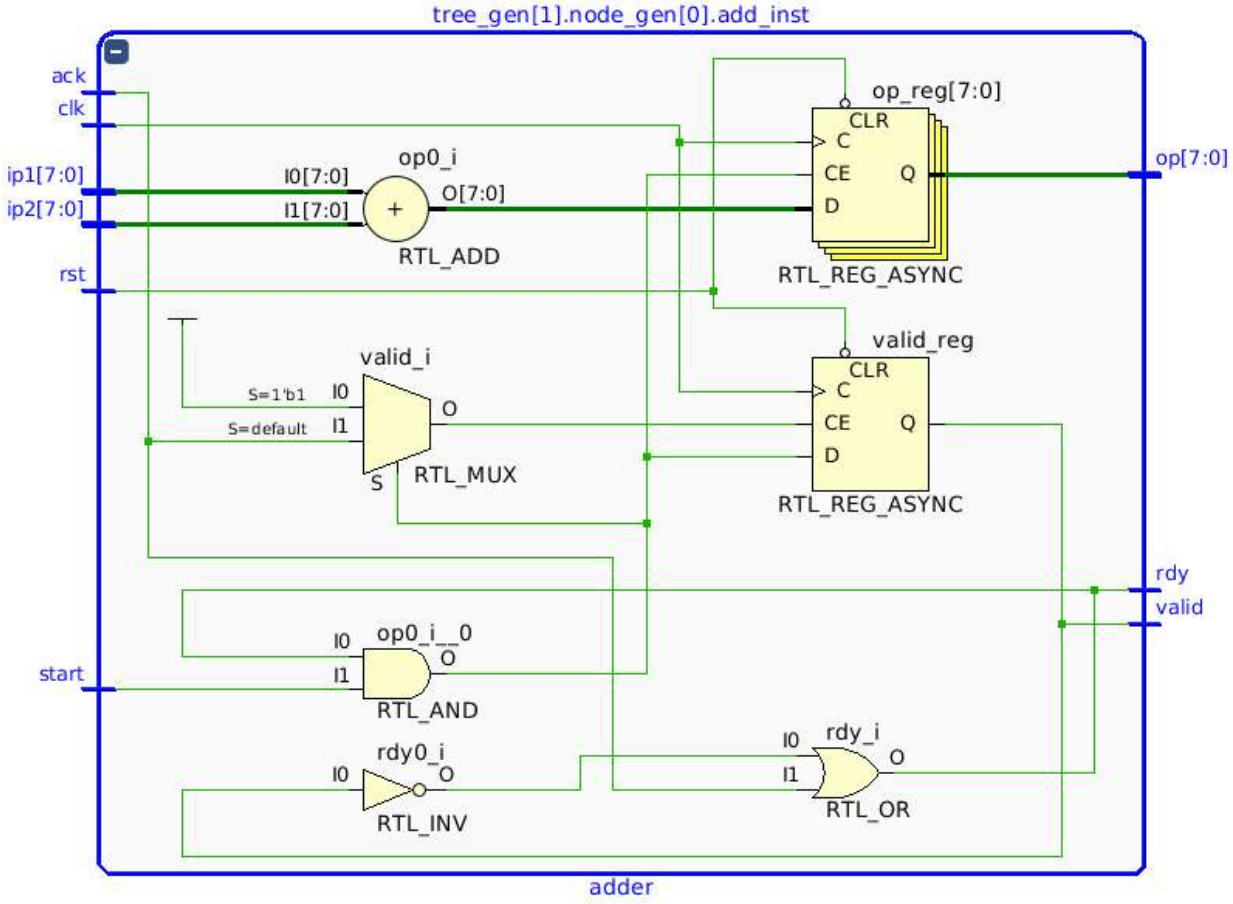
Simulation waveform (18 cycles to do $4 \times 4$ matrix multiplication):



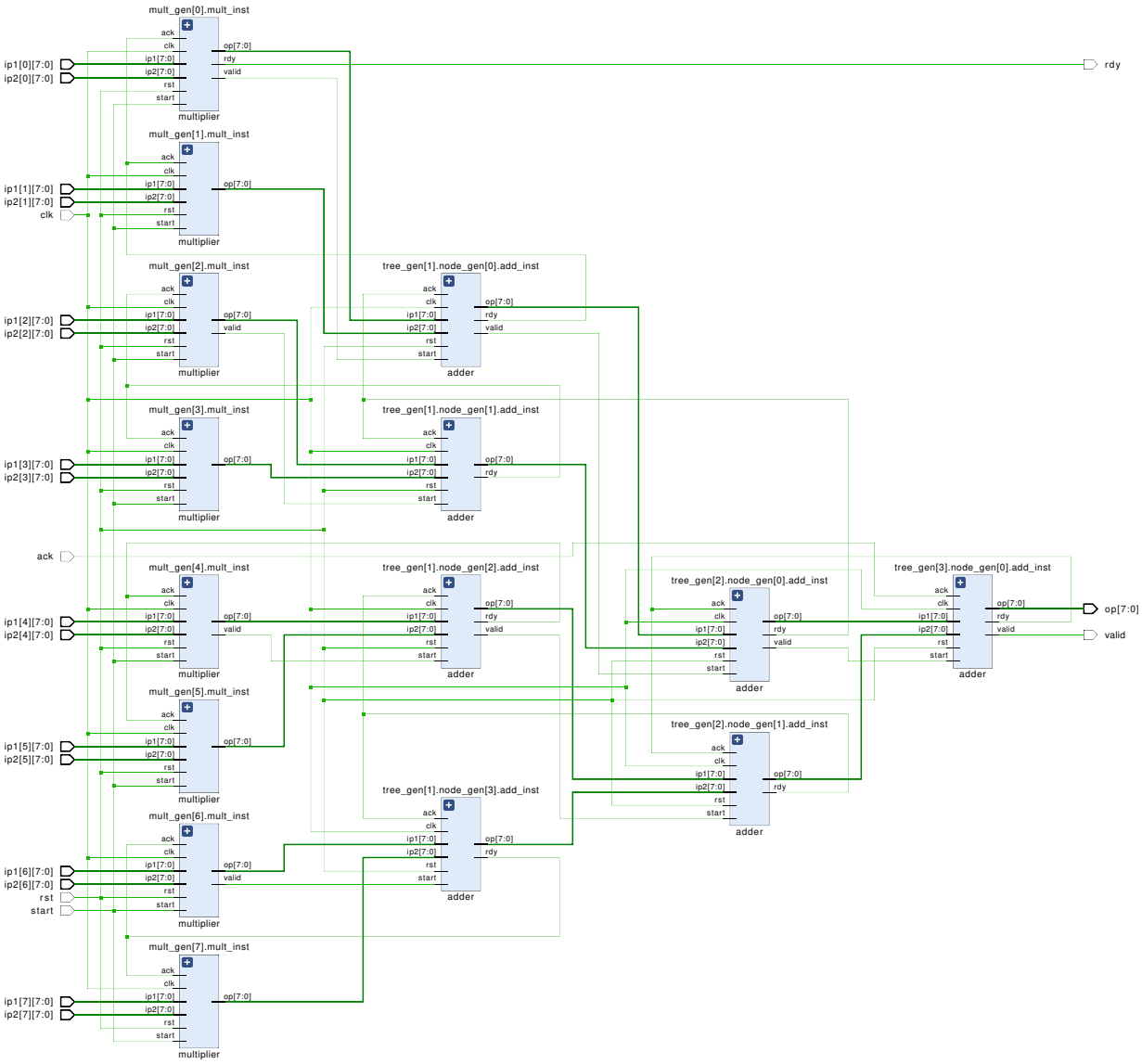

Multiplier schematic



Adder Schematic :




Overall schematic (on next page):


mult_gen[0].mult_inst
ack
clk
ip1[7:0]
ip2[7:0]
rst
start
op[7:0]
rdy
valid
multiplier
ip1[0][7:0]
ip2[0][7:0]
rdy
mult_gen[1].mult_inst
ip1[1][7:0]
ip2[1][7:0]
clk
mult_gen[2].mult_inst
ip1[2][7:0]
ip2[2][7:0]
tree_gen[1].node_gen[0].add_inst
adder
mult_gen[3].mult_inst
ip1[3][7:0]
ip2[3][7:0]
tree_gen[1].node_gen[1].add_inst
ack
mult_gen[4].mult_inst
ip1[4][7:0]
ip2[4][7:0]
tree_gen[1].node_gen[2].add_inst
tree_gen[2].node_gen[0].add_inst
tree_gen[3].node_gen[0].add_inst
op[7:0]
valid
mult_gen[5].mult_inst
ip1[5][7:0]
ip2[5][7:0]
tree_gen[2].node_gen[1].add_inst
tree_gen[1].node_gen[3].add_inst
mult_gen[6].mult_inst
ip1[6][7:0]
ip2[6][7:0]
rst
start
mult_gen[7].mult_inst
ip1[7][7:0]
ip2[7][7:0]

SYNTHESIS Results

## $4 \times 4$ *Matrix Multiplication*

Resource Utilization – 1.2% LUTs utilized

Can fit 80 such dot product units

Hierarchy

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| dp | 173 | 63 | 78 | 1 |

Hierarchy

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| dp | 1.20% | 0.22% | 144.44% | 3.13% |

Timing Summary: Minimum Clock period = 2.1 ns

Create Clock

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File |
|---|---|---|---|---|---|---|---|
| 1 | clk | 2.100 | 0.000 | 1.050 | ☐ | [get_ports clk] | <unsaved cc |

*Double click to create a Create Clock constraint*

**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 0.055 ns | Worst Hold Slack (WHS): | 0.149 ns | Worst Pulse Width Slack (WPWS): | 0.508 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 87 | Total Number of Endpoints: | 87 | Total Number of Endpoints: | 64 |

**All user specified timing constraints are met.**

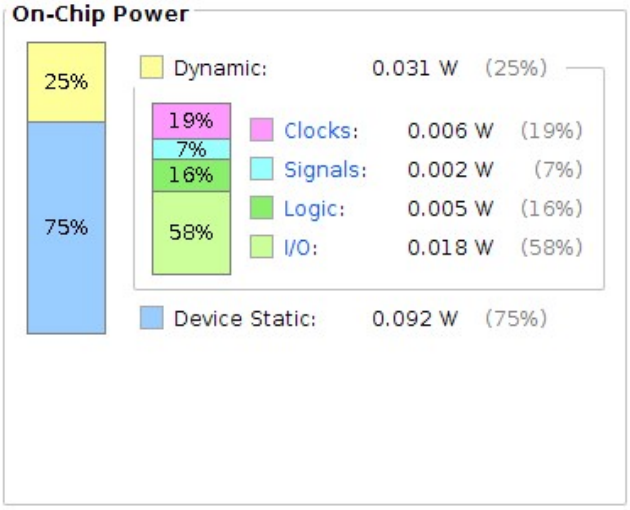
Power Consumption – 0.123 W, dynamic = 0.03 W

## Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

| | |
|---|---|
| **Total On-Chip Power:** | **0.123 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **26.4°C** |
| Thermal Margin: | 73.6°C (6.2 W) |
| Effective θJA: | 11.5°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

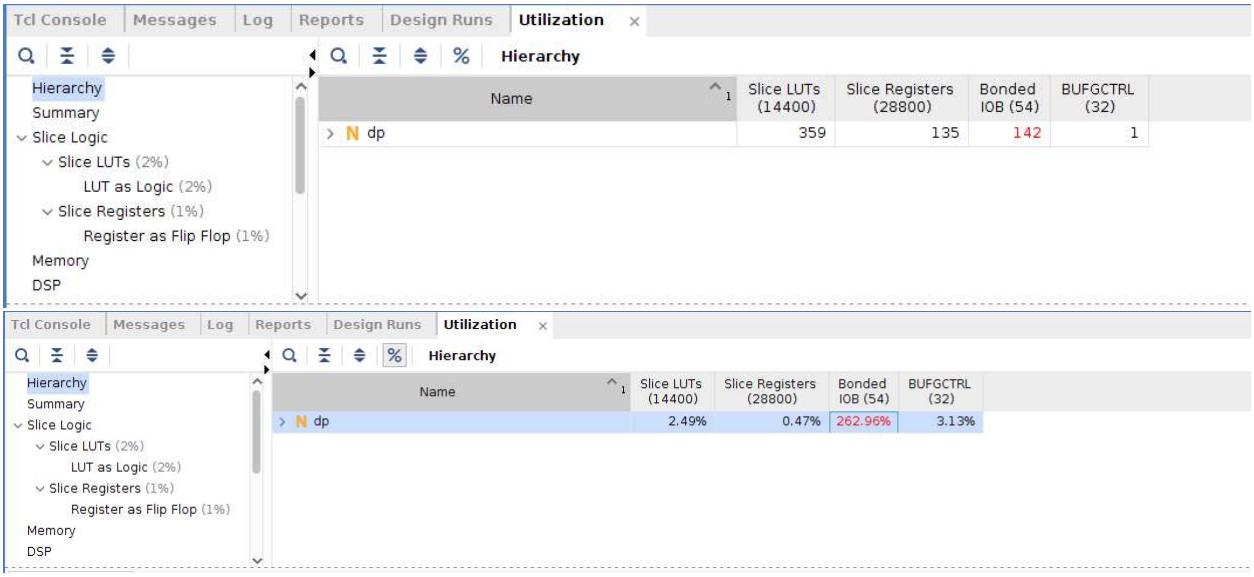
Launch Power Constraint Advisor to find and fix invalid switching activity




# $8 \times 8$ *Matrix Multiplication*

Resource Utilization – 2.5% LUTs utilized

Can fit 40 such dot product computation units




Timing Summary

Create Clock

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File | Scoped Cell | Current Instance |
|---|---|---|---|---|---|---|---|---|---|
| 1 | clk | 2.000 | 0.000 | 1.000 | ☐ | [get_ports clk] | <unsaved cc | | |

*Double click to create a Create Clock constraint*

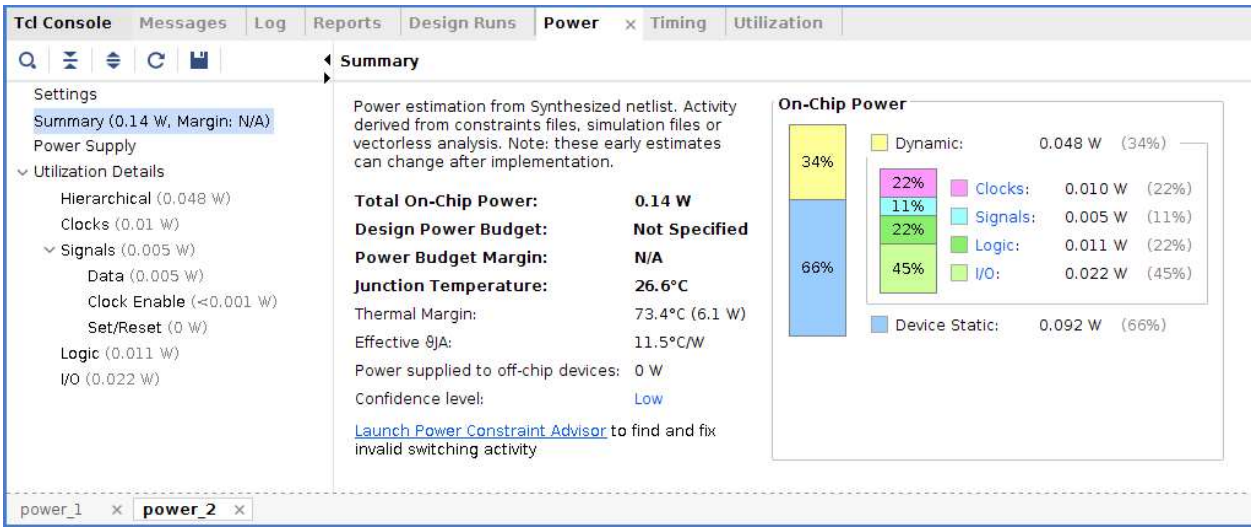
**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | -0.167 ns | Worst Hold Slack (WHS): | 0.147 ns | Worst Pulse Width Slack (WPWS): | 0.408 ns |
| Total Negative Slack (TNS): | -12.013 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 104 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 191 | Total Number of Endpoints: | 191 | Total Number of Endpoints: | 136 |

**Timing constraints are not met.**

Minimum Clock period = 2.17 ns

Power Consumption – 0.14 W, dynamic = 0.05 W




## $16 \times 16$ *Matrix Multiplication*

Resource Utilization – 5.1% LUTs utilized

Can fit 19 such dot product computation units

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| dp | 734 | 279 | 270 | 1 |

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| dp | 5.10% | 0.97% | 500.00% | 3.13% |

## Timing Summary

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File |
|---|---|---|---|---|---|---|---|
| 1 | clk | 2.000 | 0.000 | 1.000 | ☐ | [get_ports clk] | <unsaved cc |

*Double click to create a Create Clock constraint*

**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | -0.539 ns | Worst Hold Slack (WHS): | 0.150 ns | Worst Pulse Width Slack (WPWS): | 0.408 ns |
| Total Negative Slack (TNS): | -81.018 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 232 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 399 | Total Number of Endpoints: | 399 | Total Number of Endpoints: | 280 |

**Timing constraints are not met.**

## Minimum Clock period = 2.54 ns

## Power Consumption – 0.15 W, dynamic = 0.06 W

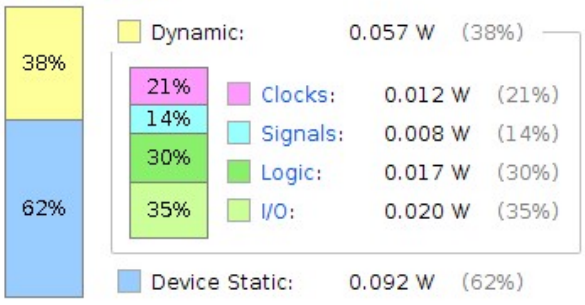
**Summary**

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

| | |
|---|---|
| **Total On-Chip Power:** | **0.149 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **26.7°C** |
| Thermal Margin: | 73.3°C (6.1 W) |
| Effective θJA: | 11.5°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Launch Power Constraint Advisor to find and fix invalid switching activity

**On-Chip Power**




## $32 \times 32$ *Matrix Multiplication*

Resource Utilization – 10.2% LUTs used

Can fit 9 such dot product units

Hierarchy

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| > N dp | 1469 | 567 | 526 | 1 |

Hierarchy

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| > N dp | 10.20% | 1.97% | 974.07% | 3.13% |

Timing Summary: Minimum clock period = 2.66ns

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File |
|---|---|---|---|---|---|---|---|
| 1 | clk | 2.000 | 0.000 | 1.000 | ☐ | [get_ports clk] | <unsaved cc |

*Double click to create a Create Clock constraint*

**Design Timing Summary**

**Setup**

| | |
|---|---|
| Worst Negative Slack (WNS): | -0.658 ns |
| Total Negative Slack (TNS): | -265.162 ns |
| Number of Failing Endpoints: | 520 |
| Total Number of Endpoints: | 815 |

**Hold**

| | |
|---|---|
| Worst Hold Slack (WHS): | 0.155 ns |
| Total Hold Slack (THS): | 0.000 ns |
| Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 815 |

**Pulse Width**

| | |
|---|---|
| Worst Pulse Width Slack (WPWS): | 0.408 ns |
| Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 568 |

**Timing constraints are not met.**

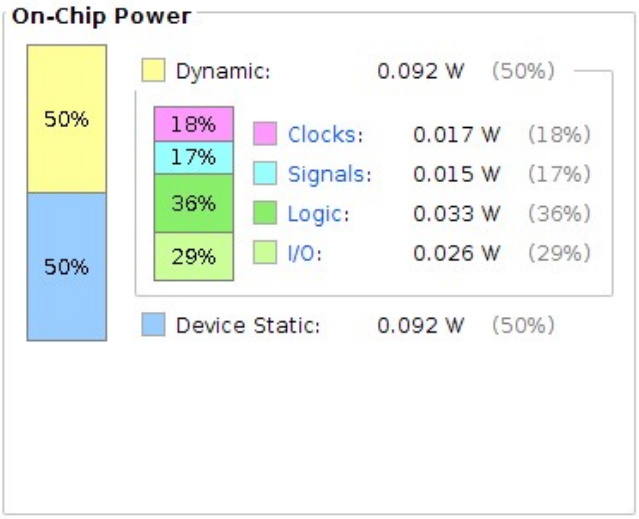
Power Consumption – 0.184W, dynamic = 0.092W

**Summary**

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

| | |
|---|---|
| **Total On-Chip Power:** | **0.184 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **27.1°C** |
| Thermal Margin: | 72.9°C (6.1 W) |
| Effective θJA: | 11.5°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Launch Power Constraint Advisor to find and fix invalid switching activity



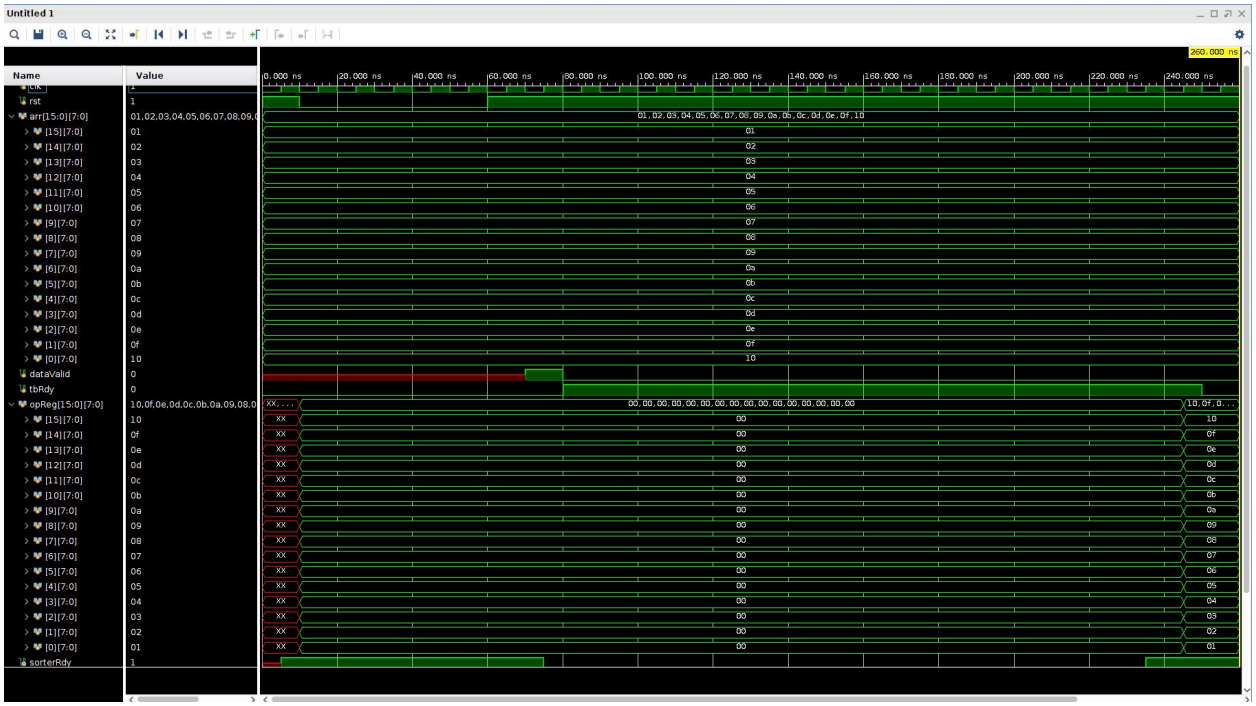

## 2. Odd-Even Transposition Sort

Simulation Results:

Input array is $arr[]$, where $arr[i] = 16 - i$

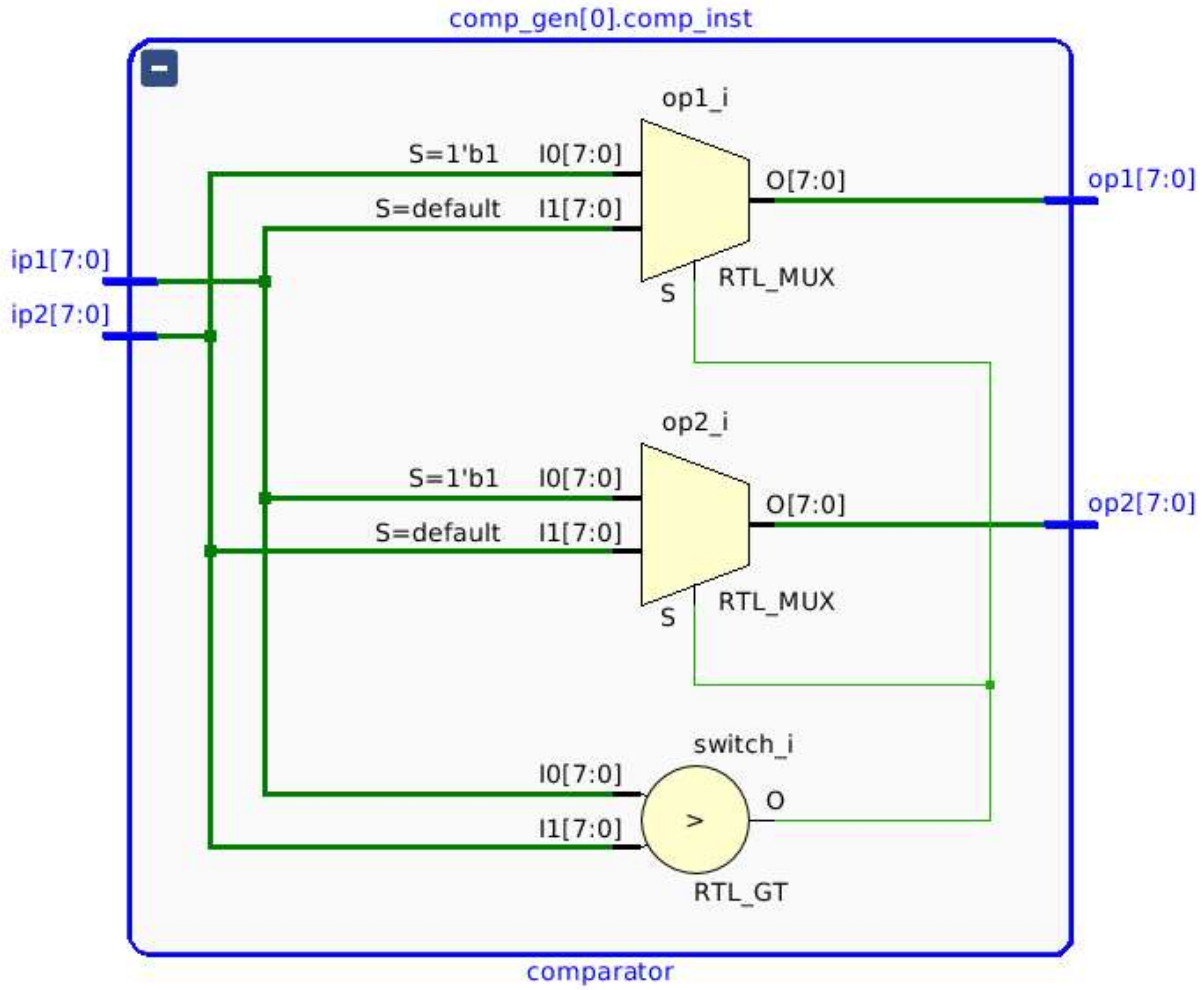
Output array is $opReg[]$ in which the elements are sorted in increasing order.

Number of clocks used to sort 16-elements = 16

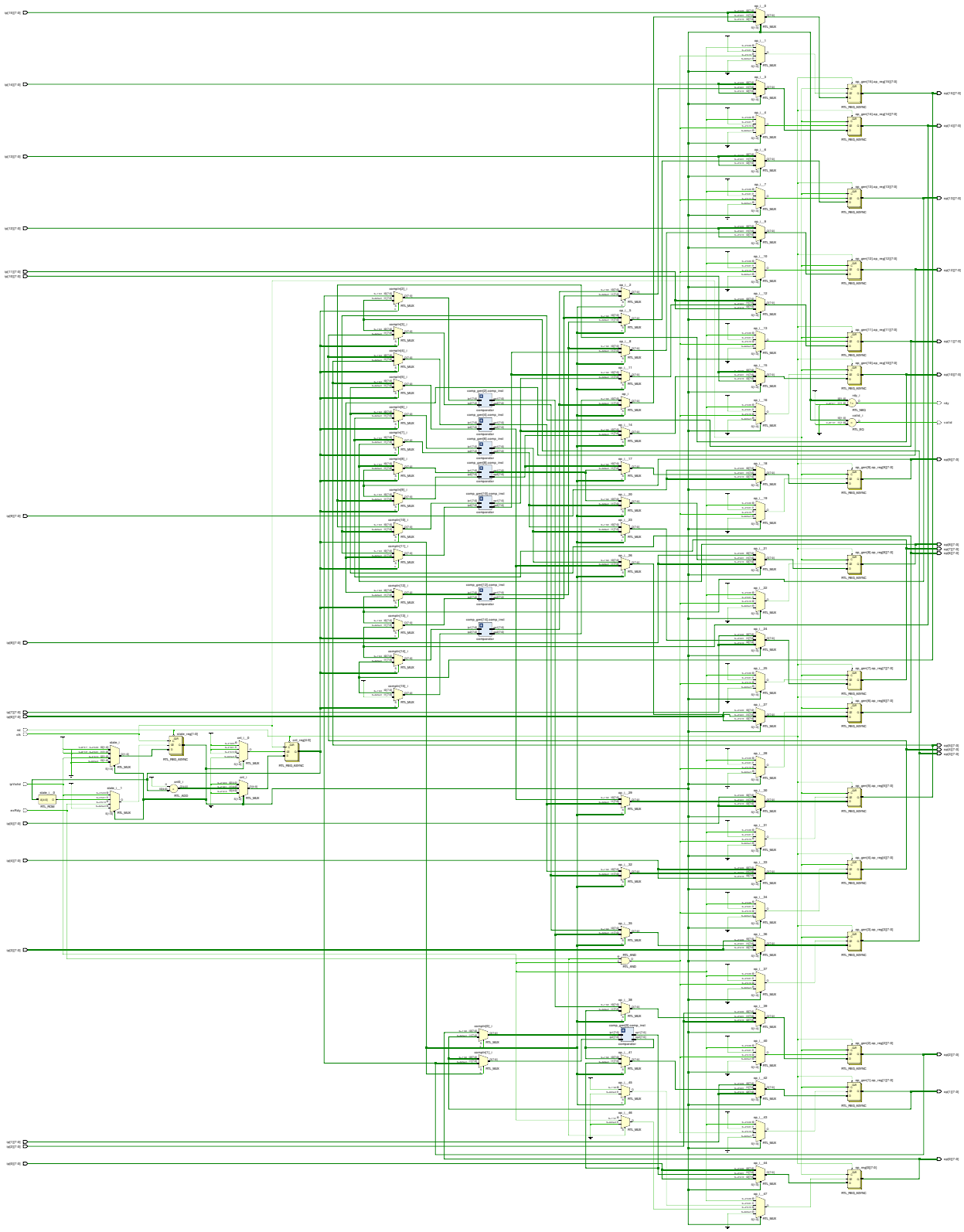



Schematic:

**Comparator**


comp_gen[0].comp_inst
op1_i
S=1'b1
I0[7:0]
S=default
I1[7:0]
O[7:0]
op1[7:0]
ip1[7:0]
ip2[7:0]
S
RTL_MUX
op2_i
S=1'b1
I0[7:0]
S=default
I1[7:0]
O[7:0]
op2[7:0]
S
RTL_MUX
switch_i
I0[7:0]
I1[7:0]
>
O
RTL_GT
comparator

**Full Design:**



**SYNTHESIS RESULTS:**

## $16 - element\ Sorter$

### Resource Utilization – 2.26% of LUTs used

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| > N sort | 326 | 137 | 262 | 1 |

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| > N sort | 2.26% | 0.48% | 485.19% | 3.13% |

### Timing Summary: Minimum clock period = 4.2 ns

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File |
|---|---|---|---|---|---|---|---|
| 1 | clk | 2.000 | 0.000 | 1.000 | ☐ | [get_ports clk] | <unsaved cc |

*Double click to create a Create Clock constraint*

**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | -2.200 ns | Worst Hold Slack (WHS): | 0.176 ns | Worst Pulse Width Slack (WPWS): | 0.408 ns |
| Total Negative Slack (TNS): | -262.828 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 258 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 274 | Total Number of Endpoints: | 274 | Total Number of Endpoints: | 138 |

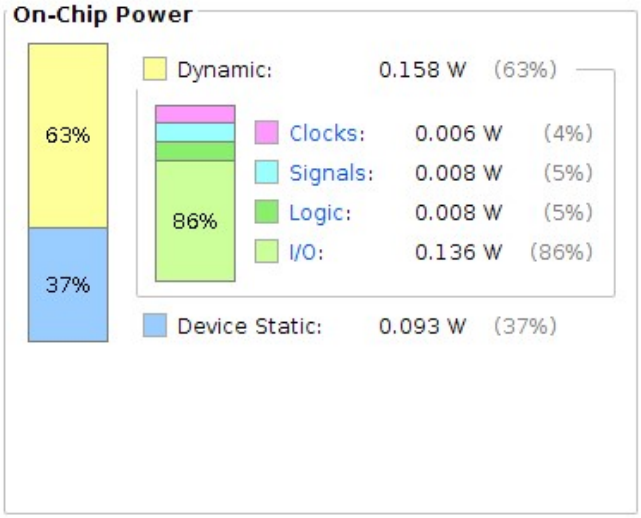
**Timing constraints are not met.**

### Power Consumption: 0.251 W, dynamic power = 0.16 W

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

| | |
|---|---|
| **Total On-Chip Power:** | **0.251 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **27.9°C** |
| Thermal Margin: | 72.1°C (6.0 W) |
| Effective θJA: | 11.5°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Launch Power Constraint Advisor to find and fix invalid switching activity



# $32 - element\ sorter$

## Resource Utilization – 4.3% LUTs used

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| sort | 615 | 264 | 518 | 1 |

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| sort | 4.27% | 0.92% | 959.26% | 3.13% |

## Timing Summary: Minimum clock period = 4.3ns

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File | Scoped Cell | Current Instance |
|---|---|---|---|---|---|---|---|---|---|
| 1 | clk | 4.200 | 0.000 | 2.100 | ☐ | [get_ports clk] | <unsaved cc | | |

*Double click to create a Create Clock constraint*

**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | -0.044 ns | Worst Hold Slack (WHS): | 0.136 ns | Worst Pulse Width Slack (WPWS): | 1.600 ns |
| Total Negative Slack (TNS): | -1.521 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 240 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 528 | Total Number of Endpoints: | 528 | Total Number of Endpoints: | 265 |

**Timing constraints are not met.**

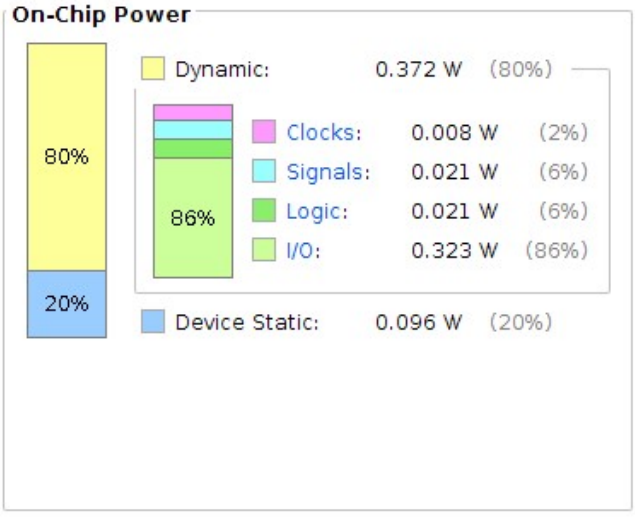
## Power Consumption: 0.47W, dynamic = 0.37W

**Summary**

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

| | |
|---|---|
| **Total On-Chip Power:** | **0.468 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **30.4°C** |
| Thermal Margin: | 69.6°C (5.8 W) |
| Effective θJA: | 11.5°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Launch Power Constraint Advisor to find and fix invalid switching activity



# 64 – element Sorter

## Resource Utilization – 9.9% LUTs used

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| N sort | 1419 | 539 | 1030 | 1 |

| Name | Slice LUTs (14400) | Slice Registers (28800) | Bonded IOB (54) | BUFGCTRL (32) |
|---|---|---|---|---|
| N sort | 9.85% | 1.87% | 1907.41% | 3.13% |

## Timing Summary: Minimum clock period = 4.3 ns

**Design Timing Summary**

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | -0.216 ns | Worst Hold Slack (WHS): | 0.136 ns | Worst Pulse Width Slack (WPWS): | 1.500 ns |
| Total Negative Slack (TNS): | -98.846 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 496 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 1078 | Total Number of Endpoints: | 1078 | Total Number of Endpoints: | 540 |

**Timing constraints are not met.**

| Position | Clock Name | Period (ns) | Rise At (ns) | Fall At (ns) | Add Clock | Source Objects | Source File |
|---|---|---|---|---|---|---|---|
| 1 | clk | 4.000 | 0.000 | 2.000 | ☐ | [get_ports clk] | <unsaved cc |

*Double click to create a Create Clock constraint*

## Power Consumption: 0.76 W, dynamic = 0.66 W

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

| | |
|---|---|
| **Total On-Chip Power:** | **0.759 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **33.7°C** |
| Thermal Margin: | 66.3°C (5.5 W) |
| Effective θJA: | 11.5°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Launch Power Constraint Advisor to find and fix invalid switching activity