Simulation Configuration : Non-Fusion Based Coherent Cache Randomization Using Cross-Domain Accesses

ZSim Simulator Configuration	
Core	OOO core configured similar to a Nehalem architecture
L1D Cache	32 KB, 8-way associative, 4 cycle latency, LRU (least-recently-used) replacement policy
L1I Cache	32 KB, 4-way associative, 4 cycle latency, LRU
L2 Cache	256 KB, 8-way associative, 10 cycle latency, LRU
L3 Cache	2MB slice per core, 16-way associative, 42 cycle latency, Random Replacement Policy
Main Memory	150 cycle latency

Table 1: Simulation Configuration