4-bit ALU Project Report

Student Information

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Project Title

4-bit Arithmetic Logic Unit (ALU) Design using Verilog HDL

Objective

To design and simulate a 4-bit ALU using Verilog HDL that performs basic arithmetic and logical operations such as addition, subtraction, AND, OR, NOT, XOR, left shift, and right shift.

Tools Used

- Verilog HDL
- EDA Playground (online simulator)
- Testbench for simulation

Project Description

The ALU is designed to take two 4-bit binary inputs (A and B) and a 3-bit opcode to determine the operation to be performed. The operations include:

000 - Addition

001 - Subtraction

010 - AND

011 - OR

100 - NOT A

101 - XOR

4-bit ALU Project Report

110 - Right Shift A

111 - Left Shift A

The design was implemented using a case statement inside an always block. The output of each operation is assigned to the 'Result' register.

Conclusion

This project helped in understanding the basics of Verilog coding, combinational logic design, and simulation of digital systems. It provides a foundation for more complex VLSI-based designs.