

Compressor based Low-Power and High-Speed Approximate Multipliers using Pass-Transistor Logic

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Abstract

Approximative 4:2 compressors are built using pass transistor logic, which allows the system to use significantly fewer transistors than traditional systems. These optimizations enable the design to be compact and highly efficient while at the same time, decreasing total power, area, and computational delay. The use of 4:2 compressors provides a new approach where the multiplier can achieve error-tolerant calculations, which is a significant limitation for modern multipliers in DSP, machine learning, and image processing. The design approaches the challenges of power and area-sensitive applications using pass-transistor logic and carefully balancing performance and resource trade-offs. In addition, the proposed architecture demonstrates its relevance for resource-constrained systems, gaining speed and energy efficiency without degrading overall system functionality. The design has been implemented and analyzed using Cadence Virtuoso with gpdk 180 nm CMOS technology, which provides quantitative insight into the design's performance indicators. This method achieves more than the previously established multiplier architectures in power and area efficiency.

Index Terms

Approximate computing, compressor, multiplier, pass-transistor logic

I. INTRODUCTION

The conceptual framework refers to an upcoming computing paradigm called Approximate Computing which willingly compromises on accuracy for improved performance, resource utilization,

and enhanced energy efficiency. The technique performs well on certain applications such as image processing, machine learning, and data analysis where precise answers are not critical. Approximate computing allows a small margin of error in calculations, resulting in lower power consumption, faster processing times, and simplified hardware architecture. Such characteristics make it ideal for error-tolerant and resource limited systems. Because of these advantages, approximation computing has gained popularity as one of the most important elements in modern circuit design, especially for high-speed and energy-efficient designs for applications in edge computing and IoT devices [1]–[4].

In the context of digital computation, a device used for multiplication is called a compressor, which is a widely utilized fundamental combinatorial circuits that reduces the summation of the partial products generated during the multiplication process [5]–[9]. It reduces the number of binary inputs in multipliers to add the partial products by outputting fewer binary signals. 4:2 compressors are unique among all other classes of compressors due to their great efficiency. They take four main inputs and one carry-in signal as well as produce two outputs : one is a carry, the other is a sum. Moreover, it also provides a carry-out signal that can be used in subsequent stages. The ease with which these operations are performed makes multipliers and even other arithmetic units in digital systems more efficient.

One of the most important digital circuits is a multiplier, which is designed to multiply binary numbers. The process is carried out by generating partial products using binary multiplication and adding them together to give the final result. These devices, known as multipliers, are widely used in image processing, cryptography, digital signal processing, and artificial intelligence [6]. Multiplier design and optimization are crucial to the high performance and efficiency of modern computer systems.

This type of architecture referred to as a 4x4 multiplier, creates an 8-bit output when two binary inputs of 4 bit are multiplied. To efficiently utilize the potential of the multiplier, 16 separate products are multiplied and later summed through compressors and/or adders. In normal 4x4 multipliers, full adders and half adders add the separate products. However, while effective, this more simple methodology can be resource heavy in terms of calculation time, area on the chip, and energy consumption.

The proposed topology replaces the usual full adders [10] with the 4:2 compressors. They were constructed with pass-transistor logic that greatly reduces the number of transistors needed compared to standard implementations of logic gates [11]. By the incorporation of these principles,

the design shows improvement in power, area, and delay performance metrics as a result of a lower number of transistors. This approach not only improves the efficiency of the multiplier, but also makes it more suitable for tight compact and low power applications. The several benefits of pass-transistor logic afford a more efficient circuit design, which is a better solution to the powerful but resource-limited systems.

The rest of the paper is organized as follows: Section II includes a review on the literature of 4:2 compressors and their applications. Section III describes the methodology adopted to design the proposed 4:2 compressors and 4x4 multipliers using the proposed compressors. Section IV discusses the Error Rate, Truth Table, Circuit Diagrams, and Simulation Results in detail. At last, Section V discusses the conclusion of the proposed designs.

II. LITERATURE SURVEY

This section includes a review on the literature of 4:2 compressors and their effect in low-power multipliers. The paper examines various designs from the standpoint of performance, latency, and resource consumption. The results lay the groundwork for the improvement of computational circuits in low power applications.

A. Compressor Construction with Pass Transistors

The increase in the usage of multimedia systems with drastically higher multipliers has posed a new challenge in power management of digital systems. In the area of partial product summation for multipliers, type 3:2, 4:2, and 5:2 compressors are for example multivariate – which are crucial. Studies have been conducted on the design of different compressors with multiplexers and XOR-XNOR gates built with PTL(pass transistor logics). These technologies are very suitable in the low-power range since they improve reduced transistor count, power use, and latency. For instance, Wallace tree multiplier 8x8 with PTL based compressors achieved power savings comparably to traditional designs of Wallace trees. [14] There are other compressor based designs discussed in [11]–[13]. Here the focus has been made to make these compressors fast and low energy consuming with decreased delay.

For the 5:2 compressor which is fast and low-power efficient, a set truth table and combination of pass transistors with static logics were employed. The design also reduces internal driving capacitance which resulted in less power dissipation and glitches. The results showed a timer with a lower latency and the absence of glitches. The use of TSMC 0.18 μm CMOS technology

also resulted in superior outcomes compared to conventional methods with 302 ps latency and 248.62 μ W power dissipation. [14]

In the same manner, adjustable truth tables and PTL were utilized to demonstrate a low-power 4:2 compressor. There was less power consumption and active area because there were fewer transistors in this design. Simulations executed with a 32 nm channel in CNTFET technology outperformed CMOS based designs. The total number of transistors for the proposed design was 58, the least number of transistors reported in the literature for 4:2 compressors. [15]

Along with cryptography and DSP, communication systems have become an integral part requiring advanced digital circuits for which the digital multipliers must be efficient. Due to a 5:2 compressor built using approximation logic and PTL, higher-order multipliers and filters performed better because power and delay were reduced. This design demonstrated the benefits of approximation logic in PTL-based compressors in high performance by achieving 98.4% speed improvement and 78.04% power efficiency improvement. [16]

Finally, two 3:2 compressor architectures were proposed which are speed optimized and power efficient based on PTL multiplexers and XOR-XNORs. This has been proved when comparing the PTL based multiplexers with the transmission gate. The performance boost which included reduced energy-delay product, delay, and power dissipation was also confirmed in simulations with 10 nm CNTFET and 45 nm CMOS technology. This achievement demonstrates the application of PTL in designing low-power high performance compressors for modern VLSI systems. [17]

B. Exact 4:2 Compressor

An exact 4:2 compressor provides the high level of precision and accuracy required in image processing, scientific computation, and even cryptography. The 4:2 is an essential part of the mathematical and engineering worlds because it does not omit any information and ensures correctness in the computational results. The 4:2 compressor does carry the power to increase the computation efficiency, specifically within the digital signal processing and computer systems on top of which it operates like a logic circuit with a single compression arithmetic operation: addition and enables two carry inputs, and four bits of the input into two bits [11]–[13], [18]–[20]. In literature various researchers have designed compressors using advanced nanodevices like FinFET and CNTFETs (Carbon Nano Tube FET).

The architecture of a typical 4:2 compressor uses XOR, AND, and OR gates as fundamental

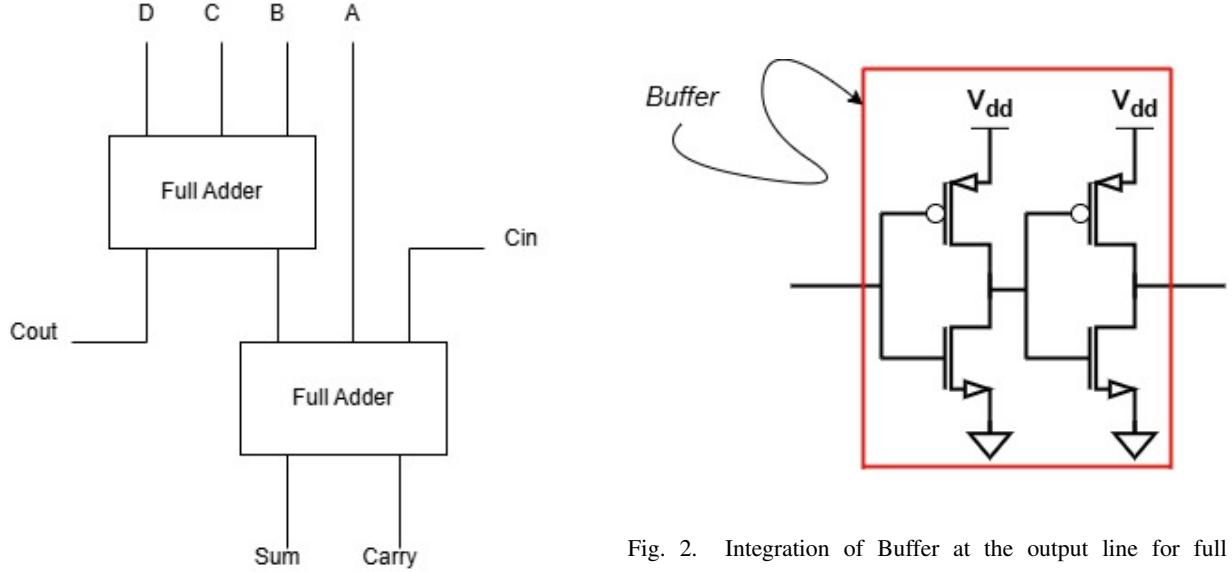


Fig. 1. Block Diagram of an exact 4:2 compressor.

logic components, which are basic operations at the bit level. The ability of this compressor to operate without the carry-in input is a major advantage because it allows parallelism in arithmetic operations and thus enhances processing efficiency. High-performance digital systems also target low power consumption and delay. Its architecture can be embedded in larger systems for example Dadda multipliers [21] or Wallace trees enhancing the efficiency of binary multiplication processes making it a fundamentally important piece of modern digital electronics.

III. METHODOLOGY

This section discusses the methods adopted to design the proposed compressors and multipliers.

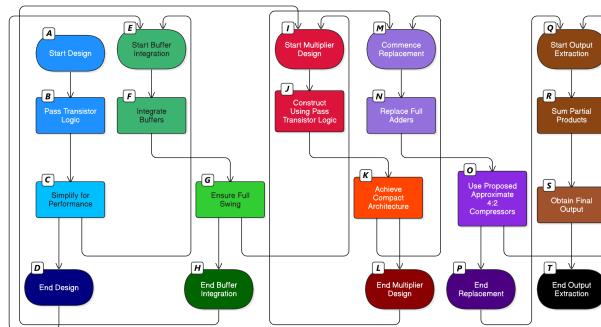


Fig. 3. A summarized block diagram representing the steps involved implementing the circuits.

A. Approximate 4:2 Compressor with Input-Based Carry Generation Employing Pass Transistors

In Design 1 of the approximate 4:2 compressor shown in figure 4, pass transistor logic is employed. The main inputs are four: A, B, C, and D. To make approximations, Carry-in (C_{in}) and Carry-out (C_{out}) have been neglected. This focuses on the Sum output and the Carry output. The simplified Boolean equation will suffice for designing the sum:

$$Sum = (A \oplus B) + (C \oplus D) \quad (1)$$

Only 4 errors out of 16 cases are achieved in the output sum using this technique. A different pass-transistor logic design used for the carry that relies only on input lines A, B, C, and D. These assumptions give 1 error out of 16 cases in the carry output. A buffer is placed before the output of both sum and carry, which is done with two inverters, to ensure a full threshold swing and stable outputs. This architecture uses more transistors for buffering but still gives good compression with faults.

B. Approximate 4:2 compressor with output-based carry generation using pass transistors.

The Design 2 shown in figure 5 has the same structure as the first, but uses a different method to implement the carry-out. However, the sum is still defined by the same equation:

$$Sum = (A \oplus B) + (C \oplus D) \quad (2)$$

Instead, the carry is taken from the output of the intermediate XOR, i.e., $A \oplus B$ and $C \oplus D$. This modification would increase the total errors in carry output to 2 out of 16. Only, two inverters are used again to buffer the outputs for good signal integrity and full threshold swing. This technique preserves the transistors at a low level and also reduces the carry output errors.

C. Approximate 4:2 compressor with Inverted outputs

The Design 3 shown in figure 6 combines the second design's method with identical approximations and simplifications for sum and carry calculations. The architecture of this design eliminates separate buffers by introducing inverted sum and carry outputs. Instead of using a buffer with two inverters per output, only one inverter is used for sum and carry calculations. This change significantly reduces the transistor count while the error count is same as the Design

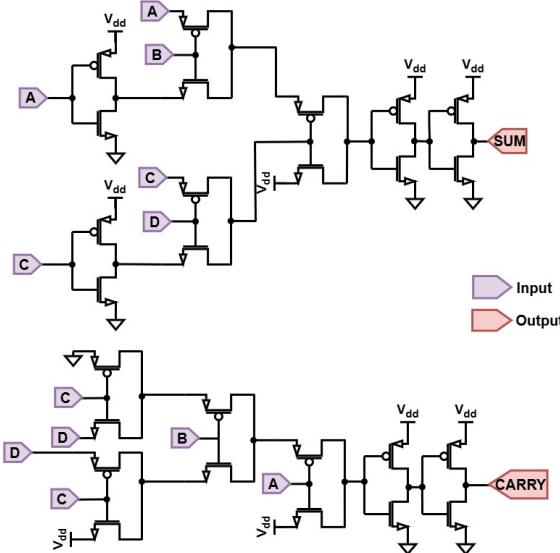


Fig. 4. Schematic diagram of design 1 for proposed approximate 4:2 compressor.

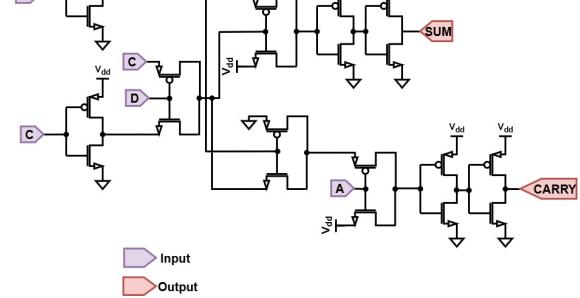


Fig. 5. Schematic diagram of design 2 for proposed approximate 4:2 compressor.

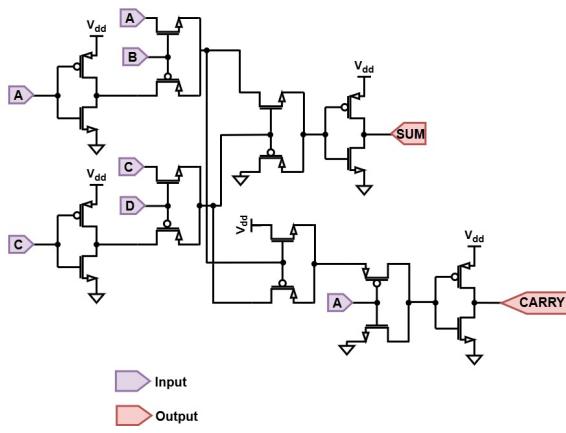


Fig. 6. Schematic diagram of design 3 for proposed approximate 4:2 compressor.

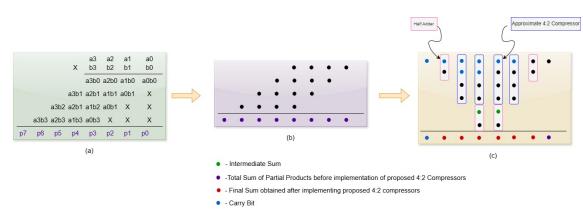


Fig. 7. (a) Partial product matrix of a 4x4 bit Multiplier. (b) Each partial product represented with a dot. (c) Reduction of partial products in 4x4 Multiplier using proposed designs of 4:2 compressors and Half Adder.

2. The inverted output is intended to reduce hardware complexity and achieve signal integrity. This architecture shows how it is possible to balance the need for inverted signal processing in downstream applications with the need for reduced transistor count.

D. Multiplier Design:

The 4x4 multiplier architecture uses pass-transistor logic and a 4:2 compressor to maximize hardware resource utilization, reduce power consumption, and save space. The multiplier generates 16 partial products from two 4-bit binary values $A=a_3a_2a_1a_0$ and $B=b_3b_2b_1b_0$. To simplify the summation stage by reducing the bit width and adding controlled approximation errors, proposed approximate 4:2 compressors are used instead of a traditional adder to sum the partial products. This has been shown in Figure 7. 4:2 compressors process partial products as they are created, producing intermediate results that are then further processed by other compressors or adders to produce the final 8-bit product. They balance output accuracy and hardware efficiency by evaluating inaccuracies caused by approximations. Assessing the multiplier performance against traditional devices requires evaluations of power consumption and area usage, as well as latency and error rates. The method of combining pass transistors with neighboring compressors produces a highly efficient 4x4 multiplier designed for high-performance low-power applications where precision is secondary.

IV. RESULTS AND DISCUSSION

A. Error Rate and Outputs of Proposed Compressor Designs and 4x4 Multiplier

In relation to a ‘perfect’ 4:2 compressor, the outcomes from the first design of the 4:2 compressor, Sec.III-A, has a total of four errors in the Sum and one error in the Carry out of 16 cases. On the other hand, the design 2 and design 3 in Sec.III-B and Sec.III-C respectively, have two errors in Carry and four errors in the Sum out of 16 cases. The 4:2 compressor produces 16 cases in total. The corresponding error estimations were calculated for those cases as well. The error rate is calculated using the formula:

$$\text{Error} = (\text{Total Number of Errors} / \text{Total Number of Outputs}) \quad (3)$$

The design proposed in Sec.III-A, for the Sum, error rate is evaluated as $4/16 = 0.25$, and for the Carry, the error rate is $1/16 = 0.0625$. In Sec.III-B and Sec.III-C, for the Sum, error rate is the same and previous design, but for the Carry, the error rate is $3/16 = 0.1875$.

B. Truth Table

This section introduces the Truth Table I for Design 1,2 and 3 for the proposed 4:2 Approximate Compressors and Table II for 4x4 Multiplier made using the proposed compressor designs.

TABLE I

TRUTH TABLE OF EXACT 4:2 APPROXIMATE COMPRESSOR
AND THE DESIGN 1, 2, AND 3 PROPOSED IN THIS REPORT.
THE INACCURATE OUTPUTS ARE MARKED IN RED.

Input		Exact		Design 1		Design 2		Design 3	
A	B	C	D	Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	1	1	0
0	0	1	0	1	0	1	0	1	0
0	0	1	0	0	1	0	1	0	0
0	0	1	1	1	0	0	0	0	0
0	1	0	0	1	0	1	0	1	0
0	1	0	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	0	1	0

TABLE II

TRUTH TABLE OF OUTPUTS p_7 (MSB) TO p_0 (LSB) OF 4x4
MULTIPLIER USING PROPOSED COMPRESSOR DESIGNS.

Inputs										Outputs					
a3	a2	a1	a0	b3	b2	b1	b0	p7	p6	p5	p4	p3	p2	p1	p0
0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1	0	1	1	1	1	1	0	1
0	1	1	0	1	0	1	1	0	1	1	0	0	1	1	0
0	1	1	1	1	0	1	1	0	1	1	1	0	1	0	1
1	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0
1	0	0	1	1	0	1	1	0	1	1	1	0	0	1	1
1	0	1	0	1	0	1	1	1	0	0	1	1	1	0	0
1	1	0	0	1	0	1	1	1	1	1	1	0	0	0	1
1	1	0	1	1	0	1	1	1	0	1	0	0	0	0	1
1	1	1	0	1	0	1	1	1	1	1	0	1	0	1	0
1	1	1	1	1	0	1	1	0	1	1	1	0	1	1	0

C. Circuit Diagrams of 4x4 Multiplier using Proposed Compressors

In Figure 8, the first factors of the product are computed using pass-transistor logic. In arithmetic processing, these products are partial and serve as intermediate signal input operands for compressors and half adders. Such intermediate signals are structured and marked as Type-I input so that confusion and differentiation are mitigated within the system. In Figure 9, a block diagram has been shown of 4x4 Multipiler.

D. Simulation Results

The electrical performance metrics, such as power consumption, propagation delay, and transistor count of the suggested approximate 4:2 compressors are shown in Table III. Cadence Virtuoso has been used to calculate the power consumption, latency, and transistor count for Designs 1, 2, and 3. A comparison of different architectures is given in the table, which also highlights differences in hardware complexity, speed, and power depending on the number of transistors.

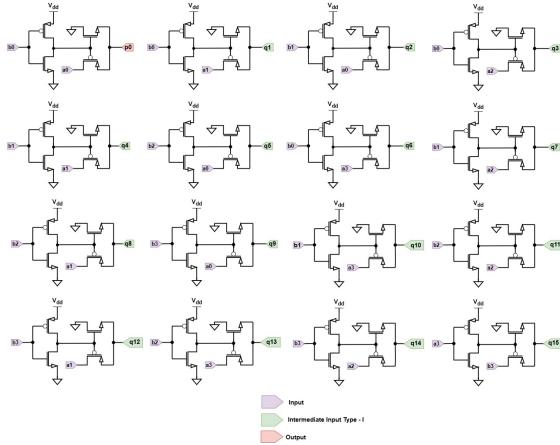


Fig. 8. Partial Products using Pass Transistor Logic for 4x4 Multiplier. Each input of circuit is shown in purple. Each output is termed as Intermediate Input Type - I shown in green except partial product p_0 which is shown in pink.

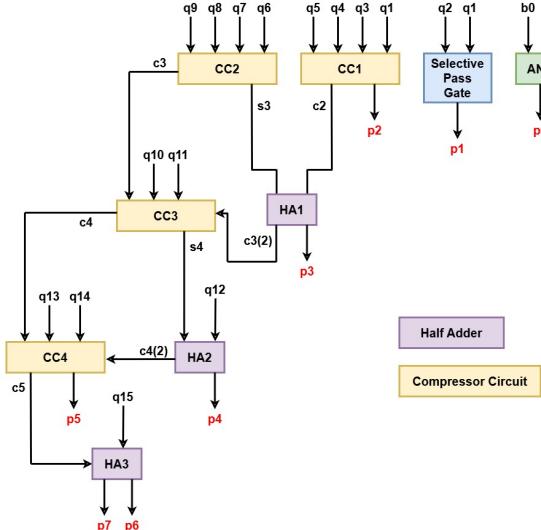


Fig. 9. Block Diagram of 4x4 Multiplier using proposed compressors. The partial products p_0 to p_7 are evaluated using AND Gate block, Selective Pass Gate block, proposed Compressor Circuit blocks and Half Adder blocks. Inputs q_1 to q_{15} shown in Fig.8 are used. The carry bits c_2 , c_3 , $c_3(2)$, c_4 , $c_4(2)$ and c_5 , and the intermediate output bits s_3 and s_4 , are further used as inputs for the Compressor Circuits and Half Adders.

Table IV shows the electrical performance characteristics of the 4x4 multiplier constructed with the recommended approximate 4:2 compressor, including power consumption, propagation delay, and transistor count. The power consumption, delay, and transistor count for Designs 1, 2, and 3 have been determined using Cadence Virtuoso. The table presents a comparison of various architectures, emphasizing variations in the complexity, speed, and power of hardware based on transistor count. An alternate version of Tables III and IV shown in Figures 10, 11 and 12, offering a different viewpoint or data arrangement to help with comparison and improve comprehension of the results.

The output graph generated by Cadence Virtuoso for the suggested 4:2 compressor and the selective output for the 4x4 multiplier is shown in Figure 13, 14, 15, 16, 17 and 18. The compressor takes 80 milliseconds to transition. The transition time for the 4x4 multiplier is 1280 ms; however, the duration is scaled from 0.9 to 1.0 s for a better graph presentation.

Figures 14, 16, and 18 show notable spikes in the graph, which are primarily caused by delay

TABLE III
ELECTRICAL PERFORMANCE OF 4X4 MULTIPLIER USING PROPOSED APPROXIMATE 4:2 COMPRESSORS.
CALCULATIONS FOR POWER AND DELAY HAVE BEEN MADE USING A 1.8 V SUPPLY VOLTAGE.

Proposed Compressor	Power (nW)	Delay (μsec)	Transistors Used
Design 1	840.558	3.71084	26
Design 2	843.914	3.99872	22
Design 3	550.816	2.89236	18

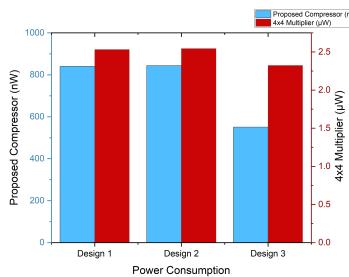


Fig. 10. Power Consumption Analysis of designs in Table III and Table IV.

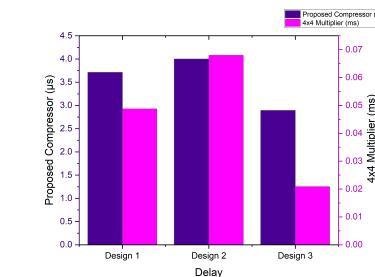


Fig. 11. Delay Analysis of designs in Table III and Table IV.

TABLE IV
ELECTRICAL PERFORMANCE OF PROPOSED APPROXIMATE 4:2 COMPRESSORS. CALCULATIONS FOR POWER AND DELAY HAVE BEEN MADE USING A 1.8 V SUPPLY VOLTAGE.

4x4 Multiplier	Power (μW)	Delay (ms)	Transistors Used
Design 1	2.53099	0.0488057	200
Design 2	2.54401	0.0679656	184
Design 3	2.3235	0.0208823	164

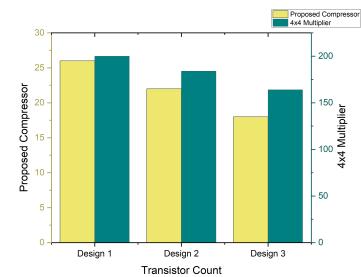


Fig. 12. Transistor Count Analysis of designs in Table III and Table IV.

issues arising from certain inputs. When there are many intermediate inputs, the delay problem becomes significantly more challenging and time-consuming to resolve. The spikes suggest that some system stages are not functioning at their best, and correcting these delays necessitates meticulous input signal tuning—a tedious procedure. Additionally, the output signals in Figures 17 and 18 exhibit discernible aberrations. The particular building technique employed in Design 3 (Section III-C) is the cause of these aberrations. In this architecture, inverted outputs are obtained directly and then routed through an inverter, eliminating the conventional usage of buffers. While this approach reduces complexity and component count, it also has its limitations. These distortions can be caused by the output not quite reaching the correct voltage level because the threshold change is smaller after eliminating the buffer. This compromise in the design approach severely affects the quality of the output and performance of the system.

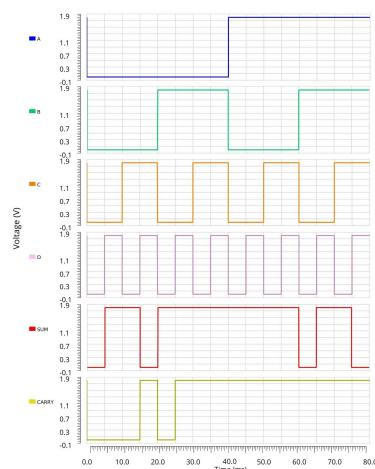


Fig. 13. Output Graph of Design 1 of the Approximate 4:2 Compressor

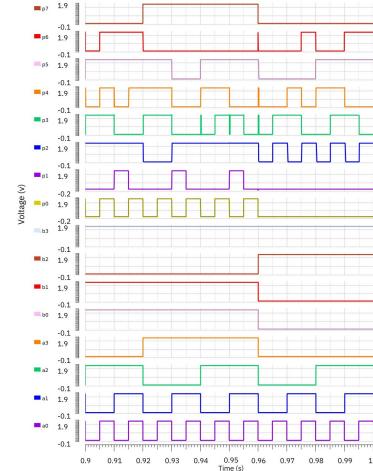


Fig. 14. Output Graph of a 4x4 Multiplier Implemented Using Design 1 of the Approximate 4:2 Compressor

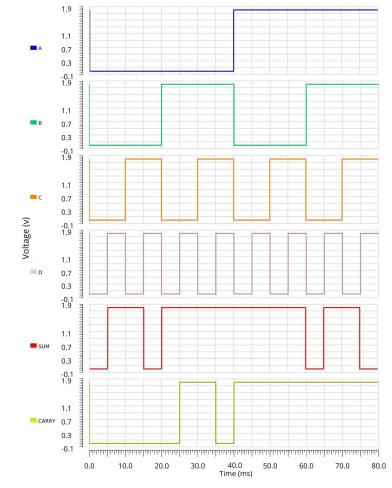


Fig. 15. Output Graph of Design 2 of the Approximate 4:2 Compressor

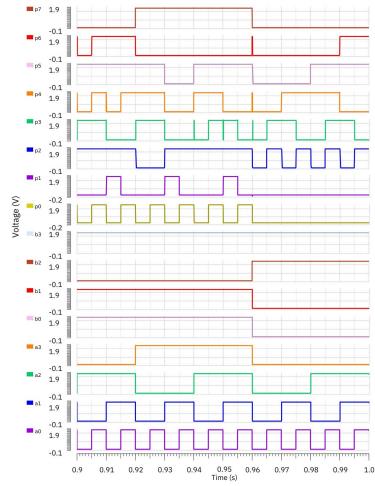


Fig. 16. Output Graph of a 4x4 Multiplier Implemented Using Design 2 of the Approximate 4:2 Compressor

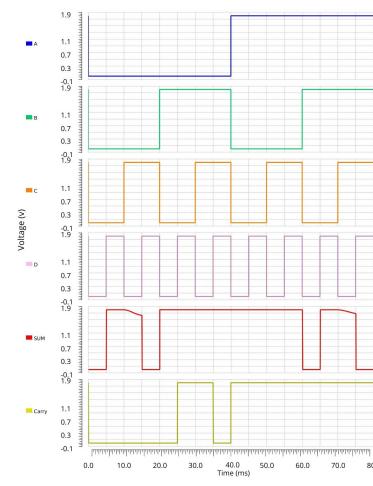


Fig. 17. Output Graph of Design 3 of the Approximate 4:2 Compressor

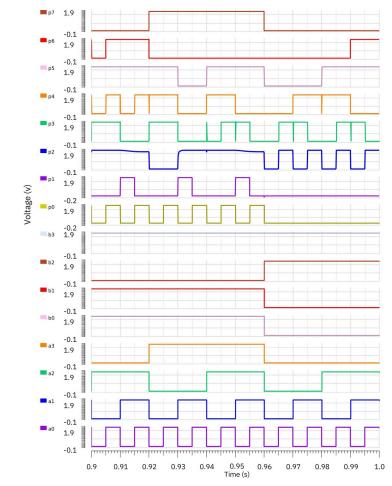


Fig. 18. Output Graph of a 4x4 Multiplier Implemented Using Design 3 of the Approximate 4:2 Compressor

V. CONCLUSION

This study develops a novel 4x4 multiplier architecture by creating a 4:2 approximate compressor using pass-transistor logic. The proposed design significantly reduces the number of transistors by replacing the traditional full adders with these compressors, thereby improving computational latency, power consumption, and area efficiency. The multiplier is well suited for power- and space-sensitive applications such as DSP, machine learning, and image processing, as it uses

approximate computing concepts to perform error-tolerant computations.

Design 3 is the most efficient, with the lowest power consumption (550.816 nW), shortest delay (2.89236 μ s), and fewest transistors (18) of the about 4:2 compressors analyzed in Table 3. In contrast, Designs 1 and 2 are less suitable for low-power applications due to their larger delays and higher power consumption (840.558 nW and 843.914 nW, respectively). Design 3's fewer transistors imply a more hardware-efficient architecture, which is beneficial for systems with limited energy. The superiority of Design 3, which attains the lowest power consumption (2.3235 μ W), shortest delay (0.028823 ms), and reduced transistor count (164), is further supported by the 4x4 multiplier evaluation in Table 4. Design 1's somewhat larger latency and transistor count suggest a less effective trade-off, even if it uses a little less power than Design 2. Since Design 3 almost invariably provides the best combination of speed, energy consumption, and hardware complexity, it is an excellent candidate for energy-saving computing circuits.

The impacts of three different 4:2 compressors on power, area, and error values were analyzed. Four errors in the sum output and one error in the carry output are produced by the first compressor design that uses input-based carry generation. This leads to a 25% (4/16) error rate for the sum and a 6.25% (1/16) error rate for the carry. The second design, which employs output-based carry generation, exhibits a decrease in carry errors while maintaining the same cumulative error rate. Specifically, the cumulative error rate stays at 25% (4/16), but the carry error rate rises to 18.75% (3/16). Similar to the second design, the third design minimizes the number of transistors without adding more errors by optimizing the buffering mechanism. Because this design is not efficient, it is ideal for new computing models like edge computing or the IoT. Further study can be about improved designs of compressors and their applicability in large-scale multiplier circuits, and effectiveness of tolerating faults versus performance.

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Authors' contributions

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There are no linked research data sets for this submission.

Declarations

Conflict of interests

The authors declare no competing interests.

Ethics approval and consent to participate

Informed consent was obtained from all individual participants included in the study.

Consent for publication

Informed consent was obtained from all individual participants included in the study.

Disclosure of potential conflicts of interest

The authors declare that they have no conflict of interest. Research involving Human Participants and/or Animals All procedures performed in this study involving human participants were in accordance with the ethical standards of the institutional and/or national research committee and with the 1964 Helsinki declaration and its later amendments or comparable ethical standards.

Informed consent

Informed consent was obtained from all individual participants included in the study.

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