Dayananda Sagar College of Engineering

Department of Electronics and Communication Engineering

ShavigeMalleshwara Hills, Kumaraswamy Layout, Bangalore – 560 078.

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A Report on

'CMOS IMPLEMENTATION OF ROW AND COLUMN DECODER FOR A NON-VOLATILE MEMORY'

Submitted by:

HRIDIK THEJUS K	**1DS22EC088**
KARTIK VIJAYASINHA DESAI	**1DS22EC097**
KRUSHIK JP	**1DS22EC107**
MD RIYAN	**1DS22EC125**

Faculty In-charge

Dr. JAMUNA S

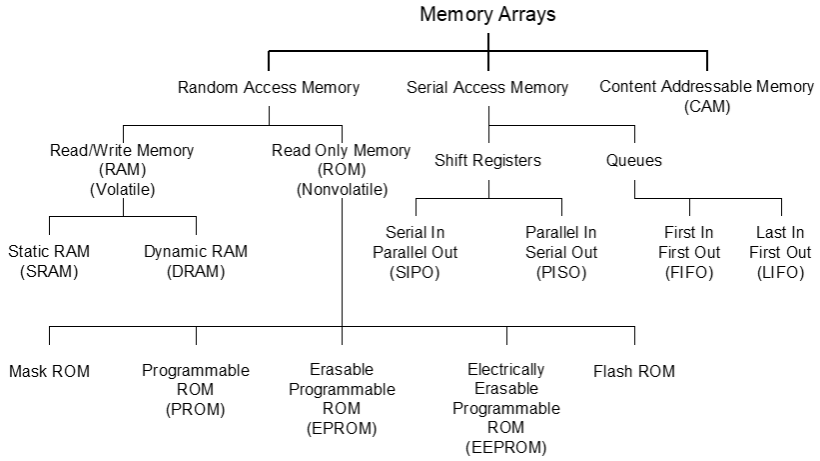
INTRODUCTION:

Non-volatile memory:

Non-volatile memory (NVM) is a type of computer memory that retains stored data even when the power supply is turned off. It is widely used in applications where long-term data retention is essential.

Below gives the classification of the memory arrays:

Memory Arrays



Basic Non-volatile Memory contents are:

Component	**Function**	**Example**
Memory Array	Stores data in binary form	Flash cells, DRAM cells
Row Decoder	Select the row for accessing memory	Worldline activation in Flash
Column Decoder	Selects the column for accessing memory	Bit line selection in SRAM
Sense Amplifiers	Amplify weak signals for reliable reading	DRAM and Flash memory
Read/Write Circuits	Handle data flow during read/write operations	EEPROM, Flash write circuits
Control Logic	Manage commands and operations	NAND Flash controllers
Address Lines	Carry address signals for cell selection	Address bus in memory chips
Data Lines	Transfer data between memory and devices	Data bus in Flash memory
Charge Pumps	Provide high voltage for write/erase	Programming in Flash memory
Error Correction	Detects and corrects data errors	ECC in SSDs
Interface Logic	Enables communication with external systems	SPI, NVMe, or SATA in storage

MEMORY ARRAY:

A memory array is the core component of a memory chip where data is stored in the form of binary values (0s and 1s). It is organized as a grid or matrix of rows and columns, with each intersection containing a memory cell that can hold a bit of data.

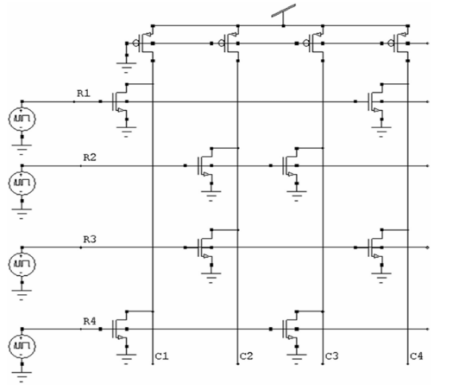


Fig. 1 Schematic diagram of 4 × 4 NOR based semiconductor ROM array

Table 1 Bit pattern inside the rom array

	Columns			
	C1	C2	C3	C4
Rows				
R1	0	1	1	0
R2	1	0	0	1
R3	1	0	1	0
R4	0	1	0	1

WHAT IS ROW AND COLUMN DECODER?

A row and column decoder are a key component in digital circuits, particularly used in memory arrays (like RAM) and multiplexing systems. The purpose of these decoders is to select specific rows and columns within a grid or array to access data or control signals. These decoders convert a binary input address into specific row and column select signals.

1. Row Decoder:

- The **row decoder** is used to select one specific row in a memory array or matrix.
- It takes the **row address** (which is usually part of the overall address in a memory system) and decodes it to activate a specific row line.
- **How it works**: When a binary address is received, the row decoder activates a unique row based on the input address, typically turning on a specific word line in a memory cell array.
- **Example in memory**: In a DRAM (Dynamic RAM) or SRAM (Static RAM) chip, the row decoder selects the correct row in the memory grid that corresponds to the address provided.

2. Column Decoder:

- The **column decoder** works similarly to the row decoder but is responsible for selecting a specific column.
- It takes the **column address** (the other part of the overall address) and activates the corresponding column line.
- **How it works**: The binary column address is decoded, and the column decoder enables the specific column where data is read from or written to.
- **Example in memory**: In a memory array, once the correct row has been selected by the row decoder, the column decoder selects a column within that row to access a particular cell.

CIRCUIT DIAGRAM AND WORKING :

Fig.2 2: 4 Row decoder

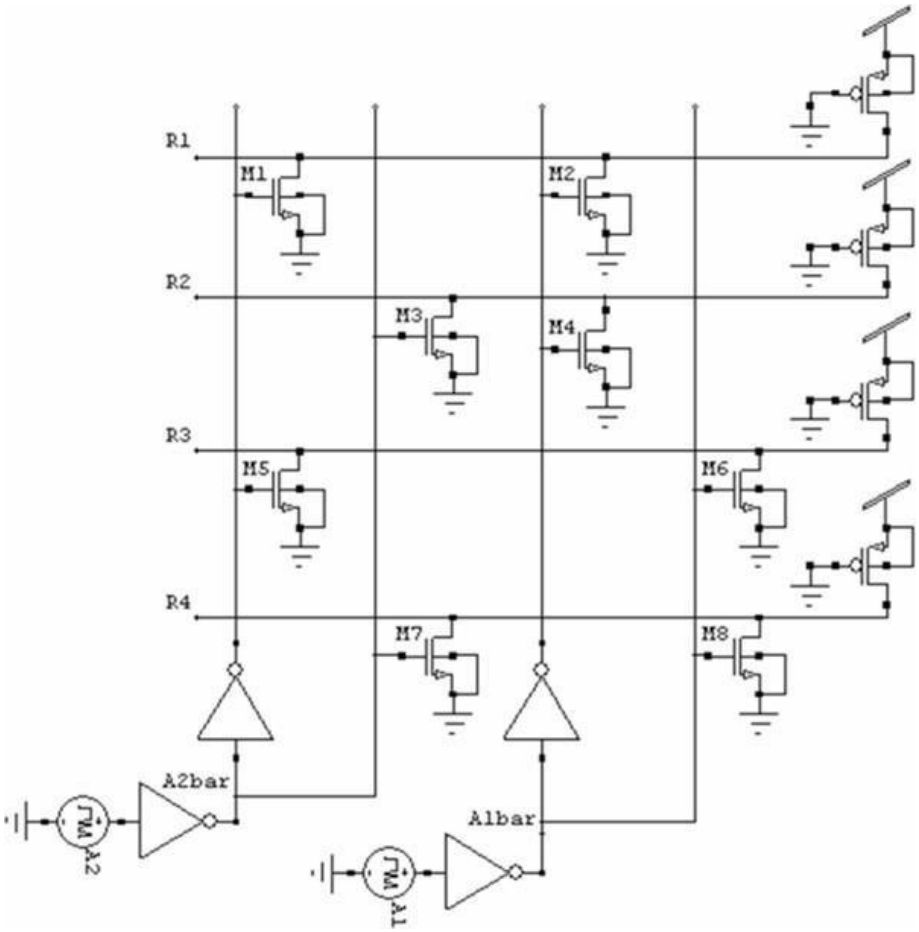


Table 2

A1	A2	R1	R2	R3	R4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig.3 2: 4 Column Decoder

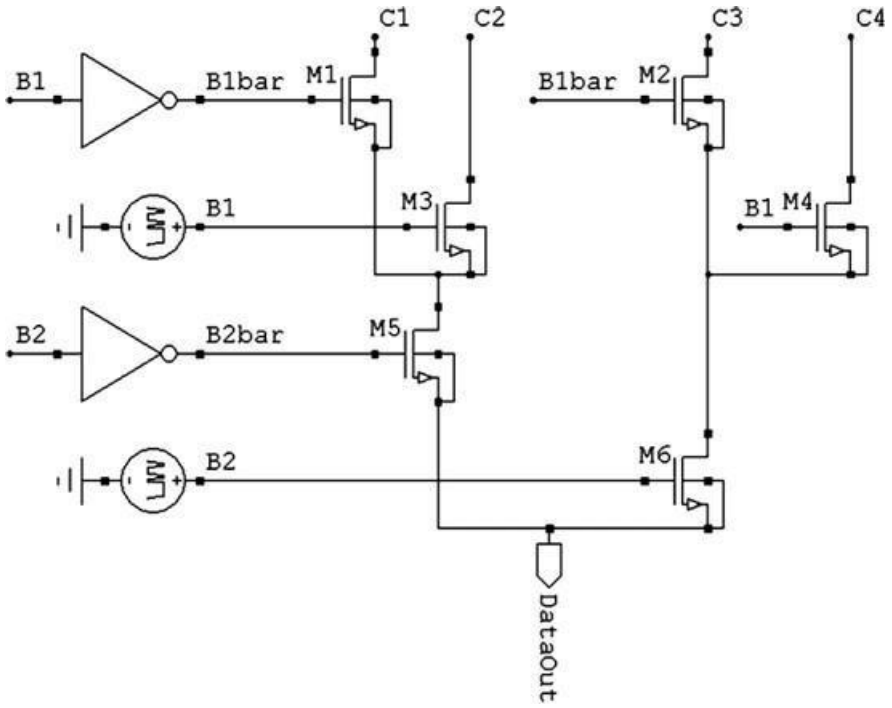


Table 3

B2	B1	Selected column
0	0	C1
0	1	C2
1	0	C3
1	1	C4

Fig.4 Circuit diagram of 4 × 4 NOR based semiconductor ROM for Simulation

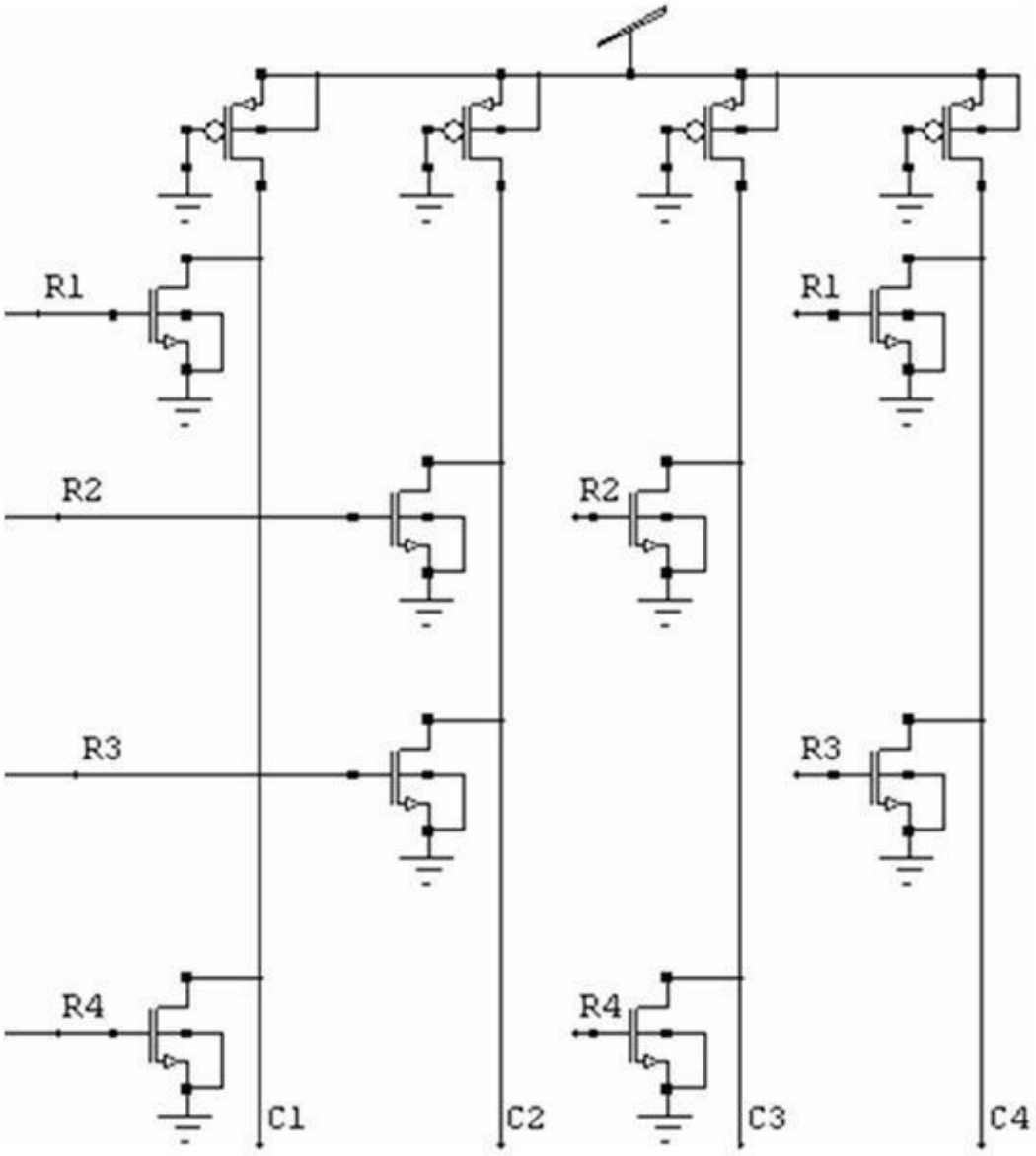


Table 4

R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1
0	0	1	0	1	0	1	0
0	0	0	1	0	1	0	1

WORKING:

- Figure 1 is the structure of 2:4 row decoder. According to the bit pattern of A1 and A2 as shown in Table 1, rows R1 to R4 are selected. For example if A1 = "0" and A2 = "0" then R1 = "1" and other rows are at logic "0". This means only R1 has been selected.

- Similarly, the structure of 2:4 column decoder (Bhowmik and Bari 2014a, b) is shown in Fig. 2. According to bit pattern of B1 and B2 as shown in Table 3 column C1–C4 are selected. At a time, only one column is selected. For example, if B1 = "0", B2 = "0" Then column C1 has been selected and other columns are deselected. This means data through column line C1 will pass to the output through terminal "Data Out". Therefore, if R1 and C1 are selected simultaneously, data from the crossing point of R1 × C1 will pass to the output through C1 lines

- The circuit diagram of 4 × 4 ROM with row lines and column lines is shown in Fig. 3. Four row lines R1, R2, R3, R4 of 4 × 4 ROM array relate to the corresponding terminals of row decoder of Fig. 1. Similarly, columns lines C1, C2, C3, C4 of Fig. 4 are connected to the corresponding terminals of column decoder of Fig. 2. The entire PMOS transistors of Fig. 3 are in the "ON" state. Therefore, the volt age level of all the columns are initially high that is at logic high level. When particular row line is selected, the voltage of that particular row line is raised and NMOS transistors whose gate is connected with that row line becomes in on state. Drain and source terminals of NMOS transistors are connected with associated column and ground respectively as shown in Fig. 3. When particular NMOS transistor is in "ON" state, the associated column voltage will become zero as column is electrically connected to ground through NMOS transistor in on condition. For example, when R1 is selected for A1 = 0 and A2 = 0 of Fig. 1 making its volt age level at high condition, then the transistor at crossing point of R1 × C1 and R1 × C4 are ON in Fig. 3. At the same time, if column C1 is selected data "0" form crossing point of R1 × C1 will pass to the output. If R1 and C4 is selected, then data "0" form crossing point of R1 × C4 will pass to the output. In contrast, by selecting R1 and C2, data "1" will pass to the output through column C2. Similarly, by selecting row lines and column lines properly data from other locations of ROM are retrieved.

APPLICATIONS:

A row-column decoder is a type of circuit or algorithm often used in digital systems and error detection/correction applications. It involves decoding data arranged in a matrix format, where data can be efficiently accessed or verified based on its row and column indices. Below are some common applications:

1. **Memory Address Decoding**
   - **Application**:
     Used in computer memory systems (RAM, ROM).
   - **How it Works**:
     - Memory cells are arranged in a matrix of rows and columns.
     - A row-column decoder translates the address into specific row and column signals to access the correct memory cell.
     - For example, an 8x8 memory matrix has 64 cells but only requires 6 address lines (3 for rows and 3 for columns) to decode the location.
   - **Advantage**:
     Reduces the complexity of memory access circuits.

2. **Error Detection and Correction (ECC)**
   - **Application**:
     Found in systems requiring data reliability, such as communication systems, storage devices, and fault-tolerant systems.
   - **How it Works**:
     - Data is stored or transmitted in a matrix format.
     - Parity bits are generated for each row and column.
     - Errors can be detected and corrected by identifying inconsistencies in row and column parities.
     - Example: Hamming code uses row-column logic for single-bit error correction and multi-bit error detection.

3. **LED Displays and Keyboards**
   - **Application**:
     Used in matrix-based input or output devices like LED panels or keypads.
   - **How it Works**:
     - Each LED or key is connected to a specific row and column line.
     - A row-column decoder determines which LED to light up or which key is pressed by scanning rows and columns.
     - Example: A 4x4 keypad requires only 8 connections (4 rows + 4 columns), reducing wiring complexity.

4. **Crossbar Switches**
   - **Application**:
     Found in communication networks and high-performance computing for connecting multiple inputs to multiple outputs.
   - **How it Works**:
     - Inputs and outputs are arranged in rows and columns.
     - A row-column decoder determines which input is connected to which output through a crosspoint.

ADVANTAGES:

Row and column decoders are used in memory peripheral circuitry to reduce the number of select signals. They have several advantages, including:

Selecting cells: Row and column decoders select specific cells in a memory array to read or write data.

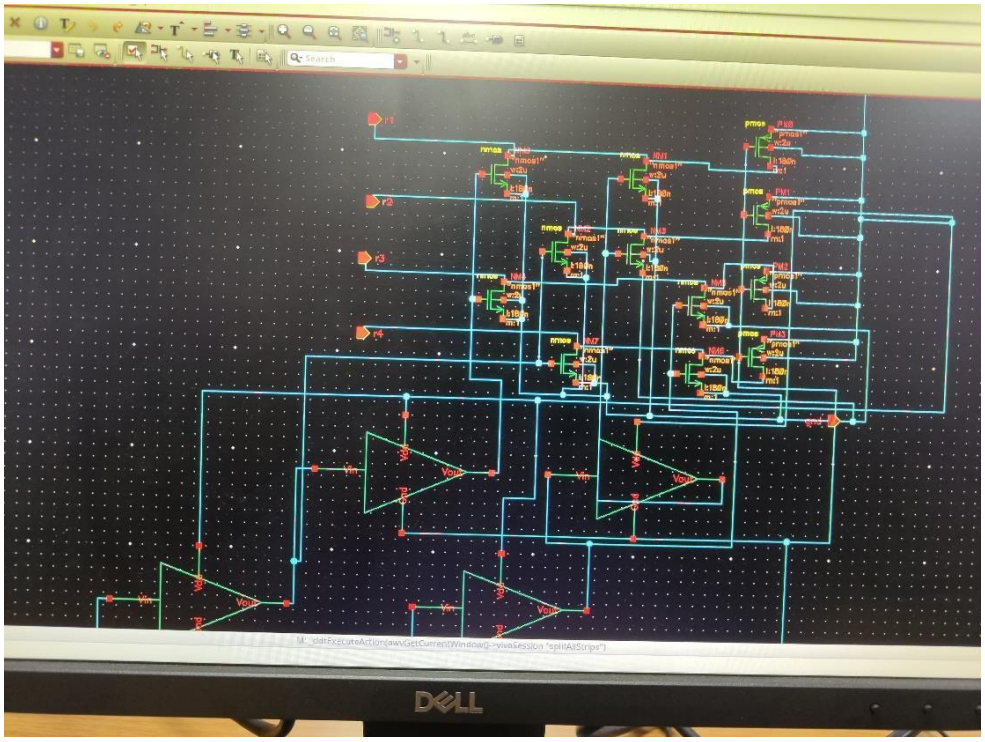
Reducing selects signals: Row and column decoders reduce the number of select signals needed.

Power savings: Block address activation only activates one block, which can save power.

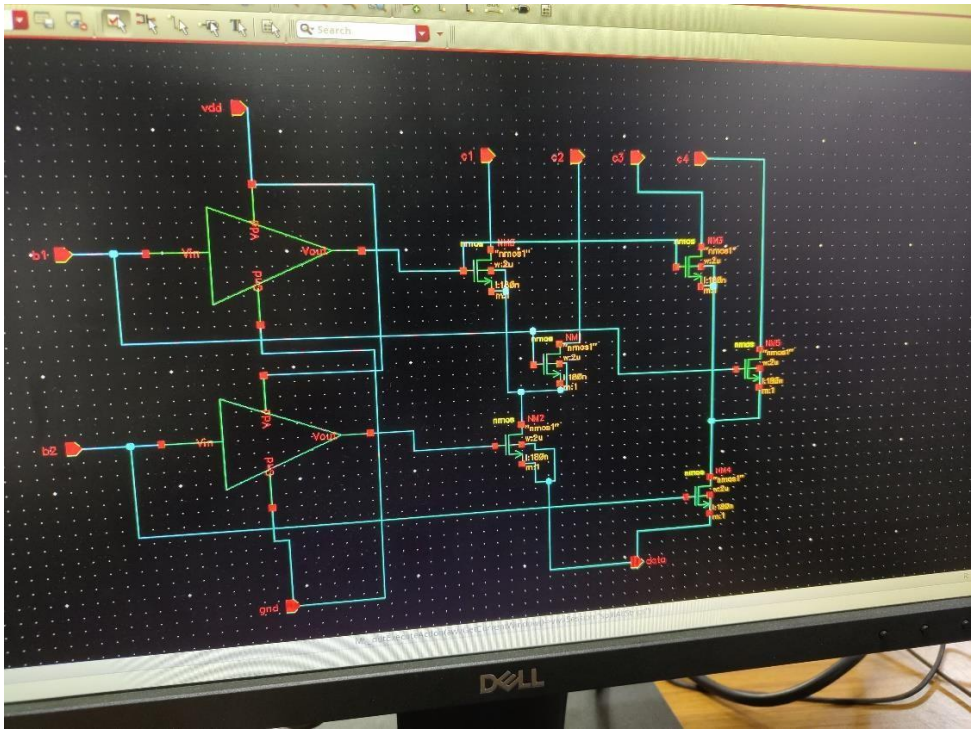
Shorter wires: Shorter wires can be used within block

RESULTS:

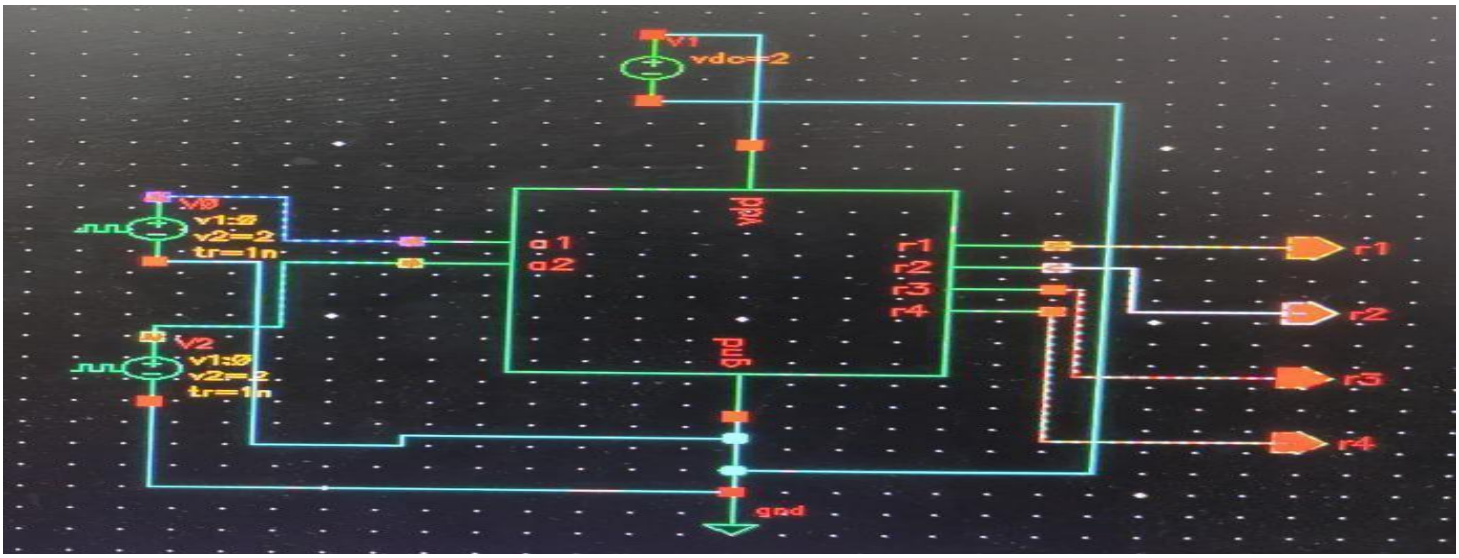
ROW SCHEMATIC:



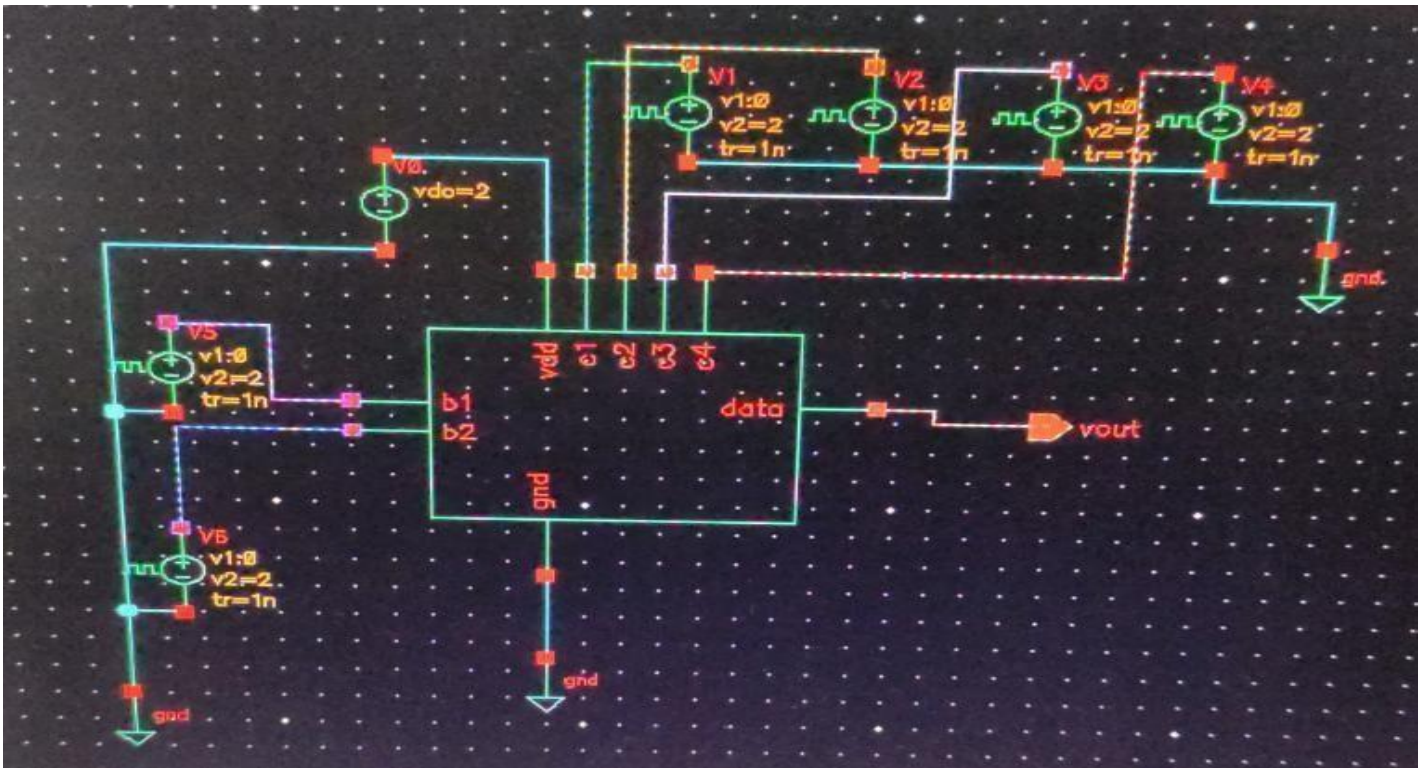
COLUMN SCHEMATIC:



ROW TEST CIRCUIT:

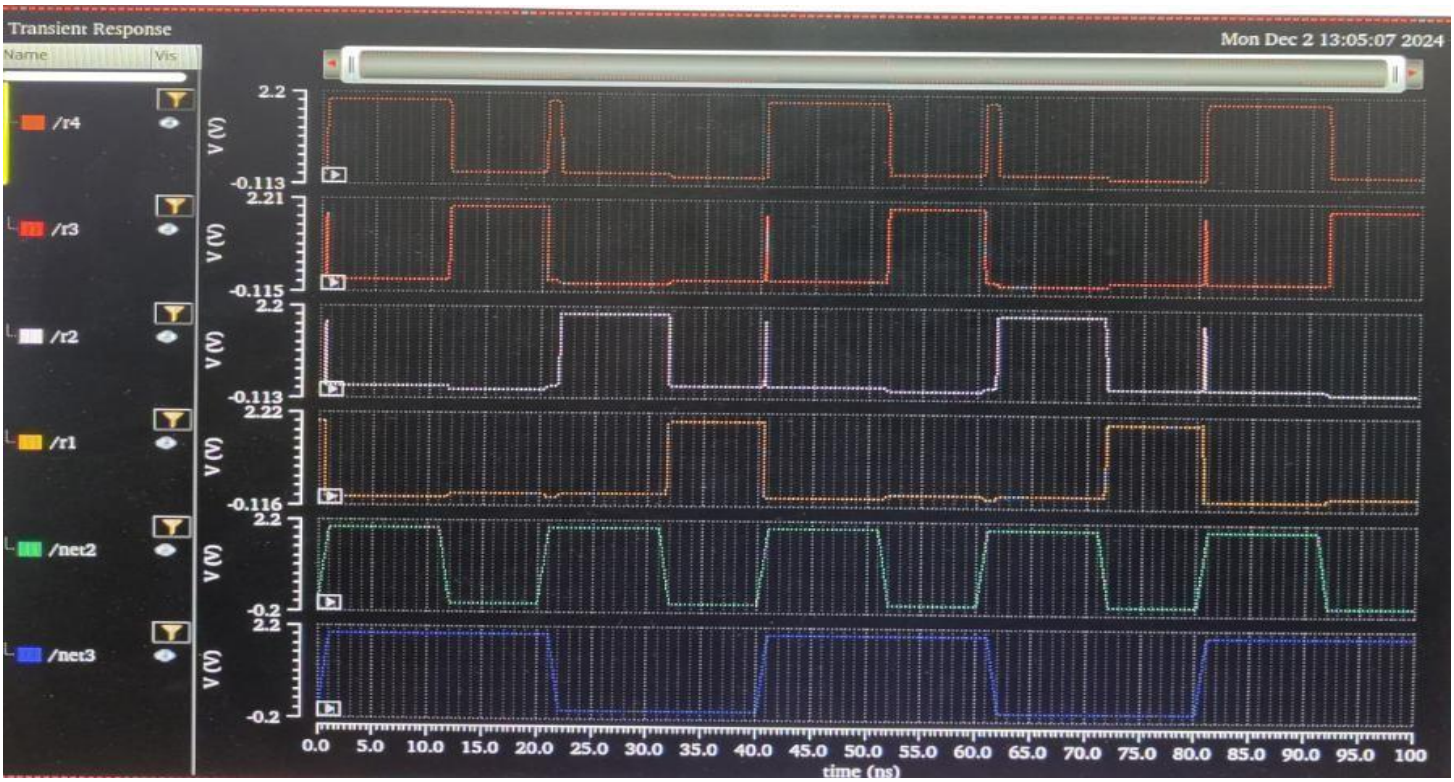


COLUMN TEST CIRCUIT:

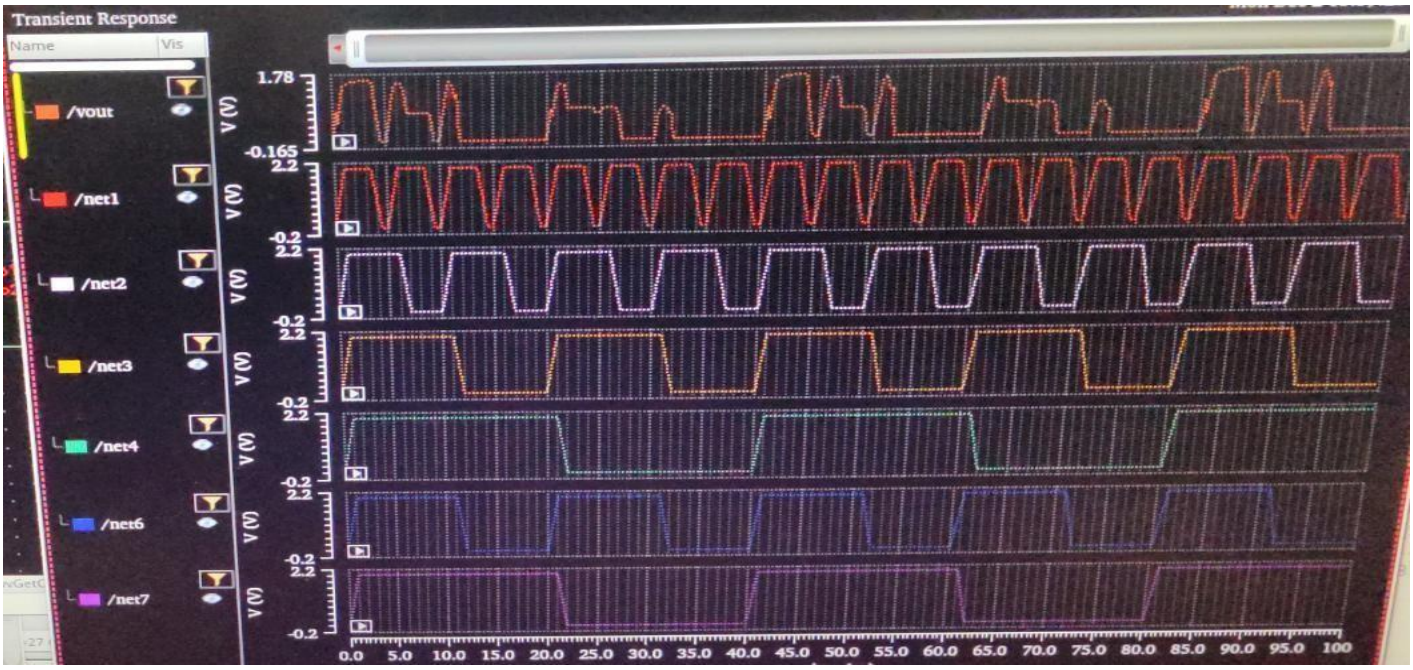


OUTPUT WAVEFORMS:

FOR ROW DECODER:

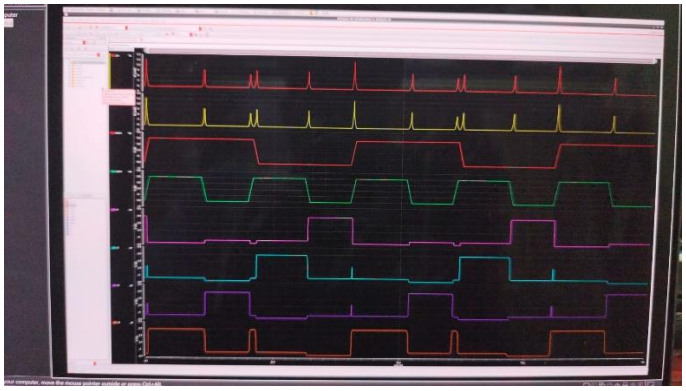


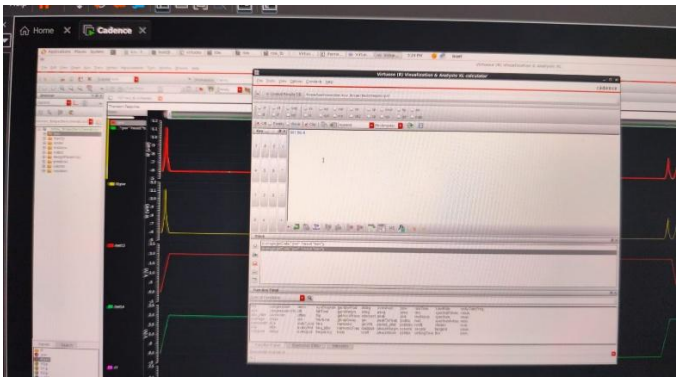
FOR COLUMN DECODER:



POWER DISSIPATIONS FOR THE NMOS AND PMOS TRANSISTORS:

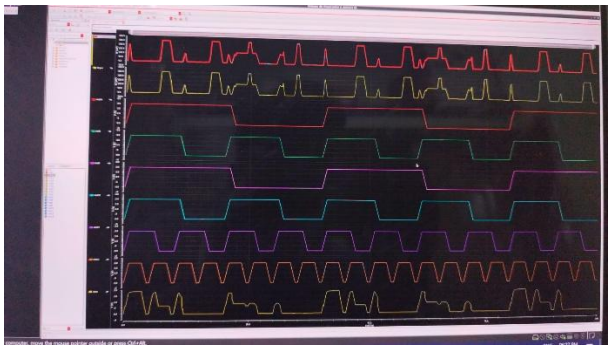
1.Row Decoder Circuit





Average power value is: 601.5 E-6

2.Column Decoder Circuit



Average power value is:58.86 E-6

CONCLUSION:

In conclusion, the CMOS-based row-column decoder successfully demonstrates the ability to convert binary inputs into specific row and column signals through efficient logic design. The implementation effectively utilizes the complementary nature of CMOS transistors to ensure low power consumption and high noise immunity, which are key advantages in digital circuit design. The decoder's performance was verified by its accurate response to input combinations, and the results show that it can efficiently drive the desired outputs while minimizing power dissipation. This CMOS implementation proves to be a reliable and scalable solution for row-column decoding applications in memory systems and other digital circuits, highlighting its suitability for modern electronic systems that demand both efficiency and robustness.

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