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A Simulation Study of NBTI Impact on 14-nm Node FinFET Technology for Logic Applications: Device Degradation to Circuit-Level Interaction

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***Abstract*— A comprehensive simulation flow is demonstrated to assess the negative-bias temperature instability (NBTI) impact on the performance and power of digital logic circuits based on the 14-nm node FinFET technology. Fully calibrated technology computer-aided design simulations are used to determine the preaged and postaged device characteristics; the results are used for calibrating the BSIM-CMG compact model. Standard cell libraries are characterized next, by only threshold voltage shift (ΔV_T) and by both ΔV_T and subthreshold slope shift (ΔSS). Various benchmark circuits are synthesized and analyzed, and their timing degradation is compared to ring oscillator results. The consequence of ignoring ΔSS on off current and static power (P_{static}) is estimated.**

***Index Terms*— BSIM-CMG, circuit simulation, compact model, FinFET, mixed-mode simulation, negative-bias temperature instability (NBTI), ring oscillator (RO), SPICE, standard cells, static power, subthreshold slope degradation.**

I. Introduction

MOSFET aging due to bias temperature instability (BTI) is a crucial reliability issue that impacts the performance of circuits over time [1]–[3]. Negative BTI (NBTI) remains as a major concern for high-K metal gate p-FinFETs, and positive BTI becomes negligible for n-FinFETs [4]. NBTI physical mechanism is predominantly governed by the generation of interface traps (ΔN_{IT}) [5] that are donor type in nature [6]. The generated traps result in the degradation of several device parameters, such as ΔV_T, ΔSS, transconductance (Δg_m), linear drain current (I_{DLIN}) and saturation (I_{DSAT}) drain current, and gate–drain capacitance (ΔC_{GD}) [7]–[10]. To continue with the technology scaling in the advanced nodes, it has become necessary to use 3-D device designs, e.g., bulk [11], [12] and silicon-on-insulator FinFETs [13], [14], and several other options are being considered as gate-all-around nanowire [15] and nano sheet [16], [17] MOSFETs, and new channel material such as silicon germanium ($Si_{1-x}Ge_x$) [18] for the p-channel device.

The shift in focus from the traditional to novel devices and channel material comes with a lot of challenges in terms of the co-optimization of performance, power, and reliability for meeting requirements of delivering the product to market in stipulated time. Previously, the process design kits, design rules and transistor models provided by the fabs were scalable as predicted by well-understood scaling rules. However, with the introduction of nontraditional devices, complexity arises and different steps in the development cycle need to interact with each other to reduce time to market. The design technology co-optimization (DTCO) technique is gaining interest in this scenario [19]–[21]. DTCO comprises technology computer-aided design (TCAD)-based device simulations and efficient compact model parameter extraction for predicting the circuit behavior ahead of time, thus speeding up the entire process. As NBTI is a crucial reliability issue, it is essential to integrate it into the existing DTCO flow to bring in aging awareness, as the current flow only focuses on the performance, power, and area optimization. Moreover, accurate estimation of NBTI induced circuit delay degradation is necessary to introduce small, yet sufficient timing guard bands to prevent timing violations and to ensure that the reliability is sustained until the end of life (EOL).

Since NBTI results in increase in V_T with time, the circuits become slower as the ON current reduces. However, the OFF current also reduces due to exponential dependence with V_T. The result of reduction in static power for circuits due to NBTI can prove advantageous over time [22]. The state-of-the-art design considers this reduction in static power after aging by using the V_T shift as the handle [22]–[24], but it often ignores the SS degradation and its potential impact on circuit standby power. Several techniques are in use, especially in low-power designs, to optimize static power in the presence

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of aging effects, such as power-gating technique using sleep transistors (STs) [22], [23] and appropriate minimum leakage vector selection [24]. These techniques tend to be less accurate unless ΔSS due to NBTI on the static power is incorporated in the existing electronic design automation (EDA) tool flows.

The scope of this paper is to demonstrate a comprehensive simulation framework at a relatively new technology node (14 nm) that goes from the device-level TCAD preaging and postaging models to SPICE model parameter extraction and subsequent standard cell characterization for the analysis of complex circuits under stress. Integration of TCAD into the flow enables more reliable presilicon DTCO in the presence of NBTI. Standard cell libraries are characterized that contain the detailed power and delay information of the gates from fresh to EOL under NBTI aging, using only ΔV_T and both ΔV_T and ΔSS. These libraries are characterized based on the careful calibration of the terminal characteristics with the experimental data and TCAD simulation for preaging and postaging scenarios. Different gates are found to show different timing degradations depending on the input signal slew and load capacitance. The static power reduction after aging is also different for different gates and depends whether only V_T shift or both V_T and SS shifts are considered. It is demonstrated that neglecting ΔSS (as done in state of the art [25]) leads to overestimation of the impact of NBTI on OFF current, and it is indispensable to include both V_T and SS degradation to accurately estimate the NBTI impact on static power (improvement) of circuits over time.[1] Error due to ignoring C_{GD} degradation after NBTI is discussed. Degradation of several benchmark circuits that are synthesized at time zero is evaluated at EOL by using the constructed aging-aware cell libraries. The timing guardband requirements are discussed.

II. Simulation Results and Discussion

Fig. 1 shows the complete simulation flow followed, in this paper, with the blocks presenting different steps involved and possible correlations. The flow begins with a TCAD-based process simulation and device simulation. The output of the TCAD device simulation is used to extract SPICE compact model parameters[2] for smaller circuit simulation. For larger circuits, standard cell libraries are characterized and are used for synthesis to obtain timing, area, and power reports under different scenarios. In the following discussion, we describe various steps in detail.

Note that the transistors are connected in various configurations in different gates and are expected to be aged differently based on the effective activity of the gate stimuli at the inputs. In this paper, activity dependence is not considered and the results provide a possible upper bound to the circuit degradation at EOL. In fact, estimating the worst case impact of aging on the delay of circuits is typically required at the design phase

[1]This paper focuses mainly on the NBTI induced degradation of the subthreshold leakage component in p-FinFETs and ignores degradation in other possible leakage components due to various mechanisms, e.g., stress-induced leakage current (SILC).

[2]SPICE parameter extraction needs detailed I–V (both transfer and output) and C–V characteristics before and after stress. I–V and C–V measurements are slow and hence challenging to perform due to NBTI recovery. The use of TCAD is beneficial in this scenario.

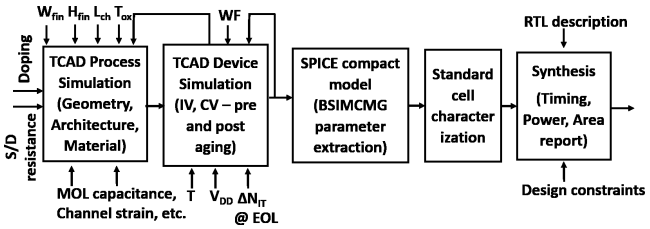
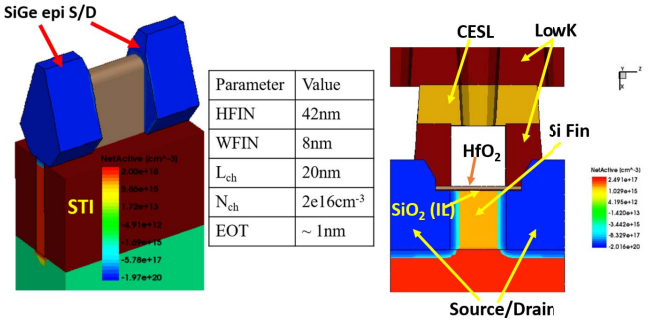


Fig. 1. Complete simulation methodology demonstrated in this paper.



Parameter	Value
HFIN	42nm
WFIN	8nm
L_{ch}	20nm
N_{ch}	2e16cm^{-3}
EOT	~ 1nm

Fig. 2. FinFET structure considered in this simulation study targeting 14-nm technology node with the dimensions as reported in [12]. The parasitic MOL capacitances are accounted for in our simulations.

when workloads are not known *a priori*, to predict sufficient timing guard band that needs to be included. This ensures that timing errors/violations due to NBTI are later on prevented during the entire projected lifetime (e.g., 10 years), regardless of which kind of workloads the end-user of circuit would run on top of it. Without such an upper bound estimation (even though it is conservative), guarantees of reliability for the entire lifetime cannot be provided. In addition, NBTI effects can be protected against in circuits by either timing guard bands, i.e., additional time slack on top of the maximum delay or by voltage guard band, i.e., additional voltage margin on top of the nominal operating voltage. In this paper, we focus on the timing guard bands as a means to protect the circuits against NBTI effects. Hence, voltage adaptation using dynamic voltage frequency scaling [26] is not considered.

A. NBTI Model and Device-Level TCAD Simulations

Many reports suggest that NBTI induced overall ΔV_T is due to uncorrelated contributions from interface trap generation (ΔV_{IT}), hole trapping in the pre-existing interlayer (IL) defects (ΔV_{HT}), and the generation of defects in the oxide bulk (ΔV_{OT}) [5], [27], [28]. For high stress bias (V_{GSTR}) and temperature (T), both ΔV_{IT} and ΔV_{OT} contribute significantly, while the ΔV_{HT} contribution is small in industrial grade devices. However, for typical use V_{GSTR} for circuit operating, ΔV_{IT} dominates overall NBTI degradation. Therefore, only the ΔV_{IT} component is used in this paper.

The 3-D FinFET structure used for TCAD simulations is shown in Fig. 2, with device related parameters obtained from a 14-nm high-volume manufacturing process [12]. Multigate devices suffer from middle-of-line parasitic capacitances, and these are accounted in our simulations for accurately capturing ac and transient response. The structure from [29] includes the relevant process-related effects, e.g., epitaxially grown

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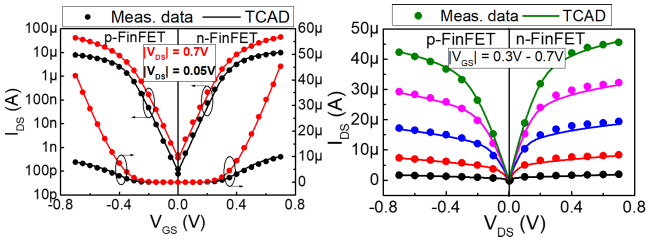

Fig. 3. Time zero (a) I_d–V_g and (b) I_d–V_d calibration with the room temperature hardware data from [12] for both p-FinFET and n-FinFET.

SiGe source/drain (S/D) for p-FinFETs and Si epi-S/D for n-FinFETs, elevated S/D with {111} facets, and out diffusion of Ge into the channel. Density gradient quantum corrections, thin-layer mobility model for scaled fin dimensions [30], high-κ layer-induced mobility degradation, channel strain-related mobility improvement, crystal orientation effects on channel mobility, and ballistic mobility parameters to account for the quasi-ballistic carrier transport in these dimensions have been considered. The S/D doping, subfin doping, source–drain series resistance, gate metal work function, low-field-mobility parameters, and high-field saturation parameters were calibrated to reproduce data of [12] (room temperature transfer and output characteristics) for both p-FinFET and n-FinFET, as shown in Fig. 3.

To calculate the effect of NBTI on device characteristics, donor-type interface traps are placed at the Si/SiO_2 interface for p-FinFETs. Experimental reports suggest that NBTI generated traps being broadly distributed in energy bandgap [31], [32]. For simplicity, in this paper, traps are assumed to be uniformly distributed in the entire bandgap, though the effect of trap energy distribution profile is discussed in Section II-C. The traps lead to the degradation of drain current in the entire span of gate and drain voltage in the transfer and output characteristics, as shown by symbols in Fig. 4(a) and (b), respectively. The EOL degradation criterion is set as 50 mV for postaging simulations in this paper, which corresponds to ΔN_{IT} of 1.5e12 cm^{-2}.

B. BSIM Parameter Extraction and SPICE Implementation

BSIM-CMG model parameters are extracted for both prestress and poststress conditions to do SPICE circuit simulations and standard cell library characterization. The steps used for preaging parameter extraction are adopted from [33] and shown in Fig. 5. In order to capture the effects of aging on V_T and SS, the V_T shift (DVTSHIFT) and interface state capacitance (CIT) parameters are tuned. SS degradation is handled empirically in BSIM-CMG by multiplying n^3 with the thermal voltage (V_{tm}) in the I–V equation (see [34] for details). For bulk FinFET, n is given by

$$n = 1 + \frac{\mathrm{CIT} + C_{dsc}}{2C_{si}||C_{ox}} \tag{1}$$

where CIT is a parameter related to interface states, C_{dsc} is the coupling capacitance between S/D to channel, C_{Si} is the

[3]This n is a BSIM-CMG variable and not to be confused with NBTI time exponent (n).

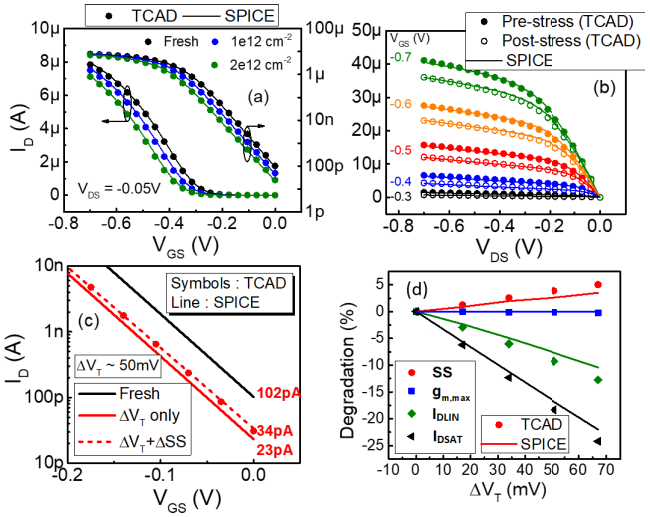

Fig. 4. SPICE validation of (a) transfer characteristics and (b) output characteristics for preaging and postaging. (c) Subthreshold slope degradation leading to higher off current predicted by SPICE. (d) Summary of SPICE validation for different devices related parameter degradation obtained from TCAD.

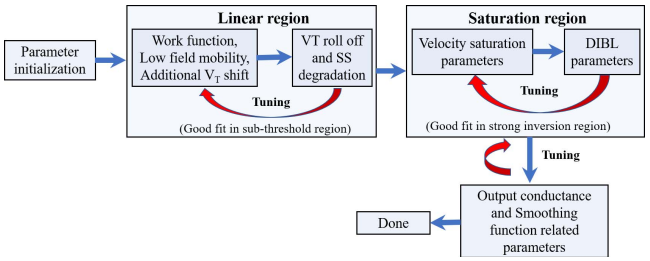

Fig. 5. BSIM-CMG parameter extraction procedure followed in this paper.

depletion capacitance, and C_{ox} is the oxide capacitance. Interdependencies between various aging-related variables and/or SPICE parameters are given by the following equations:

$$\Delta V_T = \frac{q\Delta N_{IT}}{C_{ox}} = k_1 \Delta N_{IT} \tag{2}$$

$$\Delta \mathrm{SS} = k_2 \Delta N_{IT} \tag{3}$$

$$\Delta \mathrm{SS} = k_3 \mathrm{CIT} \tag{4}$$

where k_1, k_2, and k_3 are the linear proportionality constants and their values are obtained from TCAD and SPICE simulations, as shows in Fig. 6. Using the above-mentioned methodology, TCAD results (symbols) of Fig. 4 are reproduced using SPICE simulations [35] (lines). Note that only ΔV_T-based approach is sufficient in predicting all the dc characteristics except for matching the sub-V_T region and OFF current, for which the CIT parameter is adjusted for different amount ΔN_{IT} concentrations. Fig. 4(c) shows the OFF current variation after NBTI stress with and without considering SS degradation. Only ΔV_T results in 77% reduction in OFF current, whereas inclusion of ΔSS brings it up to 67%, i.e., 10% underestimation for 50-mV V_T shift.[4] This signifies the

[4]Though this can be considered to be marginal, it would be important in low-power applications (see [23]) and must be harnessed for the advantage by the system designers. As per the authors' views, it is more of accurate estimation that is important rather than the application itself which is the designers' prerogative to incorporate.

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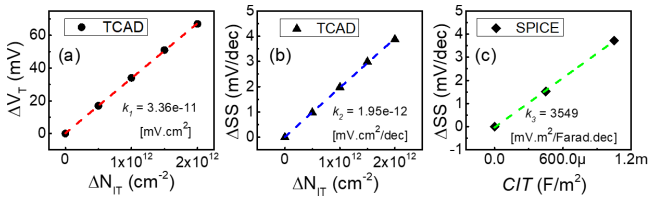

Fig. 6. Relationship between (a) ΔN_{IT} versus ΔV_T (from TCAD), (b) ΔN_{IT} versus ΔSS (from TCAD), and (c) ΔSS versus SPICE parameter CIT (from SPICE).

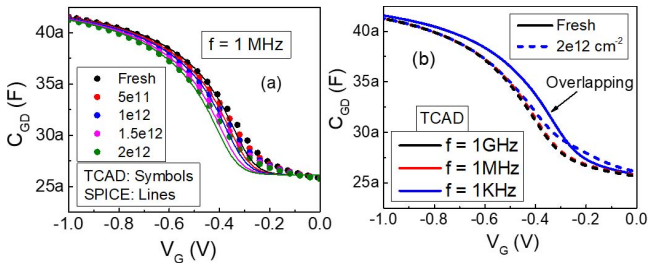

Fig. 7. (a) C_{GD}–V_G characteristics for different trap densities at f = 1 MHz predicted by SPICE using ΔV_T only. (b) Frequency dependence can be observed for C_{GD} when interface traps are present.

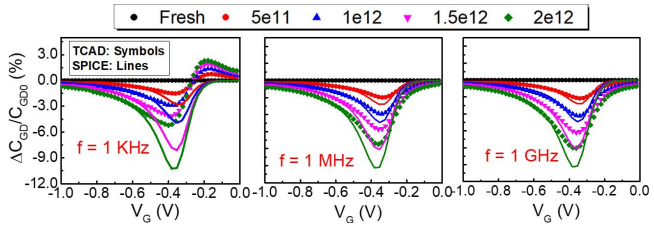

Fig. 8. Percentage ΔC_{GD} degradation for different frequencies as a function of trap density (in cm^{-2}◁. ΔV_T only approach in SPICE fails to capture the TCAD results at low frequency.

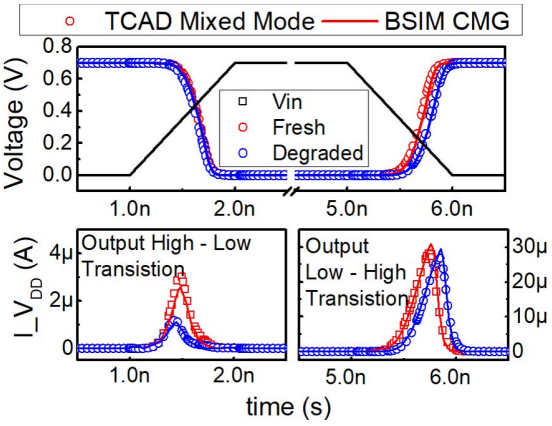

Fig. 9. Validation of SPICE framework against TCAD mixed-mode simulation for an inverter. Only V_T shifted model is good to predict timing delay.

importance of considering ΔSS in evaluating standby power for circuits, especially in low-power scenarios. To summarize dc extraction, Fig. 4(d) shows the correlation of V_T shift with I_{DLIN}, I_{DSAT}, peak g_m, and SS degradation from both TCAD and SPICE using extracted BSIM-CMG parameters. It is noteworthy that negligible peak g_m degradation is observed in our simulations, consistent with the experimental report [10].

Apart from the dc characteristics, the ac response under the effect of aging is important for transient circuit simulations. The speed of the circuit is limited by the gate capacitance, a fraction of which appears between gate–drain terminals and contributes to parasitic load capacitance. Fig. 7(a) shows the BSIM-CMG validation of TCAD simulated C_{GD} for different trap densities at 1-MHz frequency.[5] Note that only ΔV_T shift-based approach predicts the poststress CV curves reasonably well. However, as the frequency is lowered, a clear deviation can be seen as in Fig. 7(b) from TCAD simulations. As expected for a FinFET device, the fresh device CV shows independence with the frequency. But the degraded device shows skew in the CV (a well-known effect in the presence of interface states [36]) due to additional C_{IT}[6] on the account of continuous trapping and detrapping in the interface states, particularly at low frequency. At low frequency, the traps can respond to the gate signal and contribute to the increase in C_{GD}. Fig. 8 shows the percentage change in C_{GD} because of ΔN_{IT} at different frequencies. The skewness in CV of Fig. 7(b) is clearly reflected in Fig. 8(a). It can be deduced from these plots that estimating ΔC_{GD} using a pure V_T shift approach becomes increasingly accurate at high frequencies.

[5]Postaging device frequency response depends on the frequency response of the interface states. The corresponding parameters (e.g., capture/emission time constants of the traps) may need to be calibrated for a given process, though in this paper calibration has not been performed.

[6]Here, C_{IT} is a general term for interface state capacitance, whereas CIT is a BSIM-CMG specific parameter for capturing SS degradation due to ΔN_{IT}.

To verify the validity of the extraction at the circuit level and the accuracy of adopting ΔV_T only approach in circuit simulations, mixed-mode simulation is performed for a single inverter and compared against the SPICE simulations. Typical rise/fall time of 1 ns for the input pulse and a load capacitance of 5 fF are used. The results of Fig. 9 show that the voltage and current waveforms agree well with TCAD under the chosen slew and load conditions (not shown here are the validation for the rise/fall time of 1 ms that agree well with TCAD also), which justify ignoring the contribution of ΔC_{GD} for the transient circuit simulation.

C. Effect of Trap Energy Distribution and Hole Trapping

NBTI generated interface traps are suggested to have broad energy distribution as mentioned earlier. However, to illustrate the impact of trap distribution, two types of distributions, that is: 1) traps present uniformly in the entire bandgap—as done in this paper and 2) traps concentrated only in lower half of the bandgap, are analyzed. As shown in Fig. 10, for a given ΔV_T, when traps are present only in the lower half of the bandgap, the percentage I_{DLIN}, SS, and C_{GD} degradations are higher. This can be attributed to the fact that for more concentrated trap profile in energy, the spatial trap density needs to be higher to achieve the same V_T degradation and hence in effect, the Fermi level scans a larger concentration. It introduces more interface-state capacitance (C_{IT}), thus increasing SS and C_{GD} significantly. In this scenario, the SPICE compact model can be calibrated by tuning the interface-state capacitance

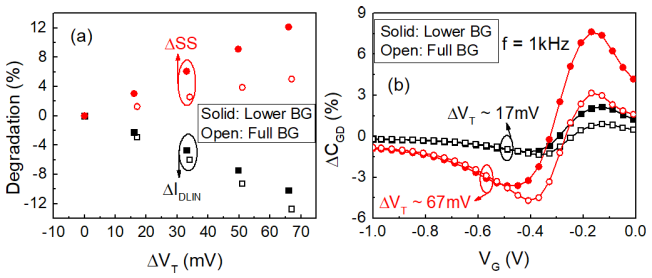

Fig. 10. Effect of trap energy distribution profile on (a) device SS and I_{DLIN} degradation and (b) C_{GD} degradation as a function of threshold voltage shift.

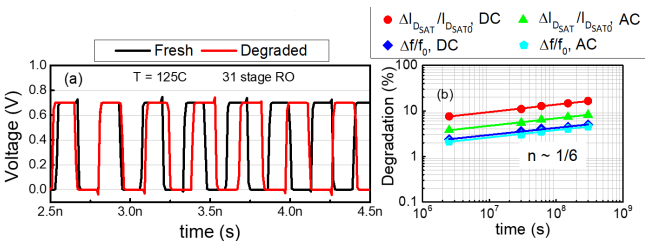

Fig. 11. (a) Transient 31-stage RO simulation showing frequency degradation after aging. (b) Frequency degradation under static and dynamic stresses for RO gives $n \sim 0.16$ similar to the device degradation.

parameter CIT, although quantitative modeling of these effects is beyond the scope of this paper.

Moreover, if the hole-trapping component (ΔV_{HT}) is non-negligible, the relative correlation of ΔV_T on SS degradation would be diminished. This is because the hole trapping does not affect SS and for a given ΔV_T ($= \Delta V_{IT} + \Delta V_{HT}$), the interface trap component (ΔV_{IT}) would become smaller [9]. However, the hole trapping is ignored in this analysis as it is found to be negligible for well-optimized devices.

D. RO Degradation Analysis

Ring oscillator (RO) frequency degradation due to NBTI is shown for a 31-stage RO under static and dynamic stresses in Fig. 11(a). Dynamic/ac stress affects all the transistors in the chain, while static/dc stress affects only alternating transistors. Degradation due to dynamic aging is always lower than that due to static aging because of recovery effects. A ratio of 0.5, typically observed in experiments [37], is assumed between ac-to-dc degradation in this analysis, e.g., in our case since dc shift is 50 mV due to ΔN_{IT} of 1.5e12 cm^{-2}, ac shift would be 25 mV corresponding to ΔN_{IT} of 7.5e11 cm^{-2}. The device-level I_{DSAT} shift closely correlates with the RO frequency degradation (Δf) and follows similar power law time exponent, as shown in Fig. 11(b). It can be noted that though dc and ac stresses have different impacts at the device ΔI_{DSAT}, however, $\Delta f/f_0$ associated with RO (f_0 being unstressed frequency) is almost independent of dc or ac stress type. It can be seen from the plot that the multiplier for the device to RO degradation is less than unity as shown in the following equation, consistent with [35]:

$$\left(\frac{\Delta f}{f_0}\right)_{\mathrm{dc/ac}} \approx \frac{1}{4}\left(\frac{I_{\mathrm{DSAT}}}{I_{\mathrm{DSAT0}}}\right)_{\mathrm{dc}} = \frac{1}{2}\left(\frac{I_{\mathrm{DSAT}}}{I_{\mathrm{DSAT0}}}\right)_{\mathrm{ac}} \quad (5)$$

E. Standard Cell Analysis

The extracted model cards (prestress for n-FinFET, both prestress and poststress for p-FinFET) are used to characterize the SPICE netlist of FinFET compatible standard cell library from [38] using a standard EDA tool [39]. This library contains the detailed timing, power, and area information of all the standard cells considered in this paper. The library has 69 different cells consisting of wide range of combinational cells[7] (e.g., AND, OR, NAND, NOR, AOI, OAI, BUF, INV, MUX, XNOR, HA, and FA), sequential cells (e.g., DFF and scan DFF), and few additional cells (e.g., tristate BUF, clock BUF, tie high, and tie low) with varying drive strengths to expand the design space and achieve better optimization goals (refer to [38] for expansions of the abbreviations). All cells are characterized in prestress and recharacterized in post-stress conditions at EOL, by using ΔV_T only and ΔV_T plus ΔSS scenarios. The aging impact on increase in t_{Delay} for different gates shows strong variation as shown in the histogram plot of Fig. 12(a). This histogram is constructed using the delay degradation obtained from all the standard cells of the library under a 7 × 7 matrix of input signal slew and output load conditions, e.g., input slew ranging till 70 ns and output load capacitance varying from 0 to 20 fF. Majority of gates are affected by ~15%, and others quite large (up to 35%) at EOL. The input signal slew and output load capacitances also impact t_{Delay} for every gate, although the impact is different for different gates as reflected in Fig. 12(b). Fig. 12(c) shows the reduction in P_{static} for a set of sequential and combinational gates owing to aging at EOL. Reduction in P_{static} varies across gates (~10%–55%, even 0% for certain cells), and ignoring ΔSS always overestimates the reduction in P_{static}. Due to the nonuniformity of aging impact and strong dependence on the load capacitance and input slew (see Fig. 12), all cells in the library require proper characterization under NBTI effects.

TABLE I
DIFFERENT BENCHMARK CIRCUITS USED IN THIS PAPER

Circuit	No. of gates	Logic depth
s15850	685	10
s13207	1219	8
spi	3227	13
s38584	6724	16
s35932	7273	6
s38417	8278	21
ac97_ctrl	11855	12
usb_funct	12808	8
aes_core	20795	15
b19	43258	24
des_perf	98341	11

[7]In the library, the format in which the cell name is identified is the name of the logic function and the number of inputs and the drive strength separated by an underscore (e.g., an AND with four inputs and drive strength of X2 has the name AND 4_X2). The suffix X2 means that the cell has twice the drive strength compared to cells with X1.

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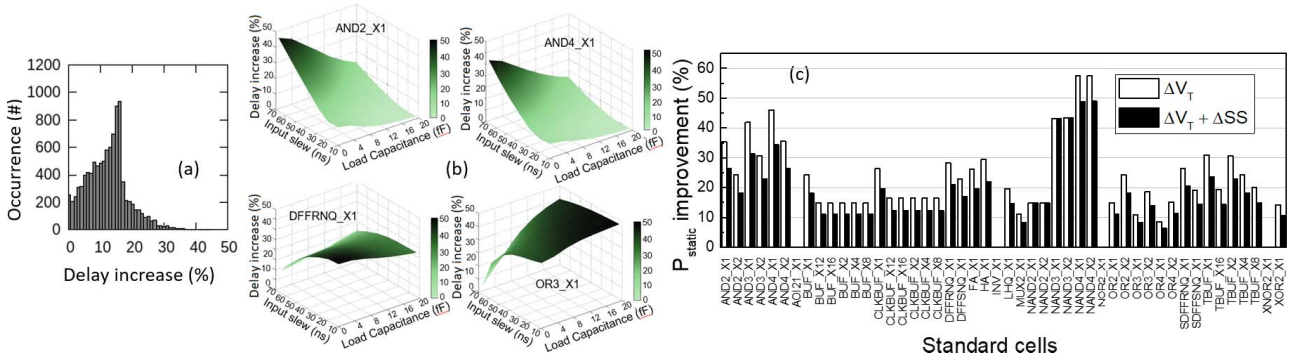

Fig. 12. (a) Impact of aging on increasing the delay of all standard cells within a FinFET cell library. Strong variation is observed. Every cell is analyzed under 7 × 7 slew and load matrix. (b) Exploring the role of input signal slew and output load capacitance in determining the impact of aging on increasing the delay of a gate. Some gates like and2 are more sensitive to aging more than others like and4. Suffixes X1 and X2 denote different drive strengths. (c) Impact of aging on reducing the static power of standard cells. P_{static} of different gates can be influenced by aging differently.

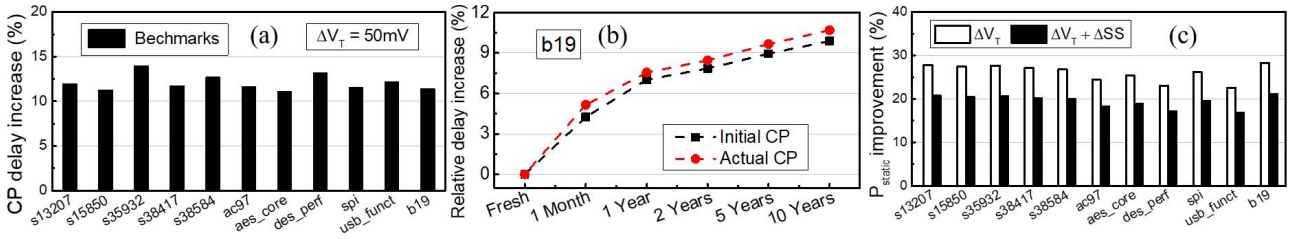

Fig. 13. (a) Impact of aging at EOL on increasing the CP delay for different circuits. (b) Delay degradation of initial CP (i.e., the path that was critical at time zero) and actual CP (the path that became critical at every time step from time zero until EOL) shows divergence with a fixed amount of device degradation for benchmark b19, signifying that CPs change after aging. (c) Static power improvement after aging can be seen at circuit level as well.

F. Logic Circuit Impact Analysis

Fresh cell library is used to synthesize (termed as time zero synthesis) different benchmark circuits [40] using a standard EDA tool [41]. The size and logic depth [defined as a number of gates between initial and terminal flip-flop of the critical path (CP)] of different circuits are listed in Table I. The impact of aging is evaluated using the static timing analysis (STA) tool [41] using aging-aware standard cells together with the time zero synthesized gate-level netlist. The results in Fig. 13(a) show the CP delay degradation that ranges from ∼11% to 14% for 50-mV V_T shift. It is noteworthy that most standard cells in the library under different input slew and output load conditions also degrade in similar magnitude for the same device-level degradation (as used in this case), see the histogram plot of Fig. 12(a), where the mean standard cell delay degradation is ∼15%, although the distribution is skewed toward larger magnitude.[8]

One of the consequences of aging is that the CP alters over time. In the case of a fixed amount of degradation assigned to all the transistors in a gate, the CP degradation (also the corresponding reordering effect) is taken into account by the STA tool. Such a worst case analysis, in which the activity dependence is not considered, would most likely provide an upper bound of the aging impact on circuits. Importantly, the ordering of the CPs would be changed when the gate-level netlist of a circuit is analyzed using the aging-aware cell library (i.e., the characterized cell library for a fixed threshold voltage shift). In other words, the path that was critical at time zero would be not likely to remain as critical when the timing analysis for the circuit's netlist is performed using the aging-aware cell library, while another path that was originally noncritical would become critical. The key reason is that the delay of gates within the cell library is nonuniformly affected for the same fixed degradation (e.g., 50 mV), as shown in Fig. 12(a) and (b). To investigate whether fixing a constant V_T shift will change the ordering of the CPs or not, we traced the initial CP (i.e., the CP at time zero) in the circuit's netlist at different time steps until the EOL. At every time step, we report the delay of initial CP and compare it with the delay of the actual CP (i.e., the new path that has become critical after aging). As shown in Fig. 13(b), in all time steps until EOL, the original CP did not remain critical and always there is a noticeable difference between the delay of the initial CP and the delay of the actual CP. Fig. 13(b) shows the analysis for one circuit (b19). However, we repeated the analysis for other circuits and found the same observation.

Fig. 13(c) shows the OFF-state power savings for the circuits at EOL. Reduction in P_{static} ranges from ∼17% to 21% depending on the circuit architecture. However, the amount of reduction in P_{static} is suppressed compared to

[8]In a chain of gates, there exist signal transitions that occur in both the directions, i.e., low to high and high to low. Though NBTI results in the degradation of the low-to-high delay, the high-to-low delay is unaffected or marginally improved due to the change in pMOS strength. In a chain of gates, this effect leads to a rectifying effect and results in a degradation, which is lower than expected. It is interesting to note that most standard cells in the library degrade similar to the CPs in magnitude.

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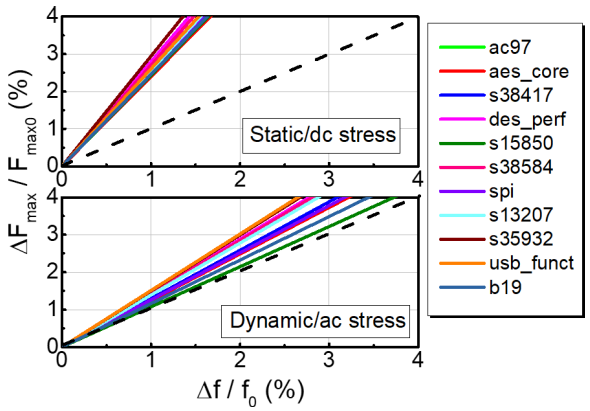

Fig. 14. Comparing the circuit F_{max} degradation with RO f degradation showing for (a) static ($\Delta V_T = 50$ mV) and (b) dynamic stress ($\Delta V_T = 25$ mV). The multiplier for RO degradation to circuit degradation is lower for dynamic stress compared to static stress.

the power savings found in standard cells. The impact due to ΔSS is reflected at the circuit level and is found to be 5%–7%.

Linear proportionality is obtained between RO f degradation and circuit F_{max} degradation, both under static and dynamic stresses as shown in Fig. 14. For dynamic stress, another cell library is used for timing analysis, assuming ac–dc ratio of 0.5. Larger than the unity slope (i.e., circuit degradation higher than RO degradation) is always obtained for static stress, whereas dynamic stress results in a correlation factor (or the multiplier for RO f degradation to circuit F_{max} degradation) closer to unity, which has been obtained for conventional paths in [37]. Note that in some cases, the circuit F_{max} degradation can be lower than that of RO degradation, though for majority of circuits, the correlation is close to unity.

III. Conclusion

A comprehensive simulation framework is demonstrated for aging analysis at 14-nm node FinFET technology-based logic circuits. Improved aging-aware FinFET-based cell libraries, considering that the effect of both threshold voltage degradation and subthreshold slope degradation are created for more accurate timing and power prediction for circuits. Impact of SS degradation on OFF-state leakage is highlighted for a wide variety of designs. Circuit F_{max} degradation is compared with the RO frequency degradation under both static and dynamic stresses. The multiplier is found to be less for dynamic case than obtained for static stress.

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