Investigation of Logic Circuit Soft Error Rate (SER) in 14nm FinFET Technology

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***Abstract*— This paper presents characterization results of soft error rate (SER) on logic circuits manufactured with 14 nm High-k/metal gate bulk FinFET technology. The FinFET SER advantage seen on SRAM was also validated on logic circuits (5-10X improvement). Alpha irradiation results reveal that charge collection only on NMOS on low critical charge can contribute to SEU. Adding NMOS on low critical charge can increase error rate, yet it can be easily mitigated by the design change. Design schemes for low-power has little impact to the SER. Single event transient on clock-line in 14 nm FinFET was substantially improved from planer-MOS.**

Keywords—soft error; alpha; SEU; SET; logic.

I. INTRODUCTION

FinFET bulk devices, quasi-SOI in nature, showed the advantage against soft-error in 22 nm FinFET technology [1]. Keeping the advantage with shrinking SRAM size was further confirmed [2], [3]. Despite the SER benefits, soft-error in logic circuits is a critical issue in reliability demanding products. The logic soft error can be difficult to recover by algorithmic techniques like error correction code. Although the dual module design can cover the logic soft error, the overheads to area and power are huge, twice or more. The accurate SER evaluation on logic is important for avoiding both the risk by logic soft error and excessive hardened design.

In this paper, we present soft error susceptibilities of logic circuit and compare with that of SRAM in 14 nm FinFET technology. We evaluate single event upset in flip-flop (SEU_{FF}), single event transient in clock buffers (SET_{clock}) and SET in combinational logic (SET_{comb}) through alpha irradiation test with various test conditions.

II. TEST PROCEDURE

We performed alpha irradiation test with 241-Amerisium alpha source in room temperature. The test chip was assembled with wire-bonding package opened on BEOL. The distance between the alpha source and silicon die was less than 1 mm. The testing was conducted in compliance with JESD89A [4].

The test chip is implemented with 5 types of shift resisters consisting of FF1, FF2, FF3, FF4, and FF5, respectively. The FFs are normal positive edge triggered flip-flops (Fig. 1) [5]. Three delay elements are between FFs for avoiding hold timing violation. Table I summarized the FFs functions. Output drive strength of FF2 is twice of FF1. FF3 and FF4 have scan function. FF4 was designed for low-power. FF5 has reset function. Table II shows critical charge (Q_{crit}), which is the minimum charge for occurring SEU.

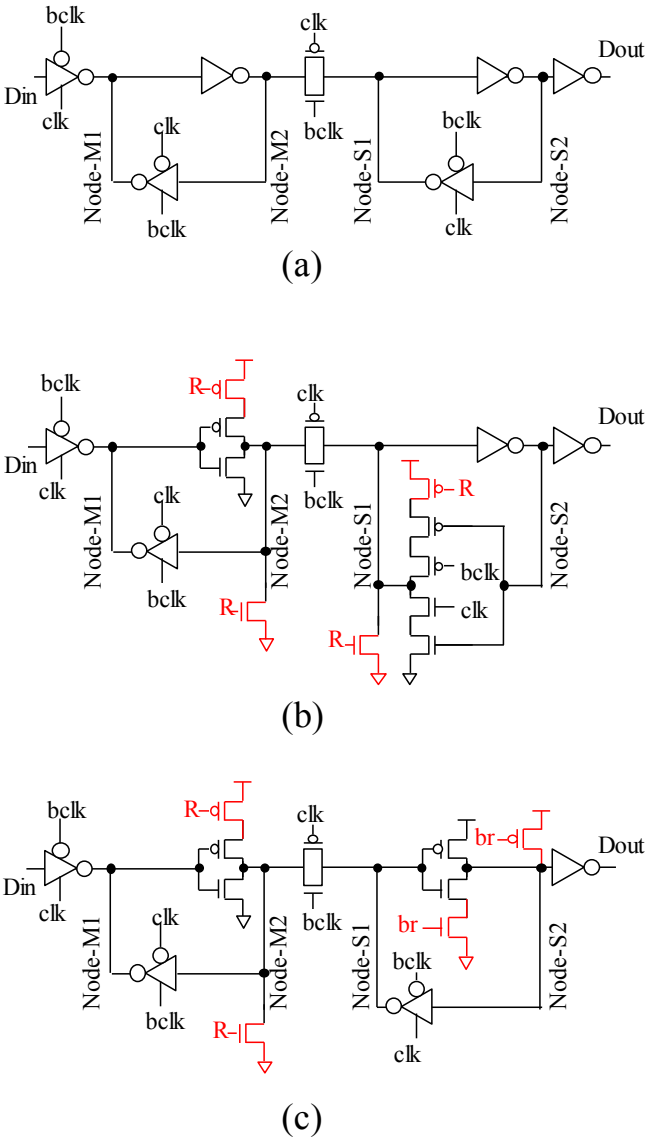

Fig. 1. Schematic of (a) FF1, (b) FF5 and (c) a sample for attenuating alpha induced SEU in resettable flip-flop. These FFs are general design [5]. The 'R' and 'br' show reset and reset-bar signal terminals. The node name corresponds with Table III.

TABLE I. LIST OF FLIP-FLOPS IN THE TEST CHIP

Name	Scan	Reset	Drive	Low Power
FF1	No	No	1X	No
FF2	No	No	2X	No
FF3	Yes	No	1X	No
FF4	Yes	No	1X	Yes
FF5	No	Yes	1X	No

TABLE II. Q_{CRIT} ON 14 NM FINFET FF1 AND FF5. THE NODE NAME CORRESPONDS WITH FIG. 1. NOTE THAT Q_{CRIT} IN 14 NM FINFET SRAM IS 0.7 FC [2].

Node name	FF1	FF5
Node-M1	1.3 fC	1.4 fC
Node-M2	4.1 fC	3.6 fC
Node-S1	1.3 fC	1.3 fC
Node-S2	3.6 fC	3.8 fC

We performed irradiation tests in flip-flops with 8 signal conditions. The sensitive area of soft-error on each condition is shown in Table III. The sensitive area is determined by the data state on each node because of charge collection only on off state transistor [6]. The written data are ALL0/1 and checker board (CHB) patterns. The clock signal kept high or low for static test (RUN1-6), and operated with 1 kHz (RUN7) and 10 MHz for dynamic test (RUN8).

III. SEU RESULT

Table IV and Fig. 2 summarizes alpha induced SEU rates in 14 nm FinFET SRAM and flip-flop. SEU_{FF} rate is ~2X higher than SEU rate in SRAM. Larger sensitive area for SEU contributes higher SEU rate in flip-flop than in SRAM. The sensitive area is drain of data retention node. While the SRAM consists of 4 fins drain [2], the FFs consist of more than 50 fins drain on the data retention node. The ratio of SEU rate in flip-flop vs. SRAM in 14 nm FinFET technology was similar to planer-MOS [7]. SEU in SRAM was dramatically improved in 14 nm FinFET technology. Although no direct comparison to planar circuits is made at this time, it is evident that very low 14 nm SER rate, the SEU advantage seen on flip-flop is similar to that in SRAM (5-10X gain) [2]. Fig. 2 shows also voltage dependency. Voltage increase of 20% (0.88V to 0.72V) decreases SEU_{FF} rate more than half. This voltage dependency is also same with 14 nm FinFET SRAM [2].

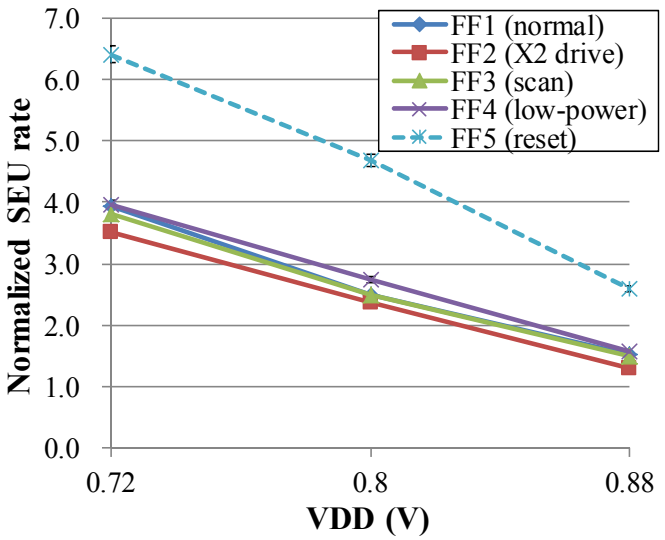

Fig. 2. SEU rates on FF1 (normal), FF2 (X2 drive), FF3 (scan), FF4 (low-power), FF5 (reset) normalized with SEU rate in 14 nm FinFET SRAM at 0.8 V.

TABLE III. SOFT ERROR SENSITIVE TRANSISTOR ON EACH TEST CONDITION, AND Q_{CRIT} OF FF1. THE NODE NAME OF SENSITIVE AREAS CORRESPOND WITH FIG. 1.

			SEU								SET				
			Master latch				Slave latch				Local clock buffer				Comb. logic
			Node-M1		Node-M2		Node-S1		Node-S2		bclk		clk		
			Q_{crit}=1.3 fC		Q_{crit}= 4.1 fC		Q_{crit}= 1.3 fC		Q_{crit}= 3.6 fC		Q_{crit}= 2.7 fC		Q_{crit}= 3.6 fC		
	Clock	DATA	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	
RUN1	Static (high)	ALL0	✓			✓									
RUN2	Static (high)	ALL1		✓	✓										
RUN3	Static (low)	ALL0						✓	✓						
RUN4	Static (low)	ALL1					✓			✓					
RUN5	Static (high)	CHB	✓	✓	✓	✓						✓	✓		
RUN6	Static (low)	CHB					✓	✓	✓	✓	✓			✓	
RUN7	Dynamic(1kHz)	CHB	✓	✓	✓	✓	✓	✓	✓	✓					✓
RUN8	Dynamic(10MHz)	CHB	✓	✓	✓	✓	✓	✓	✓	✓					✓

TABLE IV. SOFT ERROR SENSITIVE TRANSISTOR ON EACH TEST CONDITION, AND Q_{CRIT} OF FF1.

	Q_{crit} (fC)	Cell size	SEU rate
SRAM [2]	0.7	1.0	1.0
FF1 (w/o reset)	1.3	12.6	2.7
FF5 (w/ reset)	1.3	15.4	4.3

TABLE V. SOFT ERROR SENSITIVE TRANSISTOR AND Q_{CRIT}.

	Q_{crit} < 3.6fC (Node-M1, -S1)	Q_{crit} > 3.6fC (Node-M2, -S2)
PMOS	No sensitive	No sensitive
NMOS	Sensitive	No sensitive

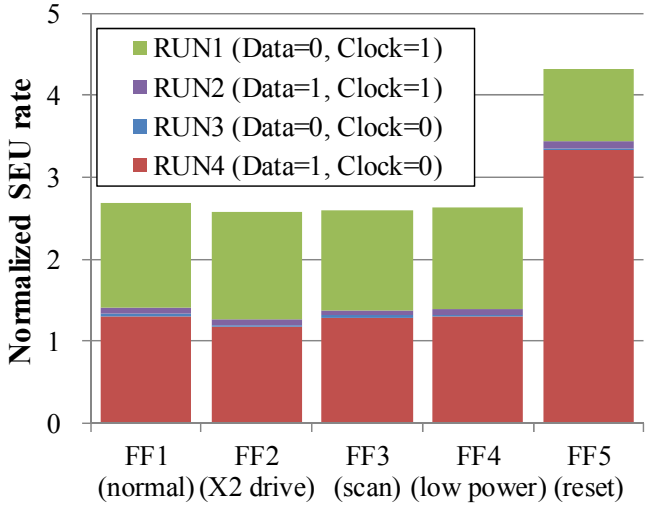

Fig. 3. Test results in 4 static test conditions (RUN1, 2, 3 and 4) at 0.8 V. The SEU rates are normalized with SEU rate in 14 nm FinFET SRAM at 0.8 V.

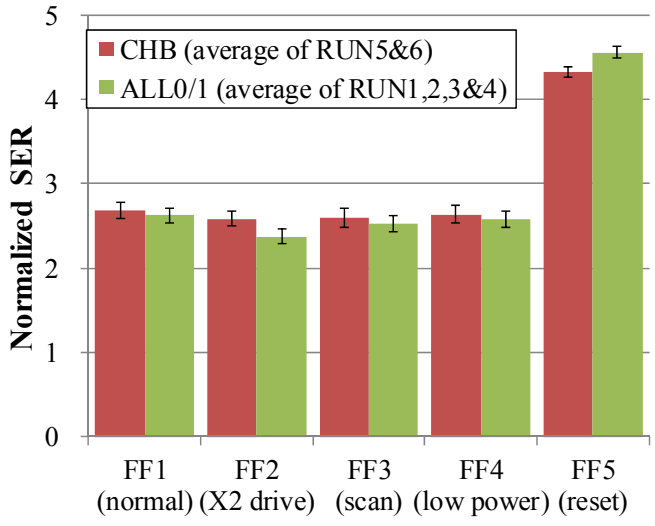

Fig. 4. Error rates in CHB and ALL0/1 data patterns. The values are normalized with SEU rate in 14 nm FinFET SRAM at 0.8 V

The static test results (Fig. 3) indicated that Alpha SEU_{FF} almost never occurred by the charge collection on PMOS or over 3.6 fC of Q_{crit} as shown in Table V. The conclusions are from the result of RUN2 and 3 in which SEU_{FF} was almost never observed. The sensitive areas on RUN2 and 3 are NMOS with large Q_{crit} and PMOS with small Q_{crit} as shown in Table II and Table III. These sensitive areas do not contribute to SEU. This means that both NMOS on high Q_{crit} and PMOS on low Q_{crit} did not contribute to SEU_{FF}.

Above SEU_{FF} trends are reconfirmed in comparison between the test results on FF1 (w/o reset, Fig. 1 (a)) and FF5 (w/ reset, Fig. 1 (b)). **RUN1:** SEU rate on FF5 is not higher than in FF1 even though FF5 have additional NMOS and PMOS on NODE-M2 for reset function. **RUN3:** SEU rates are no different between FF5 and FF1 even though FF5 have additional PMOS on low Q_{crit} node (NODE-S1). **RUN-4:** SEU rate increase from FF1 to FF5 because FF5 has additional NMOS in NODE-S1 (Q_{crit} = 1.3 fC). These results reconfirm that charge collection only on NMOS on low Q_{crit} occurs SEU_{FF}.

Reducing the NMOS area on low Q_{crit} node can easily to attenuate alpha induced SEU_{FF} rate. Fig. 1 (c) shows an example schematic of the resettable flip-flop design improved alpha induced SEU_{FF}. NMOS for reset function connects only to high Q_{crit} node (Node-M2 and -S2). This flip-flop can be expected same level SEU rate with FF1.

The test results show also that other design changes have no risk of increasing SEU_{FF}. Scan function (FF3) and 2X drive strength output of flip-flop (FF2) are little impact to the SEU_{FF} rate. Multiplexer for scan function and enlarging output buffer for 2X drive output do not increase drain area on the data storage node. The low-power design is also little impact to soft-error (FF4).

IV. SET RESULT

The 14 nm FinFET technology has strong advantage against alpha induced SET_{clock}. The test results (Fig. 4) show that SET_{clock} rate is negligibly small in 14 nm FinFET although SET_{clock} rate was more than 10% of SEU_{FF} in planer-FET flip-flops [6]. The SET_{clock} rates are evaluated from difference of results in CHB and ALL0/1 data pattern. A flip-flop stores different data of the previous stage FF in CHB. The retention data can be rewrite with previous stage data by a clock edge generate by SET on clock line. Then, both SEU_{FF} and SET_{clock} are counted in CHB. In ALL0/1, only SEU_{FF} is observed.

Fig. 5 shows error rate on 1 kHz and 10 MHz dynamic tests. SET_{comb} rate can be calculated by the difference of error rates on different frequency since SET_{comb} rate is proportional to clock frequency [1]. The SET_{comb} rate on 1 kHz is negligibly small from the result shown in Fig. 6. The error rate on 10 MHz includes 10,000 time of SET_{comb} of on 1 kHz. So, the differences of error rate on 1 kHz and 10 MHz dynamic tests show SET_{comb} rate.

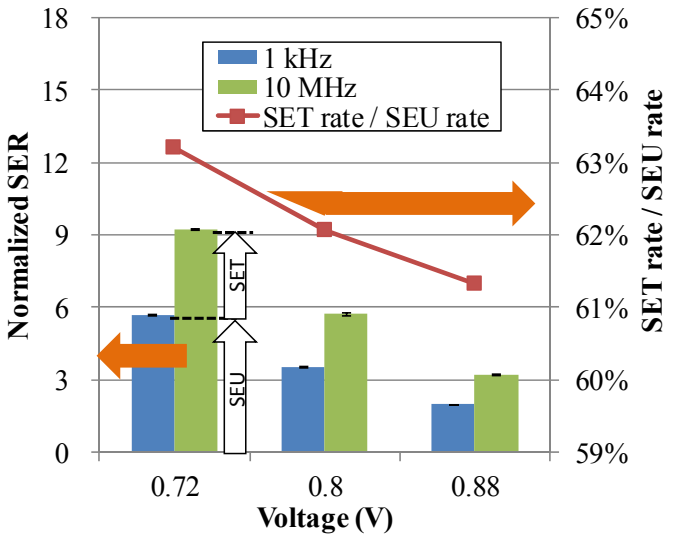

Fig. 5. Error rate on dynamic test with 1 kHz (RUN7) and 10 MHz (RUN8), and SEU ratio (SET rate / SEU rate). The error rates are normalized with SEU rate in 14 nm FinFET SRAM at 0.8 V.

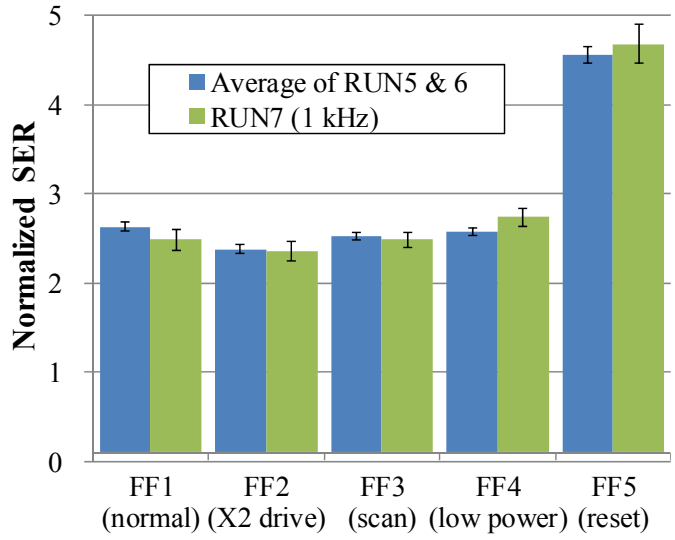

Fig. 6. Test results in static test conditions (average of RUN5 and 6) and dynamic test condition (RUN7) at 0.8 V. The error rates are normalized with SEU rate in 14 nm FinFET SRAM at 0.8 V.

The test chip was effectively designed for evaluating SET_{comb} rate even in low clock frequency. The observed SET in the test chip can be generated in the slave latch of previous stage and delay elements between FFs. The combinational logic in this test chip was designed with short stage for avoiding SET pulse attenuation. The delay element consists of small and large inverters (INVs) for high SET sensitivity. Output of large INV gives large sensitive volume for charge collection, and input of small INV gives small capacitance. The connection of the output of large INV and the input of small INV gives high SET sensitivity.

The test circuit structure can qualitatively evaluate SET effect like voltage dependency with small circuit without high frequency operation. The SEU rate decrease with voltage because increasing the quantity of electric charge and the feedback current increase Q_{crit}. In case of SET, increasing the quantity of electric charge, not feedback current, contributes the Q_{crit} increase. As a result, the voltage dependency on SET and SEU rates are different and the SET_{comb} ratio changes.

V. Conclusions

The FinFET technology provided huge advantage (5-10X gain) in SER in the same way in logic as well as in SRAM. Alpha irradiation results reveal that charge collection only on NMOS on low Q_{crit} can contribute to SEU. Adding NMOS drains on low critical charge node can potentially increase the error rate, yet it can be easily mitigated by small design change. Other design changes have no added risk of increasing SEU_{FF}. SET_{clock} rate is negligibly small, and FinFET technology improves alpha induced SET_{clock}. The SET_{comb} was also evaluated effectively, and shows the voltage dependency on SET probability to SEU rate.

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References

[1] N. Seifert, B. Gill, S. Jahinuzzaman, J. Basile, V. Ambrose, Q. Shi, R. Allmon, and A. Bramnik, "Soft Error Susceptibilities of 22 nm Tri-Gate Devices," *Nuclear Science, IEEE Transactions on*, vol. 59, no. 6, pp. 2666–2673, Dec. 2012.

[2] S. Lee, I. Kim, S. Ha, C. Yu, J. Noh, S. Pae, and J. Park, "Radiation-induced soft error rate analyses for 14 nm FinFET SRAM devices," in *Reliability Physics Symposium (IRPS), 2015 IEEE International*, 2015, pp. 4B.1.1–4B.1.4.

[3] N. Tam, B. L. Bhuva, L. W. Massengill, D. Ball, M. McCurdy, M. L. Alles, and I. Chatterjee, "Multi-cell soft errors at the 16-nm FinFET technology node," in *Reliability Physics Symposium (IRPS), 2015 IEEE International*, 2015, pp. 4B.3.1–4B.3.5.

[4] JEDEC, "Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray Induced Soft Error in Semiconductor Devices: JESD89A," *JEDEC Sold State Technol. Assoc.*, pp. 1–85, 2006.

[5] V. G. Oklobdzija, V. M. Stojanovic, D. M. Markovic, and N. M. Nedovic, *Digital system clocking: high-performance and low-power aspects*. John Wiley & Sons, 2005.

[6] T. Uemura, Y. Tosaka, H. Matsuyama, K. Shono, C. J. Uchibori, K. Takahisa, M. Fukuda, and K. Hatanaka, "SEILA: Soft error immune latch for mitigating multi-node-SEU and local-clock-SET," in *Reliability Physics Symposium (IRPS), 2010 IEEE International*, 2010, pp. 218–223.

[7] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Dependable Systems and Networks, 2002. DSN 2002. Proceedings. International Conference on*, 2002, pp. 389–398.