Evaluating the Impact of Process Variability and Radiation Effects on Different Transistor Arrangements

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***Abstract*—The high integration capacity of digital circuits, which occurs due to technological scaling, presents new challenges for nanotechnology designs. The evolution of integrated circuits has made them more susceptible to faults, besides increasing the process variability, which can lead to circuits operating outside their specification ranges. This work evaluates the effects of process variability and radiation faults on complex gates. These effects are compared to alternative circuits that implement the same functions but exploring a multi-level of basic cells as NAND2, NOR2 and Inverters. The technology adopted is 7nm FinFET ASAP. Results show that although complex cells present better timing and power results, multi-level circuits are up to 28% less sensible to radiation faults and about 40% more stable under process variability.**

***Index Terms*—process variability, radiation effects, complex gates, FinFET technology**

I. Introduction

The evolution of the transistors manufacturing process has been happening at an impressive speed. The technology scaling increases the integration capacity of integrated circuits and also allows operating frequencies to become increasingly high. Nowadays, integrated circuits have an essential role in practically every one of our daily tasks, at the cost of these circuits have become increasingly dense and complex.

By contrast, new challenges were introduced in the design of integrated circuits due to scale down, such as increased manufacturing process variability [1], Short-Channel Effects (SCE), leakage current [2] and increased susceptibility to radiation effects. Moreover, Bulk CMOS technology has reached its geometrical and physical limit. Bulk MOSFET devices have been used in the integrated circuits design for several decades. However, at each new technology node, Bulk MOSFET devices suffer from the undesirable leakage currents, soft errors and SCE [3] [4]. The use of multi-gate devices is an option to overcome these obstacles and continue the technology scaling because these devices provide better control of SCE, lower leakage and better yield [5]. FinFET (Fin-Shaped Field Effect Transistor) technology is used as the main multi-gate device replacing MOSFET devices in sub-22nm technology nodes [6].

The focus of this work is the variability and the faults arising from the radiation effects. Few works address these two effects together on the circuit design. Few solutions are found in the literature to mitigate the impact of process variability. Transistor arrangement is a technique explored to design faster circuits [7], but also to deal with Bias Temperature Instability (BTI) effects [8] or improve design robustness against permanent and transient faults. Adoption of complex gates reduce the transistor number that is correlated to the area and also reduce the delay and power consumption, but complex gates could introduce challenges related to regularity and reliability that might be avoided with more regular and basic cells.

The main objective of this work is to evaluate the impact of process variability and Single Event Transient (SET) on a set of complex logic gates considering different transistor topologies. A comparison is made between complex logic gates in their traditional versions and a multi-level of basic logic gates that implement the same function using NAND2, NOR2 and Inverter cells in FinFET technology.

Section II introduces some FinFET properties. The process variability and radiation effects concepts are shown in Section III. The methodology utilized in experiments is presented in Section IV. Section V explains the impact of process variability and radiation effects on different transistor arrangements. Finally, conclusions are displayed in Section VI.

II. FinFET Technology

FinFET devices have vertical silicon structures to form the channel region and to connect the source and drain regions at each end [6]. The gate region is wrapped around this vertical structure, named as the fin. MOS channels are formed at the two sidewalls. The ON current (I_{ON}) of these devices is a function of the sum of the drive currents contributed by the two side-gate transistors. This fin-like geometry, where the depletion regions reach from the gates entirely into the body region implies that no free charge carriers are available, making the suppression of SCE possible in FinFETs [9]. Fig. 1, presents FinFET key geometric parameters [10]: Gate length (L_G/L_{FIN}), fin height (H_{FIN}) and fin width/thickness (W_{FIN}/T_{SI}).

FinFET devices variability hardly affects the currents behavior, especially the static current [11]. On multi-gate devices,

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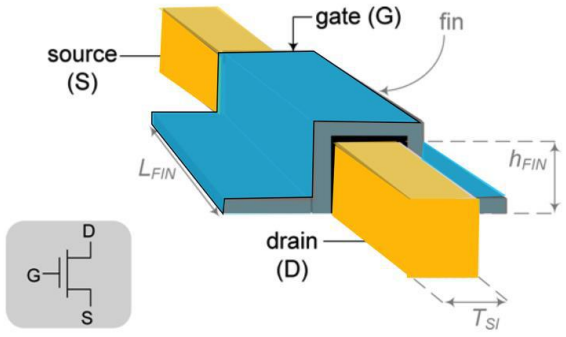

Fig. 1. Structure and geometric parameters of FinFETs [10].

variability effects are mainly due to the work function fluctuation (WFF) of the metal gate [6] [12].

III. Process Variability and Radiation Effects

The reduction of device dimensions has increased the importance of studying the reliability issues of integrated circuits. Thus, this section presents the main characteristics of two of the most significant adverse effects on the reliability of these circuits: Process Variability and Radiation Effects.

Circuits exposed to radiation, may suffer alterations and disturbances, impairing their correct functioning. The integrated circuits that experience the interaction of ionizing particles suffer two types of degradation: those of singular character, that occur due to the incidence of a single particle, and the ones of cumulative nature, which occur due to the accumulation of doses of ionizing radiation over the life of the circuit. This work addresses the effects of the incidence of a single particle, the Single-Event Effects (SEE).

An SEE occurs when a single particle hit the device, ionizing and releasing energy that can damage the device permanently or induce transient effects. The most common transient effects on combinational circuits are the SET, where the incidence of an ionized particle produces a transient pulse that can propagate through a logic path and be latched by memory elements. At a particle collision with silicon, the effects are: 1) the deposition of an additional charge on the affected device; and 2) the charge collection step proceeds through mainly Drift and Diffusion process.

Drift occurs when the high-intensity electric field rapidly collects the additional carriers deposited by the ion in this region if the resulting ionization path crosses the depletion region formed at the P-N junctions [13]. However, diffusion dominates the collection process by collecting all the remaining carriers that were generated besides the depletion layer [14]. After this collection process, a transient pulse is observed in the affected node. At nanometer nodes, it is verified an increase in the susceptibility of the circuit relative to the noise from the environment and particularly the incidence of particles of radiation [15]. Even particles with low energy that reach the Earth surface, previously overlooked, they are now able to interfere with the operation of a circuit.

Variability can be divided into three factors: environmental factors, reliability factors and physical factors [16]. The environmental factors appear during the operation of a circuit. Power supply and temperature variations are examples of environmental factors. The reliability factors are related to the aging of the transistor, due to the high electrical fields presented in modern circuits. Finally, the physical factors are associated with variations in the electrical parameters, which can occur due to the manufacturing process.

The primary sources of process variability at nanometer nodes are due to the sub-wavelength lithography [17] [16]. Variability on geometric parameters due to lithography impact directly the transistor threshold voltage (V_{th}). These variations can compromise entire blocks of cells or reduce the performance and energy efficiency of the chip.

From the beginning of FinFET devices adoption on digital circuits, many works strengthened the relevance of considering the impact of variability on FinFET devices to estimate how it will impact the design and guaranteed functional devices [3] [18] [19] [20].

The most significant parameter for the process variability effects is WFF. WFF is caused by the dependency of metal work-function on the orientation of its grains, as depicted in Fig. 2. A high correlation between the variability in I_{ON} and I_{OFF} currents and threshold voltage fluctuation in the presence of granularity of the metal gate (MGG) [19] is presented by the parameter. In the ideal fabrication process, metal gates devices have the gates produced with metal uniformly aligned and very lower WFF deviation. Nevertheless, in the real manufacturing process, metal gate devices are generally built with metals having different work-functions (Φm) randomly aligned which causes higher WF variation.

IV. Methodology

This work evaluates the impact of process variability and radiation effects on different transistor arrangements. Three logic functions were chosen (AOI22, OAI211 and XOR) and four different transistor topologies are explored (complex gate, only NAND2, only NOR2 and NAND2/NOR2/INV) to perform this analysis. For the complex gate transistor topology, the functions are optimized and designed as a complex logic gate

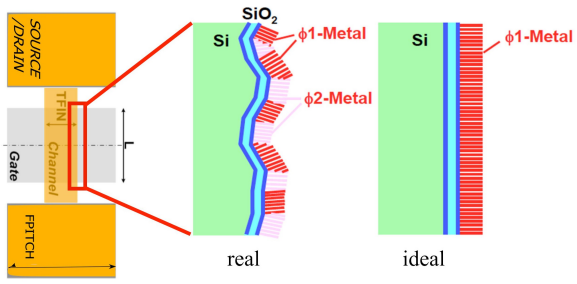

Fig. 2. Metal gate fabrication in the ideal and real aspects [11].

CMOS topology. Then, the functions are converted using De Morgan's theorem into the three other transistor arrangements, in a way that only basic cells are employed. Tables I, II and III show the complex functions of each complex gate and its respective functions converted using only NAND2 gates, only NOR2 gates and NAND2/NOR2/INV gates.

TABLE I
COMPLEX AND CONVERTED FUNCTIONS OF XOR GATE

Transistor Arrangement	XOR
Complex Gate	Y = A.B' + A'.B
NAND2	Y = ((A . (B.B)')' . ((A.A)' . B)')'
NOR2	Y = ((((A+A)' + B)' + (A + (B+B)')')' + (((A+A)' + B)' + (A + (B+B)')')')'
NAND2/NOR2/INV	Y = ((((A.B')')' + ((A'.B)')')')'

TABLE II
COMPLEX AND CONVERTED FUNCTIONS OF OAI211 GATE

Transistor Arrangement	OAI211
Complex Gate	Y = (A+B . C.D)'
NAND2	Y = (((A.A)' . (B.B)')' . ((C.D)' . (C.D)')')'
NOR2	Y = (((A+B)' + ((C+D)' + (C+D)')')' + ((A+B)' + ((C+D)' + (C+D)')')')'
NAND2/NOR2/INV	Y = ((((A'.B')')' + (C.D)')')'

TABLE III
COMPLEX AND CONVERTED FUNCTIONS OF AOI22 GATE

Transistor Arrangement	AOI22
Complex Gate	Y = (A.B + C.D)'
NAND2	Y = (((A.B)' . (C.D)')' . ((A.B)' . (C.D)')')'
NOR2	Y = (((A+A)' + (B+B)')' + ((C+C)' + (D+D)')')'
NAND2/NOR2/INV	Y = ((((A'+B')')' . (C+D)')')'

Electrical simulations with the HSPICE tool were made using the 7nm FinFET technology from ASAP7 [21] to perform all steps of this work. Table IV resumes the main parameters of the 7nm FinFET ASAP7 technology. In the experiments, the transistor sizing considers all transistors with three fins for all circuits [22]. The nominal supply voltage of the model adopted is 0.7V. The minimum switching frequency of the input signals was 500MHz, and four inverters (Fanout 4) were used as the load at the output of the circuit.

The analysis of this work can be divided into three stages: (1) nominal, (2) process variability and (3) radiation effects. In addition to comparing the results obtained in each stage, a general comparison of the results is also performed. The objective is to highlight which transistor arrangement presents the best results aiming only process variability and only transient faults, but also to give the topology that has an ideal average behavior in the three stages studied.

A. Nominal Conditions

This stage evaluates the circuits at nominal conditions, i.e., process variability and radiation effects are not considered. In this step, the propagation times and the total power consumption of the three complex gates in their different

TABLE IV
7NM FINFET ASAP7 MAIN PARAMETERS [21]

Parameter		7nm
Supply Voltage		0.7V
Gate Length (L_G)		21nm
Fin Width (W_{FIN})		6.5nm
Fin Height (H_{FIN})		32nm
Oxide Thickness (Tox)		2.1nm
Channel Doping		$1\times10^{22}m^{-3}$
Source/Drain Doping		$2\times10^{26}m^{-3}$
Work Function	**NFET**	4.3720eV
	PFET	4.8108eV

arrangements are compared. The objective is to analyze the typical characteristics of each gate and each arrangement. Nominal values are used as a form of reference values to evaluate the variability and radiation effects.

B. Process Variability

The analysis considering the effects of process variability is performed at the second stage. Metal gate work-function exhibits a multi-nominal distribution, which can be approximated by a Gaussian distribution if the number of grains on the surface of metal-gate is high enough ($>$10) which corresponds to the FinFET ASAP7 model characteristics. Thus, the WFF of each device is varied according to a Gaussian distribution with a 3-sigma deviation of 3% [11] the WFF. Two thousand simulations were run for each logic gate [23]. Timing and power consumption measurements were taken for each Monte Carlo simulation. Robustness analysis was performed using the sigma/mean ratios (called deviation) of each delay arc, always aiming at the worst case.

C. Radiation Effects

The third stage considers the effects of radiation through the insertion of transient faults. The SET fault injection is modeled as the Messenger's equation shown in Eq. 1, where *Qcoll* is the collected charge, τ_α ($1.64\times10^{-10}s$) is the collect charge timing constant, τ_β ($5\times10^{-11}s$) is the timing constant to establish the ion track and *L* (2μm) is the charge collection profundity [24]. This effect is reproduced on the SPICE simulation as a current source, simulating the SET effects on the transistors.

$$I(t) = \frac{Qcoll}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \qquad (1)$$

$$Qcoll = 10.8\times L\times LET$$

This work follows the parameter and methodology presented in [25], investigating the effects of SET 010 and 101 in all devices of the two inverter circuits. Thus, a current source is inserted into each internal node and the output of the circuit. Also, this evaluation considers all the input vectors for the selected logic gates.

The simulation adopts a linear energy transfer (LET) of $1MeV - cm^2/mg$. The fault is detected if the output of

the circuit is bigger than $V_{DD}/2$ for logic level '0' and smaller than $V_{DD}/2$ for logic level '1'; otherwise, the fault is considered masked. The fault masking is determined by Eq. 2, considering the ratio between the number of faults detected and the total inserted faults, i.e., a fault entered in each internal node and the output, for each test vector of the circuit. For example, a logic gate with four inputs has 16 test vectors, if this same gate has five internal nodes plus the output, there would be 96 inserted faults in the circuit.

$$Fault\ Masking = \frac{Faults\ Detected}{Total\ Inserted\ Faults} \quad (2)$$

V. Results

To compare the different transistor topology and to identify common characteristics to mitigate process variability and radiation effects, the results of the set of experiments performed in this work is organized into three main parts, as the methodology described: nominal behavior, process variability impact and radiation effects on the circuits.

A. Nominal Behavior

Complex gates reduce the number of literals in the equations and, consequently, this reflects on the fact that with this transistor arrangement, all the three functions evaluated presented better timing and power results. Fig. 3, compares the maximum transition time for all arches of each evaluated function. NAND2 version is about 18% slower than Complex gate versions, but NOR2 circuits could insert more than twice times of delay degradation on the OAI211 gate.

The impact of the use of different arrangements is even worse, when the total power consumption considering all timing arches, is analyzed. Fig. 4, shows that multi-level versions (NAND2, NOR2 and NAND2/NOR2/INV) consumes at least 49% more than complex gate circuits. The XOR gate has the smallest increase in power consumption (49.4%) in NAND2 version, while the AOI22 gate in NOR2 version has the most significant growth, around 129%.

Thus, to optimized circuits addressing power and timing reduction, the complex gate is the best alternative to transistor arrangement. In sequence, the evaluation of the process variability and radiation effects will throw light on these effects on complex gates and the alternative circuits evaluated.

B. Process Variability

Process variability inserts oscillations on the delay and power consumption compared to the results presented in the nominal behavior evaluation. In general, complex gate circuits under process variability show the most significant variation in the delay compared to nominal behavior, reaching up to 5% on the worst case delay. Multi-level circuits presented a difference on the mean delay of 4%, 3% and 2% for NAND2, NOR2 and NAND2/NOR2/INV alternative circuits. However, complex gate and NAND2/NOR2/INV versions present mean power values statistically identical to the nominal results,

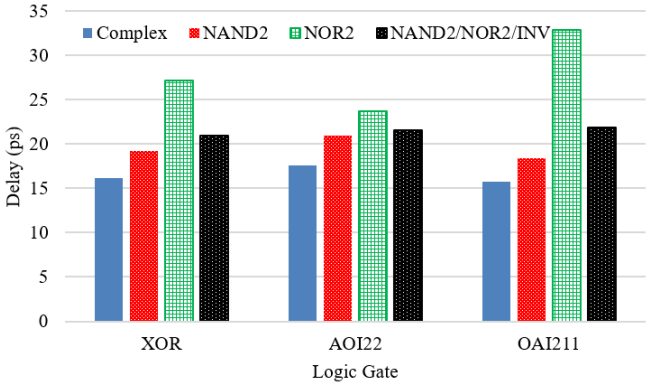

Fig. 3. Delay at nominal conditions.

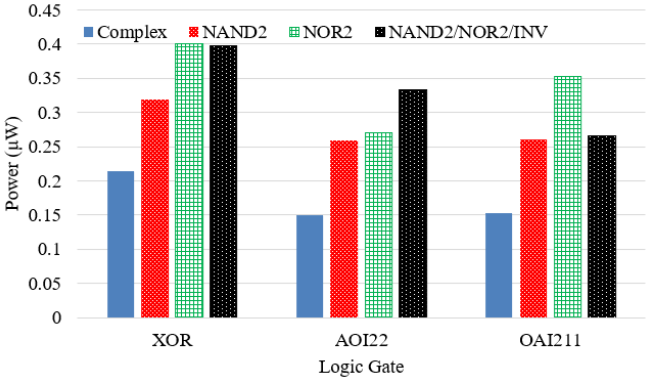

Fig. 4. Power at nominal conditions.

despite the large standard deviations. Table V shows the mean and standard deviation values obtained from the Monte Carlo simulation.

To compare the effects of process variability, considering both mean and standard deviation, are presented in Fig. 5 and Fig. 6 respectively, the deviation results for delay and power. All the circuits demonstrate more sensibility on delay due to process variability than on power results, as we are analyzing the normalized standard deviation and not the absolute values

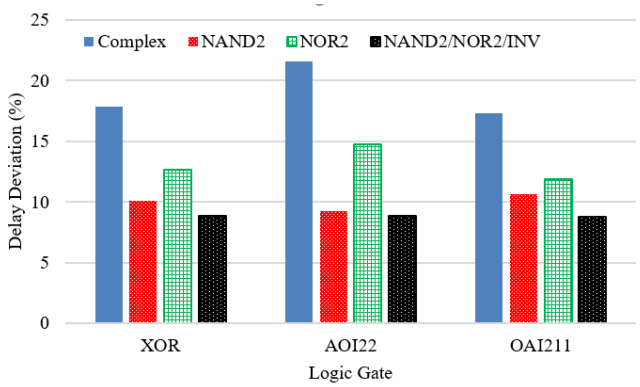

Fig. 5. Delay deviation due to process variability.

TABLE V
MEAN AND STANDARD DEVIATION RESULTS FOR POWER AND DELAY

Complex Gate	Measures	Complex		NAND2		NOR2		NAND2/NOR2/INV	
		Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma
XOR	Worst delay (ps)	17.1	3.1	19.7	1.9	28.2	3.6	21.5	1.9
	Power (nW)	213.8	9.8	311.8	15.6	401.3	17.8	394.6	23.2
AOI22	Worst delay (ps)	17.3	3.7	21.6	1.9	24.7	3.6	22.0	1.9
	Power (nW)	150.4	6.3	259.9	10.7	278.5	12.8	332.2	14.1
OAI211	Worst delay (ps)	16.5	2.8	19.1	2.1	34.2	4.1	22.4	1.9
	Power (nW)	153.3	6.5	281.1	13.2	363.8	17.5	264.9	13.9

this behavior is possible. Complex gates significantly suffer the influence of process variability on delay. For all the three functions evaluated, this alternative shows the worst results with more than 15% of delay deviation. Multi-gate with basic cells alternatives demonstrates better delay robustness to process variability. NAND2/NOR2/INV shows a slight advantage compared to NAND2 versions, with a difference of 1.5%. However, NAND2 versions present less power sensibility. One of the factors that contribute to the greater robustness of the multi-level topologies is the existence of identical elements in the vicinity, this guarantees an easy impression and final verification.

In the comparison of the normalized deviation of the multi-level alternatives with the complex gates, for all functions, multi-level circuits improved the process variability robustness over 30%. AOI22 is the cell most beneficiated with the multi-level arrangements, presenting over 50% of the reduction in delay deviation.

C. Radiation Effects

From the analysis of fault masking between the complex gate and the different arrangements with basic cells, the advantage of using basic cells is evident when the objective is to mitigate transient faults. In Fig. 7, this advantage can be analyzed mainly in the topologies that use only NAND2 and only NOR2 gates. For the XOR gate, the NAND2 and NOR2 arrangements present decreases of 7% and 14% in the sensitivity to transient faults about the use of complex gates, respectively. For the AOI22 gate, this reduction is even higher,

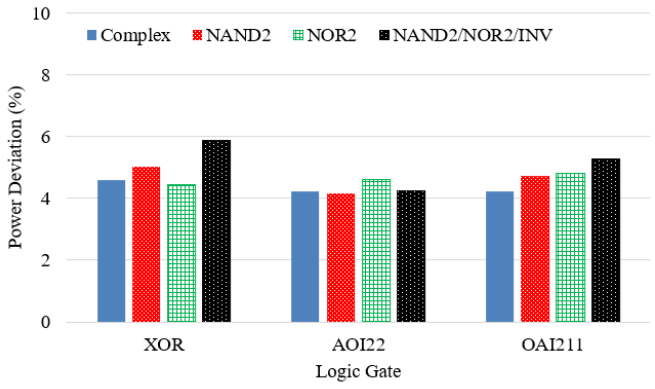

Fig. 6. Power deviation due to process variability.

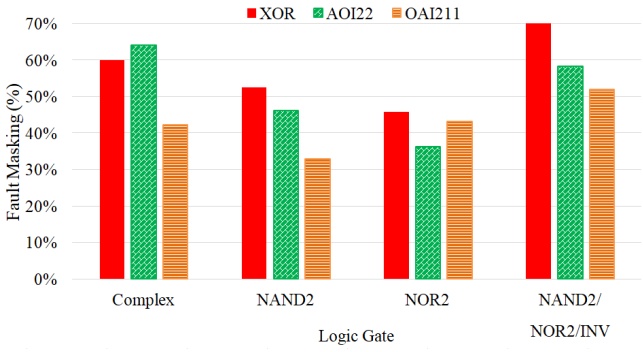

Fig. 7. Fault masking comparison.

being 18% for the topology with only NAND2 and 28% for the topology with the only NOR2.

The arrangement with NAND2 continues with the reduction of the sensitivity for the OAI211 gate, around 9%. However, the NOR2 arrangement has a small increase (1%) in the sensitivity compared with the complex gates. In general, the arrangement using NAND2, NOR2 and Inverters together does not perform well about fault masking. Only for the AOI22 gate, this topology has a sensitivity reduction (6%), whereas, for the XOR and OAI211 gates, there is an increase of 10% in the fault sensitivity. Although the NOR2 arrangement presents the highest percentages of sensitivity decrease to transient faults, the NAND2 topology is the most stable, having a significant reduction for all three gates analyzed in this study. Table VI shows the total injected faults in each logic function examined. Moreover, the number of faults masked and detected are also displayed.

VI. CONCLUSIONS

This work presented an evaluation of the influence of process variability and the radiation effects on 7nm FinFET ASAP technology. At nominal conditions, it is evident that the complex gate arrangement is the best choice to obtain less power consumption and a decrease in the propagation delay. It occurs because the complex gate topology reduces the number of transistors and the connections between them significantly. On the other hand, when the behavior of the logic gates is investigated with radiation or process variability effects, the multi-level arrangements are the best option. In comparison to complex gate topology, the XOR and AOI22 logic gates composed only by NOR2 gates can be up to 14%

TABLE VI
FAULT ANALYSIS OF ALL FUNCTIONS

Fault Analysis/ Transistor Arrangement	Logic Function											
	XOR				AOI22				OAI211			
	Complex	NAND2	NOR2	NAND2/ NOR2/INV	Complex	NAND2	NOR2	NAND2/ NOR2/INV	Complex	NAND2	NOR2	NAND2/ NOR2/INV
Inserted	20	40	48	44	64	128	224	208	64	192	192	160
Detected	12	21	22	31	41	59	81	121	27	63	83	83
Masked	8	19	26	13	23	69	143	87	37	129	109	77
Fault Masking	**60.0%**	**52.5%**	**45.8%**	**70.5%**	**64.1%**	**46.1%**	**36.2%**	**58.2%**	**42.2%**	**32.8%**	**43.2%**	**51.9%**

and 28% more fault tolerant, respectively. Similar behavior can be seen with the OAI211 gate where the arrangement with only NAND2 reaches around of 9% more fault tolerance about to the topology of complex gates.

Complex gates suffer more influence of process variations on propagation delays than the power consumption. For all logic gates analyzed, this alternative presented more than 15% of delay deviation. Compared to multi-level topologies, complex gates delay deviation impact over 30% of the stability of the functions. Finally, under the impact of radiation or process variations, better results can be found using the topologies based on multi-level arrangements. Aiming at future work more in-depth analyzes will be carried out regarding the effects of radiation. Also, the impact of the transistors sizing on these effects will also be analyzed.

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