Device to Circuit Framework for Activity-Dependent NBTI Aging in Digital Circuits

A. Thirunavukkarasu, *Student Member, IEEE*, Hussam Amrouch, *Member, IEEE*, Jerin Joe, *Student Member, IEEE*, Nilesh Goel, *Member, IEEE*, Narendra Parihar, *Student Member, IEEE*, Subrat Mishra, *Student Member, IEEE*, Chetan K. Dabhi, *Student Member, IEEE*, Yogesh S. Chauhan, *Senior Member, IEEE*, Jörg Henkel, *Fellow, IEEE*, and Souvik Mahapatra, *Fellow, IEEE*

***Abstract*— A framework is proposed for activity-dependent timing degradation due to p-FET negative bias temperature instability (NBTI) in digital circuits. A fixed-time compact model is proposed for NBTI and validated with physical model predictions for various digital circuits under different input signal slew and fan-out load conditions. The model is used to predict the timing degradation in digital circuits under arbitrary input activities. An equivalent degradation level is found that can be applied to all p-FETs in the circuit and can serve as an upper bound of degradation due to arbitrary input activity and avoid the conservative worst case dc analysis. The activity dependence is studied in microprocessors as well as arithmetic circuits under different actual workloads.**

***Index Terms*— Arbitrary input activity, compact model, digital circuits, frequency degradation, negative bias temperature instability (NBTI).**

I. Introduction

NEGATIVE bias temperature instability (NBTI) continues to remain as a serious reliability concern in high-K metal gate p-FinFETs [1]–[5]. NBTI is due to the buildup of positive gate insulator charges, which shifts parameters such as threshold voltage (ΔV_T), transconductance (Δg_m), and drain current (ΔI_D) with time [6], and affects circuit performance [7]–[15]. It results in higher timing delay ($\Delta \tau$) in digital blocks, which leads to an increase in combinational path delay [7]–[11]. As the clock frequency (f) is determined by the largest combinational path ($\sim$ critical path) delay between the flip-flops, delay degradation in critical path can lead to circuit failure because of timing violations [11], [16]. Hence, timing guard bands at design time have to be accurately estimated for accommodating the frequency degradation (Δf) due to NBTI-induced ΔV_T during runtime to ensure circuit reliability over its desired lifetime [15], [17]. Usually, V_T of all p-FETs is shifted by the worst case (dc) value to estimate $\Delta \tau$ related to NBTI in a circuit. However, since digital circuits operate under ac pulse, and ac NBTI is lower than dc due to recovery [3], it is necessary to develop an ac-activity aware framework to estimate circuit degradation under actual operating workloads.

In this paper, it is shown that ΔV_T under arbitrary ac stress patterns having multiple cycles cannot be predicted by using a single cycle of stress and recovery with effective stress ON/OFF time. The fixed-time compact model (FTCM) framework is proposed and used to calculate ΔV_T of all the p-FETs present in a circuit under arbitrary stress patterns. The resulting $\Delta \tau$ is benchmarked to that due to ΔV_T obtained from full cycle-by-cycle simulation by using the bias temperature instability analysis tool (BAT) [18]. Different combinational standard cells [19] and cascaded circuit chains are analyzed, and $\Delta \tau$ for different combinations of input signal slews and fan-out loads is estimated. An equivalent ΔV_{TEQ} that can be applied to all p-FETs in a multistage circuit and can serve as an upper bound of $\Delta \tau$ caused by different arbitrary stress patterns is estimated. Aging-induced delay in complex designs such as microprocessors and large arithmetic circuits under the impact of different workloads is estimated using the standard cell libraries that are precharacterized under NBTI. Estimated $\Delta \tau$ assuming ΔV_{TEQ} assignment to all p-FinFETs is compared with $\Delta \tau$ due to different workloads, and the advantage of using ΔV_{TEQ} in all p-FETs over ΔV_{TDC} in all p-FETs is discussed.

II. Device to Circuit Framework

The BAT framework is used to estimate ΔV_T of a transistor due to NBTI stress [18]. An arbitrary stress pattern is applied as an input to BAT, and the end of stress ΔV_T is estimated by full cycle-by-cycle transient simulation, this is denoted as BAT in Figs. 2–5. ΔV_T obtained by BAT and FTCM are

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A. Thirunavukkarasu, J. Joe, N. Parihar, S. Mishra, and S. Mahapatra are with the Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India (e-mail:vickythirunavukkarasu@gmail.com; jerinagnes@gmail.com; np.electro@gmail.com; subrat.mishra90@gmail.com; souvik@ee.iitb.ac.in).

H. Amrouch and J. Henkel are with the Institute of Computer Engineering, Karlsruhe Institute of Technology, 76131 Karlsruhe, Germany (e-mail: amrouch@kit.edu; henkel@kit.edu).

N. Goel is with the Department of Electrical and Electronics Engineering, BITS Pilani Dubai Campus, Dubai 345055, UAE (e-mail: goel.nilesh@gmail.com).

C. K. Dabhi and Y. S. Chauhan are with the Department of Electrical Engineering, IIT Kanpur, Kanpur 208016, India (e-mail: chetan.dabhi2013@gmail.com; chauhan@iitk.ac.in).

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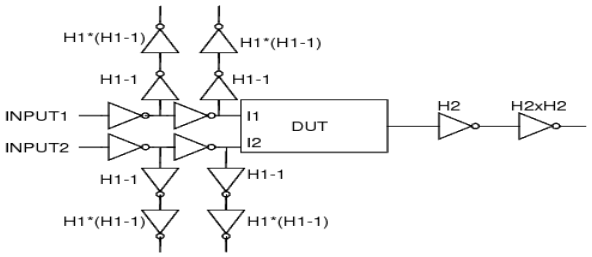

Fig. 1. Test structure for measuring delay of DUT for different slew and fan-out load conditions. The fan out of the DUT can be varied by varying H2, and input slew can be varied by varying H1.

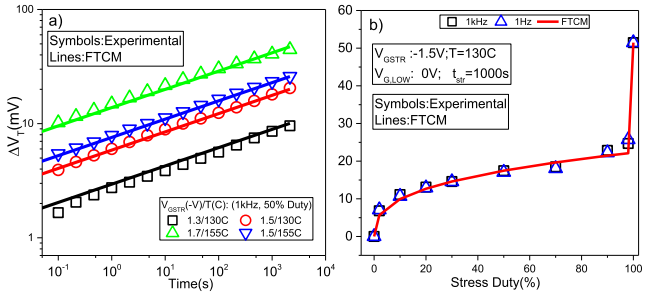

Fig. 2. FTCM prediction of ultrafast measured ΔV_T for ac stress (a) at different V_{GSTR}/T (b) at different frequencies as function of duty cycle.

used in SPICE framework for the calculation of rise delay degradation ($\Delta\tau_R$) in inverters.

In combinational standard cells and cascaded circuit chains with multiple p-FETs, the stress patterns input to a particular p-FET may not necessarily be the stress experienced by all p-FETs. The stress pattern for a p-FET can be different from the ac input pattern, and it depends on the structural connection of FETs in the circuit (stacked in parallel or in series) [8]–[11], [16], [17]. Note that NBTI for p-FETs connected in parallel configuration depends only on its gate input pattern. However, for p-FET in a stacked series configuration, NBTI depends not only on its gate input but also on the condition of all p-FETs in series under stress [8], [9], [17]. Arbitrary digital ac pattern (1 or 0) having effective pulse duty cycle (PDC) of $d_i \in \{10, 30, 50, 70, 90\}$ is given at each of primary inputs of the circuit, and the pattern (1 or 0) at each node in the circuit is estimated by using the pull up and pull down logic of the network. The ac stress pattern seen by each p-FET in the circuit is evaluated based on the location of the FET in the circuit (parallel or series) and its corresponding gate node stress pattern. BAT and FTCM estimate ΔV_T of the transistor based on the input stress pattern at the gate node. This procedure is used to determine ΔV_T of each FET in the circuit and obtained ΔV_T is input into SPICE to determine $\Delta\tau$.

Fig. 1 shows the test structure [20] used for measuring NBTI-induced circuit delay by using SPICE; the circuit under test is denoted as "device under test (DUT)." The propagation delay from the input to the output of the DUT is measured. The delay is determined for different input signal slew and fan-out load conditions, by varying the number of inverters connected to the input (H1) and the output (H2) of the DUT. Berkeley short-channel insulated-gate-FET model common multi gate (BSIM-CMG) [21]-based model cards for 14-nm FinFETs are extracted for fresh n-FETs and p-FETs and for p-FETs under NBTI [22] and used for SPICE analysis in different circuits. All analysis used calibrated BSIM-CMG modelcards with 14-nm FinFET node [23] (see [22] for details). ΔV_T of 50 mV is used for dc, and the universal duty cycle dependence is used to determine ΔV_T for ac stress [14] using the FTCM framework as described in the following.

III. FTCM Framework and Validation

As explained in [18], overall ΔV_T during dc NBTI stress is due to uncorrelated contributions from the generated interface (ΔV_{IT}) and bulk (ΔV_{OT}) traps as well as hole trapping (ΔV_{HT}) in preexisting traps. Note that ΔV_{OT} is not significant unless very high-stress bias (V_{GSTR}) and temperature (T) are used, and ΔV_{HT} is negligible for digital ac stress. Hence, ΔV_T for ac stress (under moderate V_{GSTR}/T) is due to ΔV_{IT}, which is given by FTCM as follows:

$$\Delta V_T(t) = A V_{GSTR}{}^{\Gamma} e^{-\frac{E_a}{kT}} t_{STR}^{n} \mathrm{PDC}^{\alpha} \quad (1)$$

where A is a device-specific constant, V_{GSTR} is the dc stress bias, T is the stress temperature t_{STR} is the total stress time, PDC is the stress duty of arbitrary random pattern and defined as the ratio of on time to total time, Γ (=4.5) is the power-law voltage acceleration factor (VAF), E_A (=0.1 eV) is the Arrhenius T activation energy, n(= 0.16) is the power-law time exponent, and α (=0.35) is the power-law duty exponent. ΔV_T for dc stress is given in (1), plus a constant term that depends on electron capture (in generated interface traps) during pulse-OFF phase (ΔV_{EC}) and ΔV_{HT} (see [18] for details).

Fig. 2(a) and (b) shows the FTCM prediction of measured ΔV_T time kinetics at different V_{GSTR} and T and ΔV_T at the fixed time at fixed V_{GSTR} and T as a function of duty cycle, for mode-B ac stress in a single p-FET (data from [18]). Note that FTCM can predict measured data well for various conditions.

Fig. 3(a) shows an example of arbitrary input stress pattern applied to the gate of a single p-FET, and Fig. 3(b) shows the corresponding BAT and FTCM simulations. Note that BAT is well calibrated with the experimental data in [18], and hence, the cycle-by-cycle simulation is a close representation of the experimental data. Similar analysis has been done for different random patterns, and the resultant ΔV_T at the end of ac stress segment from BAT and FTCM is plotted versus duty cycle in Fig. 3(c) and (d) for various V_{GSTR} and T. FTCM can predict BAT data under various random experimental conditions. From Fig. 3(b), note that the prevalent approach used for calculating ΔV_T by effective single-cycle stress-recovery simulation with effective ON- and OFF-time of arbitrary stress pattern [denoted as BAT effective duty (BAT-ED) in Fig. 3(b)] underestimates the end of stress ΔV_T obtained by using cycle-by-cycle BAT simulations. The exact reason behind the failure of this approach needs to be explored in detail and is beyond the scope of this paper.

Note that for a given device level ΔV_T, the overall $\Delta\tau$ in a circuit would depend on its architecture (i.e., pull up and pull down nets), as well as on input signal slew and fan-out load [13], [17]. Hence, it is necessary to validate FTCM

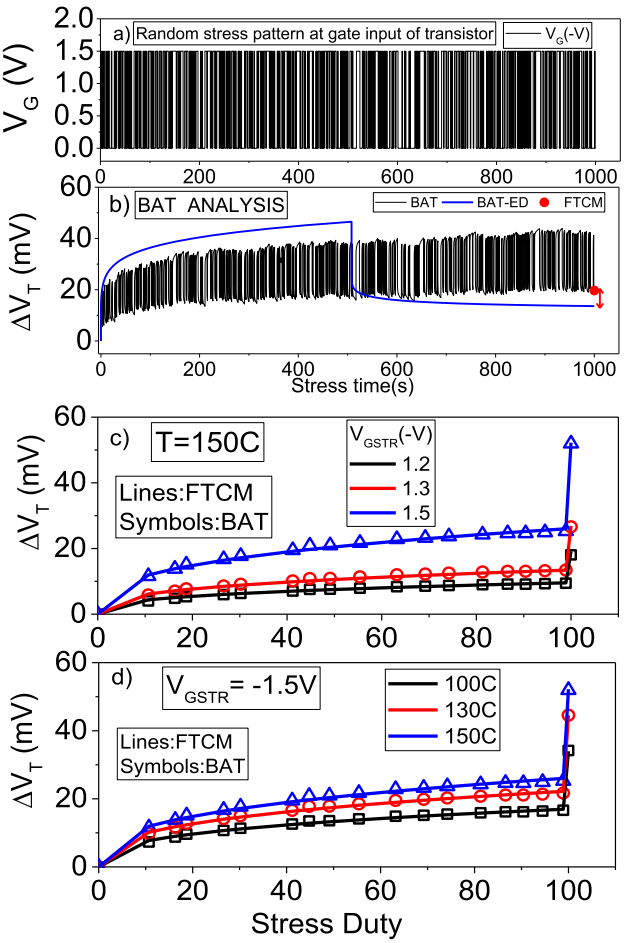

Fig. 3. (a) Arbitrary random pattern given as stress input to BAT. (b) Prediction of ΔV_T by full cycle-by-cycle simulation (BAT), effective single-cycle simulation (BAT-ED), and FTCM indicating BAT-ED is under predicting degradation and FTCM predicts ΔV_T. BAT and FTCM prediction of ΔV_T for arbitrary stress pattern as a function of duty cycle (c) for different stress high voltages (V_{GSTR}) and (d) for different temperature (T).

predictions against actual cycle-by-cycle BAT analysis at the circuit level for different circuit structures, input signal slew, and fan-out load conditions. This is done using an inverter and various digital gates as the DUT in Fig. 1. ΔV_T obtained from BAT and FTCM due to arbitrary random input pattern are fed into SPICE, and $\Delta\tau_R$ for an inverter due to ΔV_T of p-FET from the above-mentioned models is obtained. Fig. 4 shows the comparison of $\Delta\tau_R$ for ΔV_T obtained from BAT and FTCM. Once again, FTCM is able to predict the end of stress segment $\Delta\tau_R$ obtained by cycle-by-cycle BAT simulation.

FTCM is also compared against BAT at the circuit level for different input slew and fan-out load conditions, using circuits with different structural arrangement of transistors, multistage circuits, and cascaded circuit chains. Fig. 5 shows the comparison of $\Delta\tau_R$ for the NAND and NOR gates when ΔV_T in transistors is obtained using BAT and FTCM, the methodology is discussed earlier in Section II. $\Delta\tau_R/\tau_R$ as predicted by FTCM is within $\pm 0.4\%$ for NAND and $\pm 0.6\%$ for NOR when compared to that using BAT for different fan-out load conditions (not shown here for brevity).

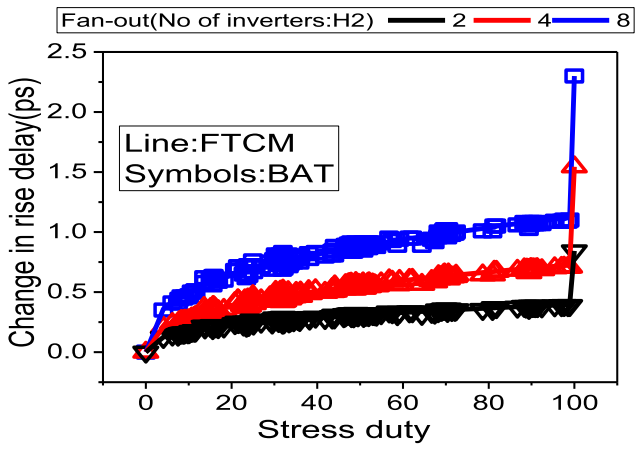

Fig. 4. Comparison of change in rise delay ($\Delta\tau_R$) of inverter for different fan-out load of inverters due to ΔV_T (because of arbitrary input stress pattern) predicted by BAT and FTCM.

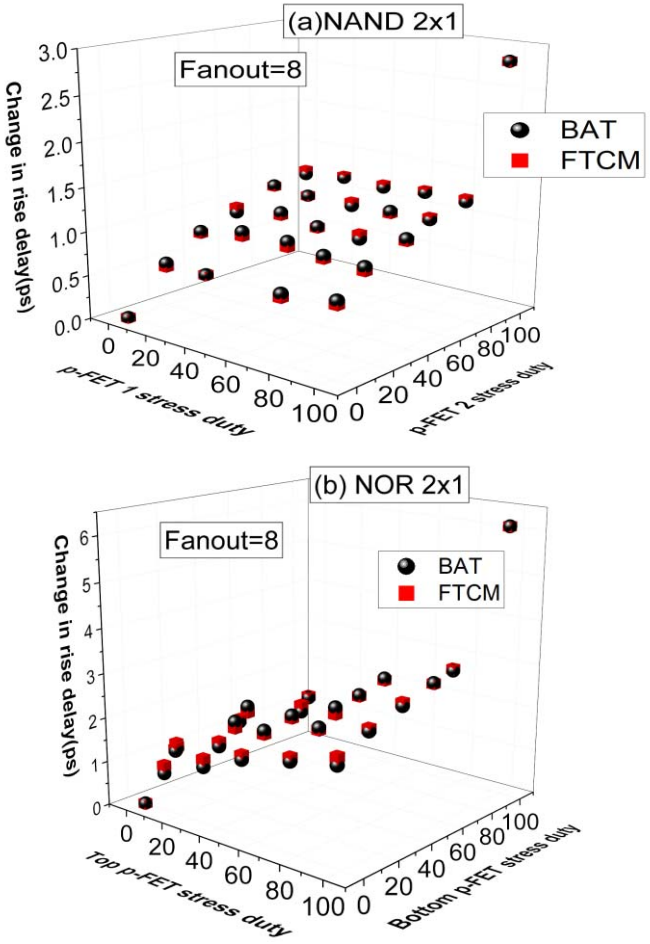

Fig. 5. BAT and FTCM prediction of change in rise delay ($\Delta\tau_R$) due to arbitrary input pattern at primary inputs for (a) nand and (b) nor (for fan-out load of eight inverters).

For multistage standard cells (AND, OR, 2 × 1 MUX, and full adder, refer to [19] for description), the degradation in average delay ($\Delta\tau_{AVG}$) is considered, as p-FETs can be present in both the rise path and fall path from input to output. Fig. 6 shows the schematics of the circuits analyzed, and Fig. 7

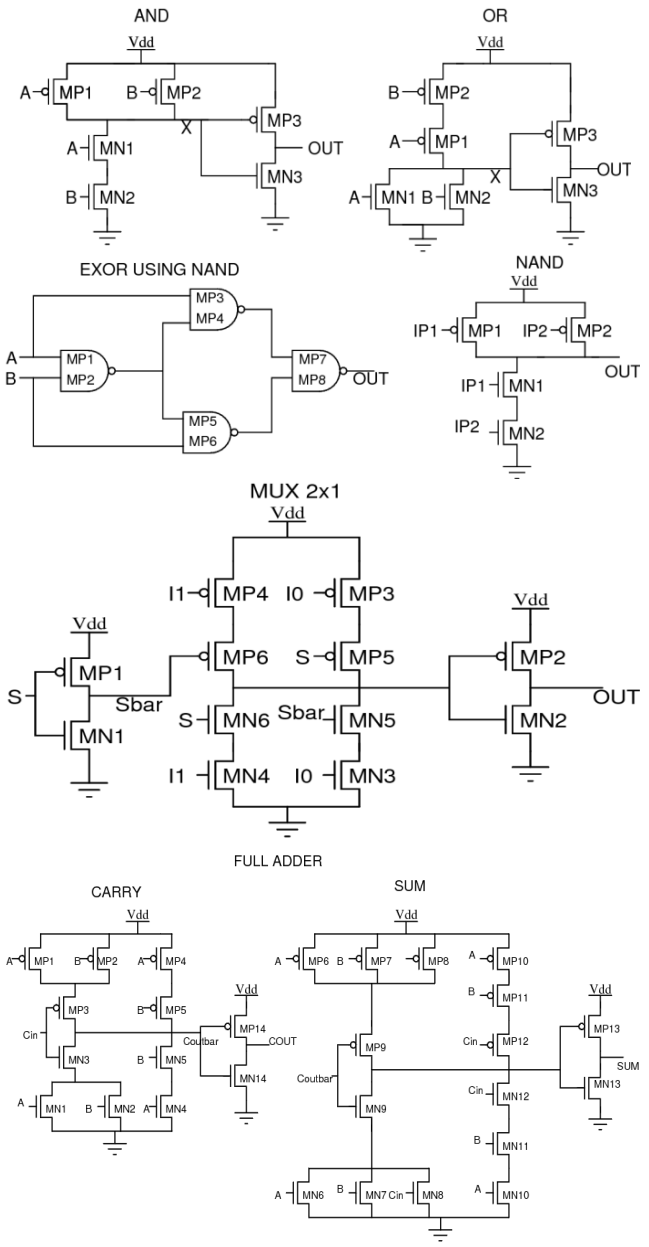

Fig. 6. Schematics of circuits from [19]. (a) and (two input). (b) or (two input). (c) exor using nand. (d) 2 × 1 MUX. (e) full adder carry. (f) full adder sum.

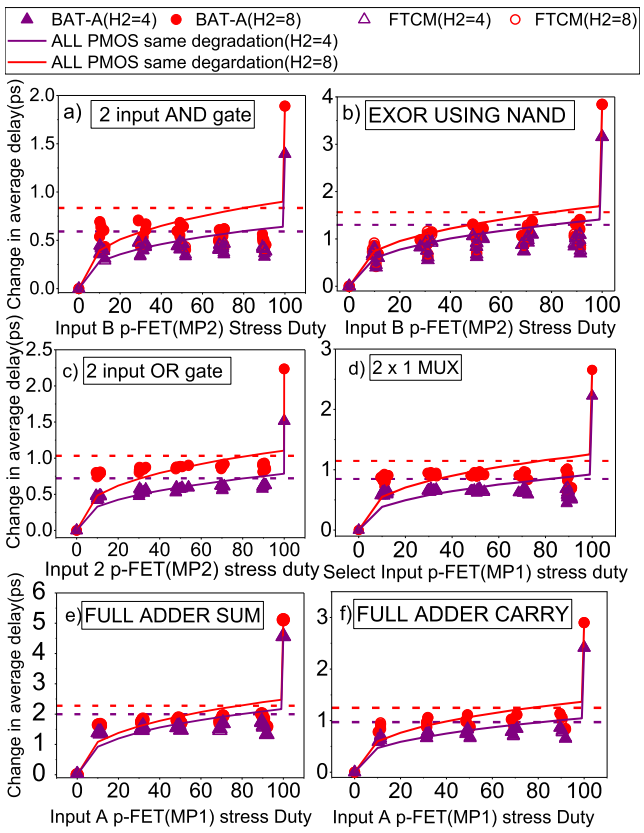

Fig. 7. BAT and FTCM prediction of change in average delay ($\Delta\tau_{AVG}$) due to arbitrary input pattern at primary inputs for (a) and(2 × 1), (b) exor using nand (2 × 1), (c) or (2 × 1), (d) 2 × 1 MUX, (e) full adder sum, and (f) full adder carry [note: lines indicate case of degrading all p-FETs by the same ΔV_T. Degrading all p-FETs by ΔV_T corresponding to 80% duty serves as upper bound of all the random cases (indicated by dashed line)].

shows the comparison of $\Delta\tau_{AVG}$ obtained using BAT and FTCM for different multistage standard cells such as two-input AND, two-input OR, 2 × 1 MUX, full adder (sum and carry), and cascaded circuit chain (EXOR using NAND) for different fan-out load conditions. The delay degradation increases with increase in fan-out load. Note that the difference in $\Delta\tau_{AVG}$ obtained using BAT and FTCM diminishes for multistage standard cells and circuits (not shown here for brevity).

IV. Equivalent Stress Duty Calculation

It is extremely difficult and computationally intensive to estimate ΔV_T of each transistor in complex circuits such as microprocessors as it may involve thousands of combinational and sequential logic gates and millions of transistors. Hence, it is necessary to predict an equivalent ΔV_T (denoted as ΔV_{TEQ}), which can be used as degradation parametric for all transistors (irrespective of its activity and actual ΔV_T) to evaluate timing degradation in sophisticated circuits due to aging. ΔV_{TEQ} should be decided such that $\Delta\tau_{AVG}$ due to the same ΔV_{TEQ} for all p-FETs should be greater than the maximum $\Delta\tau_{AVG}$ due to all the arbitrary cases of different ΔV_T produced for every p-FET due to actual arbitrary ac stress pattern that each of the FETs experiences. Normally, the state of the art [17] considers applying dc degradation to all p-FETs to determine the worst case NBTI-induced delay increase in circuits. Such estimation represents a theoretical upper bound that is very conservative. As a result, timing guard bands that are larger than required would be included leading to considerable efficiency losses at runtime. It is known that ΔV_T of a FET is dependent on stress duty under ac operation. Hence, stress duty experienced by transistors in some multistage basic combinational standard cells is analyzed to decide on the equivalent stress duty (d_{EQ}), which can be used to find ΔV_{TEQ}.

For AND (four input) shown in Fig. 8(a), the transistor MP5 is stressed only when its gate input node X is 0, which only happens when all of MP1, MP2, MP3, and MP4 have gate input of 1 (i.e., NBTI unstressed). If any of

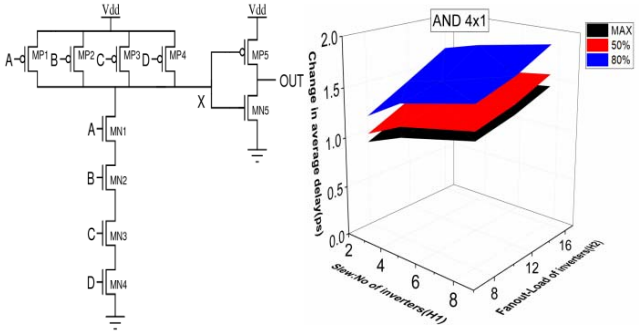

Fig. 8. (a) and(four input) circuit. (b) Comparison of maximum change in average delay ($\Delta\tau_{\text{AVG-MAX}}$) due to all arbitrary input pattern cases, change in average delay($\Delta\tau_{\text{AVG,50\%}}$) due to d_{EQ} of 50%, and change in average delay ($\Delta\tau_{\text{AVG,80\%}}$) due to d_{EQ} of 80% for different slew and fan-out loads.

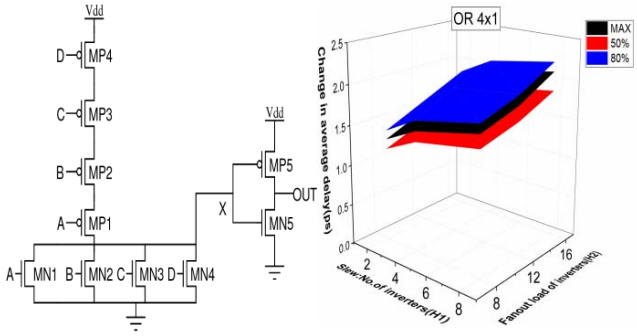

Fig. 9. (a) or(four input) circuit. (b) Comparison of maximum change in average delay ($\Delta\tau_{\text{AVG-MAX}}$) due to all arbitrary input pattern cases, change in average delay($\Delta\tau_{\text{AVG,50\%}}$) due to d_{EQ} of 50%, and change in average delay ($\Delta\tau_{\text{AVG,80\%}}$) due to d_{EQ} of 80% for different slew and fan-out loads.

MP1 through MP4 is ON (NBTI stressed), node X would be 1, and hence, MP5 would be unstressed. Hence, the maximum stress duty of MP5 would be 1—maximum (stress duty of MP1 through MP4). This states that for the arbitrary pattern at the primary inputs in a multistage circuit if the first stage is more stressed, the next stage would be less stressed, and the subsequent stage would be stressed more and so on. Hence, equivalent stress duty (d_{EQ}) that would serve as an upper bound of delay degradation due to arbitrary input pattern for a given circuit can be estimated. Arbitrary digital input pattern with effective PDC of $d_i \in \{10, 30, 50, 70, 90\}$ is applied at each of the primary inputs. There are four inputs, and hence, 5^4 different cases of arbitrary ac input patterns are applied and FTCM is used for finding ΔV_{T} for every transistor, and delay degradation is estimated for different input slew and load conditions. The maximum change in delay of 5^4 cases is referred as $\Delta\tau_{\text{AVG-MAX}}$. An equivalent stress duty is determined and ΔV_{T} corresponding to this d_{EQ} is obtained from FTCM, and all p-FETs in the multistage circuit are degraded by the same ΔV_{TEQ} corresponding to d_{EQ} and the delay degradation is reestimated. Fig. 8(b) shows $\Delta\tau_{\text{AVG-MAX}}$ versus input signal slew and output load capacitance for arbitrary stress, and compare it with equivalent stress duty (all p-FETs under identical ΔV_{TEQ}) simulation. An equivalent duty of 0.5 serves as the upper bound of $\Delta\tau_{\text{AVG-MAX}}$ produced due to different arbitrary input cases for different input slew and load conditions for this circuit.

For OR (four input) shown in Fig. 9(a), MP1 through MP4 is stacked in series, and MP5 is unstressed only when all of MP1 through MP4 are stressed. MP1 is stressed only when its gate input is zero, and all p-FETs (MP2, MP3, and MP4) above it are also stressed. Stress at MP1 indicates MP5 is unstressed. Therefore, the stress duty of MP5 would be 1 (stress duty of MP1), and the maximum stress duty of MP1 equals minimum stress duty among MP1, MP2, MP3, and MP4. The maximum stress duty of MP2 equals minimum stress duty among MP2, MP3, and MP4. Once again, 5^4 different arbitrary ac input patterns are applied and FTCM is used for finding ΔV_{T} for every transistor, and $\Delta\tau$ is estimated for different input slew and load conditions. Fig. 9(b) shows $\Delta\tau_{\text{AVG-MAX}}$ versus input signal slew and output load capacitance for arbitrary stress and compares it with equivalent duty simulation. Note that the equivalent duty of $d_{\text{EQ}} = 0.8$ (and NOT $d_{\text{EQ}} = 0.5$) serves as upper bound for $\Delta\tau_{\text{AVG-MAX}}$ for this circuit. This is because or gates with series connected p-FETs are expected to degrade more as compared to and gates with parallel input p-FETs.

Several combinational multistage standard cells from open-source 15-nm FinFET library [19] and cascaded circuit chains are analyzed similarly. For m-input DUT, 5^m different cases of arbitrary ac input pattern are applied, and $\Delta\tau_{\text{AVG-MAX}}$ is noted for different input signal slew and fan-out loads. Fig. 10 shows obtained $\Delta\tau_{\text{AVG-MAX}}$ from the above-mentioned exercise, and compare it to $\Delta\tau$ from equivalent stress duty of 0.5 and 0.8 for different fan-out loads and input signal slew. The degradation is higher for larger input signal slew and output load, while d_{EQ} of 0.8 can serve as the upper bound of delay degradation due to arbitrary ac input patterns at the primary inputs for different multistage combinational standard cells as four input AND, four input OR, 2×1 MUX, two-input XNOR, and half and full adder, and also in cascaded circuit chains such as two-input EXOR (using two-input NAND), two-input EXOR (using two-input NOR), and c17 benchmarks [24] (using five-input and two-output circuits consisting of cascaded chain of two-input NAND gates). It is observed that $d_{\text{EQ}} = 0.8$ holds because of averaging effect of degradation due to stress and no stress at alternate stages in multistage cells or cascaded circuit chain. Therefore, the timing degradation due to arbitrary input activities in combinational circuits can be predicted by the ED approach. This would benefit the analysis of very large circuits as discussed in the following.

V. Analysis of Complex Circuits

A. Analysis Methodology Under Actual Workloads

Aging-induced timing degradation in complex designs such as microprocessors and large arithmetic circuits as illustrated in Table I is determined when the impact of activities caused by running workloads on top of circuits is taken into account. This is then compared to the equivalent duty or worst case dc cases when all FETs in the circuit are degraded by the same amount.

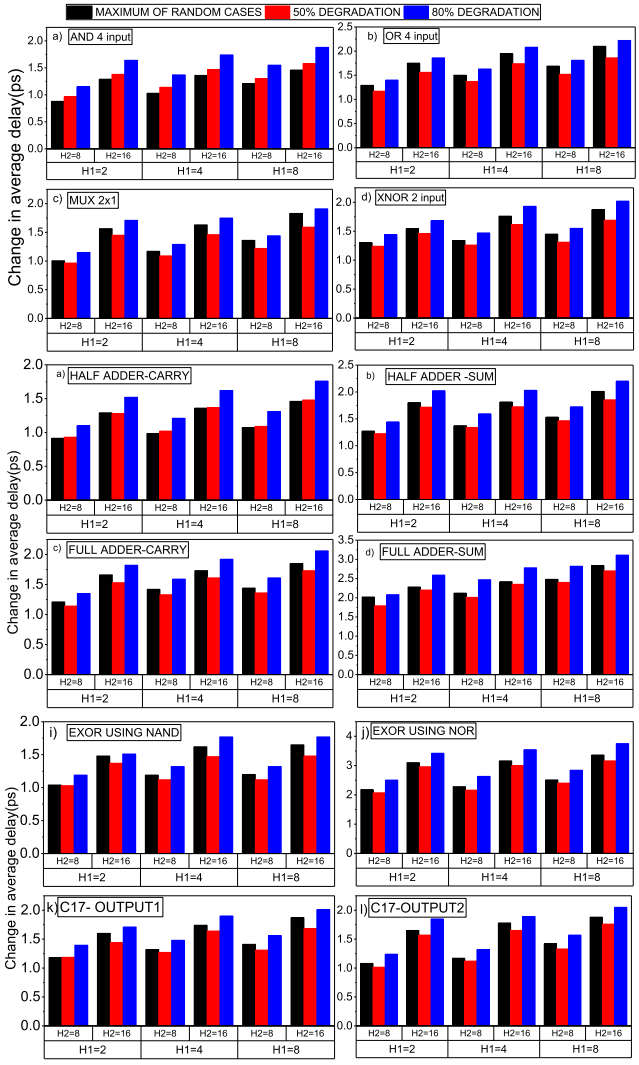

Fig. 10. Comparison of maximum change in average delay ($\Delta\tau_{AVG\text{-}MAX}$) due to all arbitrary input pattern cases, change in average delay($\Delta\tau_{AVG,50\%}$) due to d_{EQ} of 50%, and change in average delay ($\Delta\tau_{AVG,80\%}$) due to d_{EQ} of 80% for different slew and fan-out loads for multistage standard cells such as (a) four input and, (b) four input or, (c) MUX (2 × 1), (d) two-input xnor, (e) half adder carry, (f) half adder sum, (g) full adder carry, (h) full adder sum, (i) exor using nand, (j) exor using nor, (k) C17 output 1, and (l) C17 output 2.

The workload dependence is analyzed as follows. Standard cells [19] are characterized using calibrated time-zero FinFET modelcard (refer [22] for details) using [25], and subsequently, the register transfer level for different circuits is synthesized [26]. The output of this step is gate-level netlist and detailed delay information of all cells within the netlist. Gate-level simulations using [27] are done next when representative workloads are executed on top of the circuit's netlist. Standard applications/benchmarks are executed for microprocessor, while the arithmetic circuits are simulated under 100-K random input data to represent the wide range of activities that can be caused by varied workloads in reality. The switching activity and, hence, the signal probability of input–output of every cell in the circuit netlist are noted, and the duty cycle of every p-FET in each cell is averaged within a granularity of 10 (the duty cycle range is from 0 to 100 with a step of 10). This average value is assigned to every p-FET in a given cell inside the netlist for a particular workload.

TABLE I
COMPLEXITY OF DIFFERENT ARITHMETIC CIRCUITS AND IWLS BENCHMARKS

Circuit	Number of gates	Critical path depth
PULP-Processor	27630	39
Bar	1748	12
Adder	1846	10
Max	2730	73
Square	13685	28
Multiplier	25264	28
ac_97	11855	12
aes	20795	15
des	98341	11
spi	3227	13
usb_funct	12808	8
s13207	1219	8
s15850	685	10
s35932	7273	6
s38417	8278	21
s38584	6724	16
fpu	78,589	219

A total of 11 p-FET modelcards are created where V_T of the transistor is determined as per input duty cycle of the gate, with 0 being prestress and 100 being dc stressed. Standard cells are recharacterized using aged modelcards (for different duty). Note that all cells in the standard cell library are always (prestress and poststress) characterized using seven input signal slew × seven output load capacitance matrix.

The static timing analysis (using [28]) of the circuit's netlist is done at time-zero and under actual workloads; the activity-dependent cell libraries are used for the workload dependence. This analysis provides the maximum delay of a circuit's netlist based on delay information in the generated cell library. The timing guard band is determined by comparing the circuit's delay at time-zero with delay obtained when modified libraries are used. Furthermore, aged cell libraries where all p-FETs are assigned a fixed V_T shift corresponding to a fixed ac duty or dc are also used. Different large circuits are analyzed to cover different circuit design complexities as shown hereinafter.

B. Analysis of Benchmark Applications and Circuits

The open-source 32-bit PULP processor based on state-of-the-art RISC-V instruction set architecture [29] is used under various real-life standard applications/benchmarks and is listed as follows: 1) sorting algorithm (Bubble Sort); 2) cyclic redundancy check (CRC32) for error detection in communication; 3) Fibonacci sequence algorithm; 4) tower of Hanoi algorithm; 5) matrix multiplication; and 6) motion detection for image processing. Fig. 11(a) shows that the delay increase due to aging for different actual workloads is always much below the worst case obtained by assigning ΔV_{TDC} to all p-FETs corresponding to dc stress at end of life. Such a conservative analysis would result in large overestimation of timing guard bands than what is actually needed. Moreover, it can be noticed

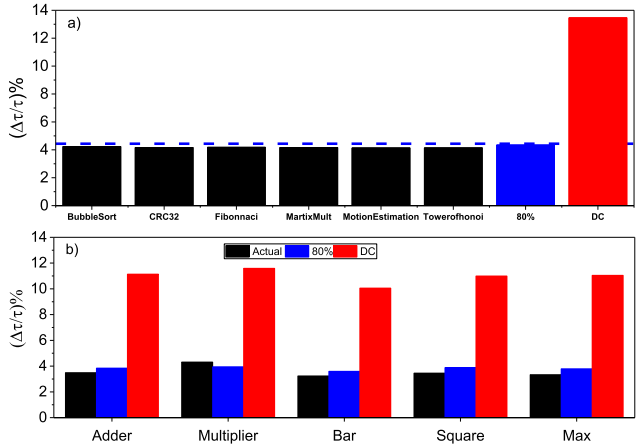

Fig. 11. (a) Delay degradation for different applications (workloads) running on top of processor (red dashed line: equivalent degradation duty d_{EQ} of 80%). (b) Comparison of actual delay degradation due to input pattern-dependent ΔV_T, delay degradation due to ΔV_{TEQ} corresponding to duty d_{EQ} of 80%, and delay degradation due to ΔV_{TDC} in different arithmetic circuits.

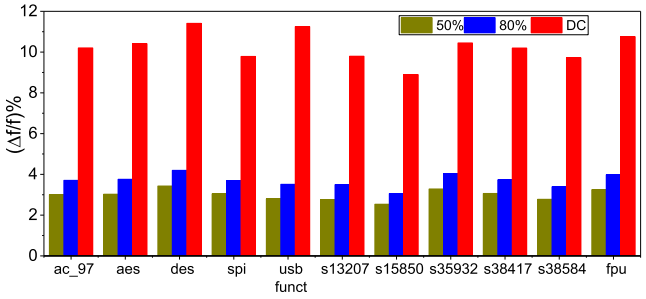

Fig. 12. Comparison of frequency degradation in different IWLS benchmarks due to ΔV_T (dc) degradation and ΔV_{TEQ} equivalent degradation corresponding to duty d_{EQ} of 80% and d_{EQ} of 50%.

that the aging-induced delay degradation in all applications is slightly below the aging case due to constant ΔV_{TEQ} for all p-FETs corresponding to the duty cycle of 80%. Therefore, a duty cycle of 80% in the analysis would enable the designers to estimate more realistic timing guard bands.

Furthermore, different complex arithmetic circuits obtained from state-of-the-art circuit benchmarks [30] are also used: 1) 128-bit multiplier; 2) 256-bit adder; (3) 135-bit barrel shifter; (4) 64-bit square; and (5) 512bit max. All circuits are analyzed under workload activities to obtain delay increase due to aging and compared to aging under a constant ΔV_{TDC} (dc worst case aging) and a constant ΔV_{TEQ} (under 80% duty cycle) that are assigned to all p-FETs. Fig. 11(b) shows that in all circuits, worst case aging leads to a significant overestimation of delay degradation compared to when workloads are considered, and the latter is very close to the case of assuming a constant duty cycle of 80% for all p-FETs in the circuit.

To estimate the extra margin in timing guard band that can be obtained with ΔV_{TEQ} corresponding to 80% duty compared to ΔV_{TDC} for worst case dc, the standard cells characterized with aged model cards (all p-FETs in the cell degraded by ΔV_T corresponding to duty of 50%, 80%, and worst case dc) are used to analyze different International Workshop on Logic and Synthesis (IWLS) benchmark circuits (also refer to Table I) [31] as follows: 1) WISHBONE ac 97 controller; 2) Advanced Encryption Standard Cipher; 3) Data Encryption Standard (performance optimized); 4) Serial Peripheral Interface IP; 5) Universal Serial Bus function core; 6) sequential ISCAS'89 benchmark circuits (s13207, s15850, s35392, s38417, and s38584); and 7) floating point unit. Fig. 12 shows that the frequency degrades by 3%–4% due to ΔV_{TEQ} of 80% rather than 9%–11% when ΔV_{TDC} is applied for different benchmarks that indicate the significant overestimation of timing guard band for worst case dc aging.

One of the cases (128-bit Multiplier) shows slightly higher degradation than the 80% value, while for all other cases, the degradation is lower than 80%. Therefore, an additional guard band can be used over 80% to be on the safer side, although the analysis shows that there is still a very large gap between dc and ac, even with a reasonable additional guard band.

VI. Conclusion

FTCM can be used to predict ΔV_T of every transistor in the circuits due to arbitrary digital ac pattern at primary inputs and timing degradation can be estimated using SPICE. FTCM is verified against BAT at the circuit level for different circuit structures, input signal slew, and fan-out load conditions. An equivalent degradation (ΔV_{TEQ}) for all FETs corresponding to equivalent stress duty (d_{EQ} of 80%) that can serve as an upper bound for the degradation due to arbitrary input activity is verified for various multistage standard cells, cascaded circuit chains, complex arithmetic circuits, and processors under actual workloads. The equivalent degradation of d_{EQ} around 80% can be used to find the maximum timing degradation due to activity-dependent NBTI aging in different arithmetic circuits and processors running different workloads, and estimate the timing guard band required to facilitate aging rather than using pessimistic ΔV_{TDC} for all p-FinFET. The saving in guard band due to this approach is also verified in different IWLS benchmarks.

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