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Exploration of Noise Impact on Integrated Bulk Current Sensors

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Abstract Current CMOS (Complementary Metal Oxide Semiconductor) technologies show an increasing susceptibility to a rising amount of failure sources. This includes also radiation induced soft errors, which requires countermeasures on several design levels. Hereby, BBICS (Bulk Built-In Current Sensors) represent a promising approach on circuit level. However, it is expected that these circuits, like similar sensors measuring substrate effects, are strongly susceptible to substrate noise. The intention of this work is an in-depth noise analysis of representative bulk sensors based on extracted layout data. Thereby, several aspects are considered, like sensor activation thresholds, impact of the distance to the noise source, and noise generation by test circuits. Results indicate that already noise RMS level of 5 to 9 % of the supply voltage can lead to false detections, which are values in the same order of magnitude of noise generated by test circuits.

Keywords Reliability · Noise · Substrate Extraction · CMOS · Bulk Sensors

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1 Introduction

The continuously downscaling of CMOS technologies leads to progress in nearly all areas of human society. It comes with a price, though. With the advancement of the technology nodes, new issues emerge which need to be overcome. This includes, for example, leakage currents due to short channel effects and tunneling. Another serious problem is gate oxide thickness, as its traditional small value is leading to higher susceptibility to breakdown and consequent system failure [33].

Further, radiation induced particles, which have been a problem solely for avionics and aerospace environment and memories, are a rising concern for ground level applications and combinational logic [11]. This trend is based on the decreasing critical charge levels and supply voltages of the integrated circuits in the current nanoscale era. The resulting transient faults can lead to soft errors or even system crashes. Amongst the several strategies to detect this kind of effects, Bulk Built-In Current Sensors represent a promising approach [23]. Their advantages are high sensitivity detecting radiation induced effects, fast response times and reasonable increase in area and power consumption in comparison to related approaches such as spatial redundancy or circuit hardening techniques [10, 16].

An additional challenge in integrated circuits is noise, which especially is critical in mixed-signal designs [29]. Due to diminishing voltage levels, increasing complexity, and steeper signals, though, also exclusive digital designs can be affected. Amongst the several noise sources, circuits with high switching activity, steep signal slopes, and high complexity have a dominant role and should lead to a noise analysis of the design [34].

There are several related works that explore and propose countermeasures to substrate coupling noise. However, to the best of our knowledge, there is no published research done on

noise analysis of integrated substrate sensors. Bronckers et al. present in [6] an optimal ground resistance value needed to minimize the substrate coupled noise generated by a transistor operating in a wide range of frequencies. In [25], the coupling of noise injected by digital circuits into the substrate is demonstrated to affect radio-frequency Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) due to variation of the threshold voltage, caused by the potential fluctuations in the substrate. These approaches target the noise influence in signals in the device, and, differently from this work, not in the substrate itself. Le et al. show in [13] that asynchronous implementations of originally synchronous digital circuits are able to reduce the injected noise and introduce system-level modifications as a prevention to noise generation. In [26], the authors propose a resistive-capacitive model for the drain of a MOSFET to substrate connection and obtain the model values from the Y parameters originated from the noise analysis. Apart from not aiming bulk-signal based devices, the substrate parameters are obtained from noise analysis, instead of being physically modeled. The authors of [35, 37, 38] explore strategies to reduce substrate noise in 3-D integrated circuits, introduced by through-silicon via (TSV) technology, characterizing degradation by noise prevention. Wolfel et al. demonstrated a method to reduce the influence of Flicker noise contribution on the readout of a Depleted p-channel field effect transistor (DEPFET) sensor [38]. Even though it explores a bulk-signal based device, the approach involves a novel measurement procedure, and not a fault detection system.

It is expected that sensors measuring substrate effects, like the mentioned BBICS, DEPFET sensors [37] or bulk pixel sensor [20], show a high susceptibility to noise. Consequently, the intention of this work is the exploration of the noise susceptibility of integrated nanoscale circuits for bulk current measurements.

The rest of the work is structured as follows. Section 2 gives preliminary information, while section 3 explores the noise generation. The following section 4 presents the executed experiments and discusses the results. Finally, section 5 concludes this paper.

2 Theoretical Background

2.1 Substrate Modeling

In order to analyze the effects of the substrate parasitic, an appropriate model is required. Such a model consists of interconnected electrical components, which values are obtained from its composition and geometry. The electrical components modeling can be achieved by techniques that suit in three different categories: numerical methods, analytical methods and empirical methods.

Analytic methods rely on approximate mathematical models based on electromagnetic laws. Although it involves the neglecting of various physical effects, such methods provide acceptable accuracy. Given that their implementations comprise intensive mathematical computation, they are not recommended for the extraction of layouts with large numbers of interconnects [31].

The empirical methods, in turn, make use of vast collections of experimental data, which are then fitted to a mathematical model. In the commercial scenario, many specific layout configurations take place, which would require different descriptive equations in a method other than the empirical. This is a reason for which it is extensively used in the industry. In contrast with that, the empirical technique involves computationally expensive functions such as logarithms and exponentials, which constitutes one drawback of this method.

Finally, there are the numerical methods, for example the FEM (Finite Element Method) approach, which is the chosen method in this work. Hereby, the substrate is discretized into cubes. The cube is translated into an electrical circuit composed by resistances and capacitances, as depicted in Fig. 1. Their values depend on the dimensions of the cuboid and the electrical characteristics of the material [29]. The reconstitution of the entire substrate is accomplished by interconnecting the appropriate nodes, obeying the spatial disposition of each element.

Finite Element Method provides a three dimensional modeling of the entire substrate. However, in order to obtain satisfactory modeling resolution, the computational time can easily reach impractical values. Consequently, a technique of fine discretization of heterogeneous areas (usually closer to the surface) and a coarser discretization of more homogeneous ones (deepest regions) are applied in order to reduce de computational cost [29].

Another approach is the Boundary Element Method (BEM), which implements a discretization of selected structures, for example contacts, well and substrate taps as well as diffusion regions [12]. Those structures are two dimensional, and thus, BEM provides a 2-D substrate model, comprising only regions of the substrate surface. Although BEM is

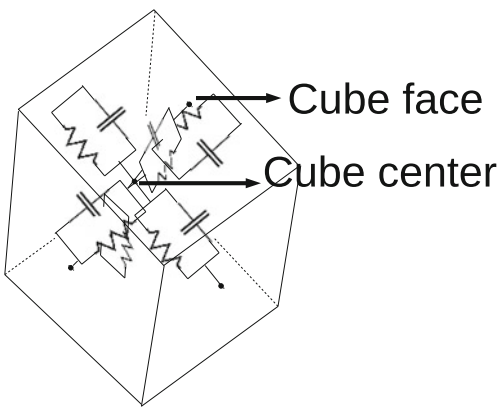

Fig. 1 Discrete element for substrate modeling

efficient in terms of computational effort, it cannot model deepest substrate characteristics [29].

2.2 Noise Modeling

An in-depth noise analysis requires the modeling of different kinds of noise. In VLSI (Very Large Scale of Integration) circuits, noise can be classified under two main categories: the intrinsic noise of the devices and the noise due to switching activity of the digital circuit [29]. In case of Device Noise one can find essentially three kinds of noise: Thermal Noise, Shot Noise and Flicker Noise [14].

Thermal noise, as the name states, occurs due to inherent crystalline structure agitation of the material, which causes charge carriers in the conduction band to move randomly. Its realization in time is modeled by the Normal Distribution, and since its Power Spectral Density (PSD) shows ideally the same power density for all frequency bands, it is so-called White noise. Hence, thermal noise is hereby modeled as White Gaussian Noise (WGN) [12].

In integrated circuits, shot noise refers to fluctuations in the current due to the discrete nature of charges. In contrast to thermal noise, shot noise is dependent upon the mean current flow in a semiconductor [14]. This kind of noise is also White Noise, although not necessarily Gaussian. Nevertheless, it can be modeled as such as [14], and thus, shot noise is modeled in this work as WGN, too.

Since both Thermal and Shot Noise are WGN, they can be represented by just one Normal Distribution realization, with following variance v_{WGN}:

$$v^2{}_{WGN} = v^2_{\text{thermal}} + v^2_{\text{shot}}$$

with $v_{thermal}$ meaning the variance of the "thermal noise", while v_{shot} represents the variance of the "shot noise". The mean of the applied noise, and thus of its components, is zero [34].

Flicker noise (also known as 1/f noise or pink noise) is a yet not fully understood phenomenon and a subject of much controversy [1]. One widely accepted explanation is based on trap-assisted recombination. This phenomenon is characterized by abnormalities in the silicon crystalline structure, responsible for the generation of intermediate energy levels in the bandgap. An electron eventually loses the amount of energy necessary to fall into the trap. Note that this energy loss is insufficient to make a transition to the valence level. Once the electron is in the trap, it is possible that it liberates energy again, ending up in the valence band and, thus, suffering recombination. The same observation concerning lower energy applies. Hence, the capturing and emission of carriers originated from this process result in fluctuation of the total number of mobile electron-hole pairs. Subsequently, this causes variation in electrical quantities such as current, voltage and electric fields [17].

One approach that can be used to model Flicker noise (in fact, any correlated type of noise) is to apply the WGN to a linear time invariant (LTI) system, more specifically, to a sequence of filters [22]. The output of the filter comprises the category of colored noise, since it no longer presents all frequencies with the same power density. Flicker noise is compounded by a specific spectral shape, as are other different types of colored noise, and that shape is what defines each. This kind of noise is known to be present in VLSI circuits and to have a PSD that decreases with increasing frequency. Given that Flicker Noise actuates stronger at low frequencies, one can conclude that its power spectrum constitutes the WGN power spectrum, which means WGN is a more general type of noise. Hence, a signal that behaves like Flicker noise can be filtered from WGN, which is the approach applied in this work.

Switching Noise results from logic transitions of digital signals. It can be transferred via interconnect coupling, which is outside the scope of this work, and via substrate coupling [7]. In case of the latter, the coupling occurs due to impact ionization, coupling from the reverse biased source-drain junction capacitances of the transistors during switching, and coupling from the supply network [5]. Contrary to Device Noise, Switching Noise is not strictly a random process, as it dependents on the switching activity of the digital circuit. However, it can be treated as random phenomenon due to the characteristics of integrated digital circuits [29, 30].

2.3 Soft Errors

As stated in the introduction, soft errors can cause system failure or logic errors. Those errors can be called SEUs (Single Event Upsets) or SETs (Single Event Transients), depending on their nature. Both are caused by energetic particles that strike the integrated circuits and form high levels of charge carrier generation through p-n junctions, which are then briefly short circuited [11].

SEUs are digital faults that change the signal state in memory elements such as flip-flops or latches, and consequently, affecting sequential logic. In contrast, SETs are perturbations that change a signal for a short time before it returns to its original state. If the effect of such perturbation reaches an enabled memory element it will cause incorrect behavior [23].

Such signal corruptions take place specifically in transistors at cut-off state. In the event of a particle incidence, an electron-hole pair track is formed through the particle's path. This affects the depletion region's electrical field configuration, which briefly adopts the shape of a funnel towards the substrate and starts the so-called carrier collection, which can be observed as a current on the affected node. The subsequent phase of carrier collection is defined by a slower phenomenon, in which carriers are conducted through the depletion region due to diffusion [32].

The mentioned effect is can be modeled by double exponential pulse I_{strike} as approximated by following equation [23]:

$$I_{\text{strike}}(t) = \frac{Q_{\text{coll}}}{t_f - t_r}\left(e^{\frac{-t}{t_f}} - e^{\frac{-t}{t_r}}\right) \quad (1)$$

Hereby, Q_{coll} indicates the total collected charge, t_r is the time constant for the funnel collection and t_f represents the second phase of carrier collection.

A common cause of soft errors in today's circuits is related to cosmic rays that react with the Earth's atmosphere and produce complex cascades of sub-particles [4]. At terrestrial altitudes, main components of the resulting isotropic flux are neutrons, whose reactions with silicon possess a linear energy transfer (LET) sufficient to cause upsets in the struck devices. It should be noted, that cosmic neutron flux is less prone to shielding, and thus, requires countermeasures on chip and/or device level.

2.4 Modular Bulk Built-In Current Sensors

Built-In Current Sensors (BICS) are an efficient mechanism to detect permanent faults and SEU in CMOS circuits during its quiescent state, that means when the circuit is not switching [36]. However, this method is not applicable for detection of SET, as the amplitude of transient currents induced by radiation can have the same order of currents normally generated by switching activities in combinational logic circuits [21]. As alternative have been proposed Bulk BICS, that measure the anomalous currents that flow through the junction between a bulk and a reversely biased drain of a disturbed transistor [23, 24]. Thus, these analog sensors enable the detection of radiation induced currents that might lead to SET and SEU in digital circuits. More information can be found in the related literature [3, 23, 39].

Amongst the several implementations, the modular BBICS (mBBICS) represents a promising trade-off between sensitivity, response time, robustness and area offset [32]. Further, its basic concept is similar to other BBICS. Hence, it was chosen as representative circuit.

The mBBICS is composed of two functional blocks: the head and the tail (see Fig. 2). The head circuits are connected to the bulk of the monitored transistors, while the tail circuit latches the output signal of several head circuits. In detail for the NMOS version of the mBBICS, the drain of transistor N_{h1} is connected to the bulk of the monitored transistors, its source is at GND, and its gate connected to V_{DD}. In normal operation, the drain of N_{h1} acts as a virtual GND while the drain of N_{h2} is at V_{DD} level. In the event of a strike, the fault current is conducted through N_{h1}. The consequent voltage drop increases the gate voltage of N_{h2}, which is switched on and pulls down the signal $head_{NMOS}$ that is connected to the drain of N_{h2} and the input of the tail circuit. The latter latches the input and

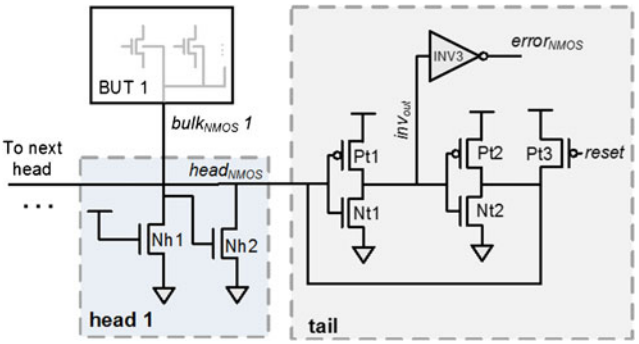

Fig. 2 Structure of a modular BBICS (NMOS version)

activates the error flag. The circuit remains in that state, until the reset transistor is activated, causing the circuit to go to initial state and be ready for another detection [32]. The PMOS version, which permits the detection of radiation effects in PMOS devices, possesses a complementary behavior. It is omitted for the sake of simplicity.

Further information regarding layout consideration, dimensioning, and amount of monitored devices can be found the related literature [32].

It should be noted that the processing of a detection of a radiation event occurs on higher processing layers and is not considered in this work. Further information can be found in [2, 15].

3 Noise and Fault Injection

3.1 Substrate Extraction and Probing Strategy

Careful layout design requires the application of a sufficient amount of taps that connect the substrate or doped well to a fixed voltage (e.g. GND or V_{DD}). However, since the substrate is not a perfect conductor, noise generated at the transistor bulks during the circuit operation could be conducted through the substrate network. Moreover, the inherent noise that is present in transistor bodies can traverse such a grid. Thus, the modeling of the circuit together with the substrate is mandatory for the analysis of the noise susceptibility of sensors measuring bulk effects.

In this work, the comercial tool Cadence QRC has been applied for the extraction of the substrate [27]. Thereby, technology dependent rules for substrate modeling are utilized during the layout extraction of the analyzed circuit. Consequently, two netlist are generated, one for the actual circuit and the other for the substrate. The resulting substrate netlist is connected to the circuit by tie devices. Hence, the extracted substrate network provides an access terminal for each layout tap or group of connected taps.

The analysis of the noise can be executed by placing an outtake tap in a region and extracting the substrate.

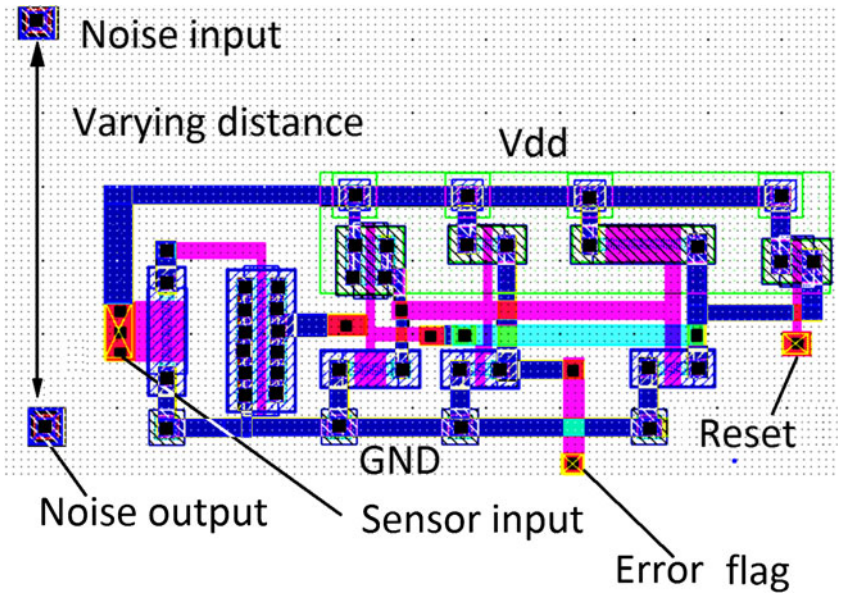

Fig. 3 Layout of the PMOS Modular Bulk-BICS, with indication of its terminals, the input, output, reset and power rail terminals. In the sensor activation analysis, noise is applied to the BBICS input

Thereby, the farther this tap is placed from the source circuit, the larger the area that composes the layout. As a consequence, the substrate equivalent circuit augments with more components and interconnections.

3.2 Noise Generation and Injection

Noise is constantly present in real electrical circuits and has to be considered by the designer [17]. The method for noise injection applied in this work utilizes a current or voltage source, depending on the situation, that is capable of introducing an arbitrary signal into the circuit. Thereby, the signal has been defined previously and stored in a file. It should be noted, that this methods enables the modeling of any noise generated by random sources. This includes inherent noise by the semiconductor devices, as in case of Shot, Thermal, and Flicker Noise, and noise due to switching activity.

Referring back to the theoretical background, the three common forms of Device Noise in VLSI circuits are thermal, Shot and Flicker noise [29]. Both thermal and shot noise can be modeled as WGN. In this work, WGN is generated by successive realizations of a Gaussian random variable and multiplying the resulting signal by a scaling factor. Flicker noise is obtained by filtering White noise by a low-pass.

In case of modeling of Switching Noise, WGN can be applied as well [30].

4 Simulation Results

4.1 Simulation Environment

In order to perform an in-depth analysis of the noise robustness of the mBBICS, it was necessary to design and extract the circuit layout. Therefore, the transistor level representation of

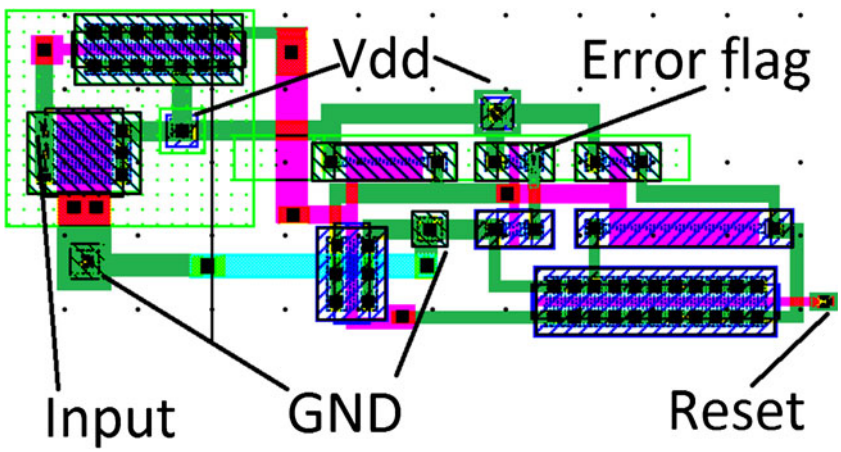

Fig. 4 Layout of the NMOS modular BBICS, with indication of the input, output, reset and power rail terminals. The substrate noise input and output taps, used in the distance analysis, are also indicated. In the sensor activation analysis, noise is applied to the BBICS input and the substrate noise taps are set to 0 V. In the distance analysis, the BBICS input is set to zero, and noise is applied to the substrate input and measured at the output tap

the sensor circuitry was implemented, including appropriate transistor sizing. Hereby, a predictive 90 nm process development kit with a V_{DD} of 1.2 V has been applied [28]. This was followed by the layout design (see Fig. 3 for the NMOS sensor and Fig. 4 for the PMOS one) and its extraction.

The results presented in this work are those obtained from the layout extracted netlists, including the substrate. A notably advantage of this method in comparison to solely schematic based analysis is the consideration of not only components, but also interconnects dimensions and physical constitution. In this case, the substrate as a network of undesired components is additionally included.

4.2 Exploration of Required Noise Level for Sensor Activation

The first analysis focused on the exploration of required noise levels that would lead to a false detection of a SET by the BBICS. Therefore, the levels of the RMS voltage V_{rms} of the noise on the bulk that lead to an activation of the sensors were determined for each combination of noise characteristics. This iterative procedure, consisting of applying noise at the sensor's input and verifying if an activation occurred, requires the definition of a desired tolerance or safety margin. Therefore, iterations were performed for every combination, with a stop criterion of 2 % tolerance. This criterion is based on the achievement of reasonable accuracy and limitations of the simulation procedure.

During this analysis, two noise waveforms were applied to stimulate the input of the sensor that is connected to the bulk of the monitored transistors. One noise was WGN, generated from the realization of a Normal distributed random variable with zero mean and variance equal to one, corresponding to thermal and shot noise. The second noise characteristic was the result of the WGN subjected to a low-pass filter, yielding the so-called Flicker Noise. Both waveforms were multiplied by an iteratively adjusted factor in order to adapt the Root Mean Square (RMS) value. The duration of each simulation was set to 10 μs.

It should be noted that this modeling considers noise caused by the device N_{h1} at the sensor's input, as well as Device Noise and Switching Noise generated by all devices connected to the substrate. Thus, maximum noise levels present in the substrate that affect the functionality of the BBICS can be determined.

Fig. 5 summarizes the results of this analysis for the NMOS and PMOS versions of the implemented modular Bulk-BICS. Hereby, W means WGN and F stands for Flicker noise. It should be noted that due to the intended generality of the analysis the dependency of Flicker noise on area has not been considered. Further, V and C indicate that the noise was applied to the circuit as voltage or current, respectively. Finally, N means the results for the NMOS sensor, whereas P indicates

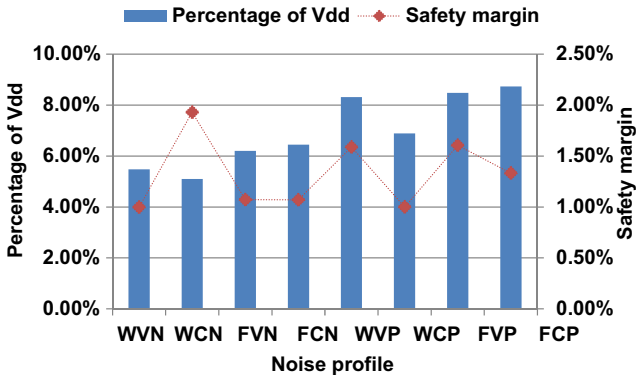

Fig. 5 Minimum noise RMS values for different noise profiles that lead to an activation of a BBICS. W stands for White noise, F for Flicker noise, V for voltage, C for current, N for NMOS BBICS and P for PMOS BBICS. The dotted graph indicates the difference between the activation values and the closest non-activation ones. Noise applied as current has its effect also represented as percentage of VDD, since the resulting voltage at the BBICS input is being measured

the PMOS one. As an example, FCP stands for Flicker noise being applied as a current signal to the PMOS sensor's input. Notice that noise applied as current has its effect also represented as percentage of a voltage (i.e., V_{DD}), since the resulting voltage at the BBICS input is being measured.

It can be concluded that the sensors are most susceptible to White noise, while Flicker noise applied as current requires the highest RMS values to activate the sensors. White noise induced as current to the NMOS BBICS is capable of flipping the error flag with a noise RMS value of 5.1 % of V_{DD}. In contrast, if applied to the PMOS sensor, an RMS value of 6.9 % of V_{DD} is required.

Further, it can be seen that the noise susceptibility of both types of BBICS is similar. For both sensors, White noise applied as current requires the minimum RMS value for activation, followed by White noise applied as voltage (5.5 % for NMOS sensor, 8.3 % for PMOS), Flicker noise induced as voltage (6.2 % for NMOS sensor, 8.5 % for PMOS) and Flicker noise applied as current (6.4 % for NMOS sensor,

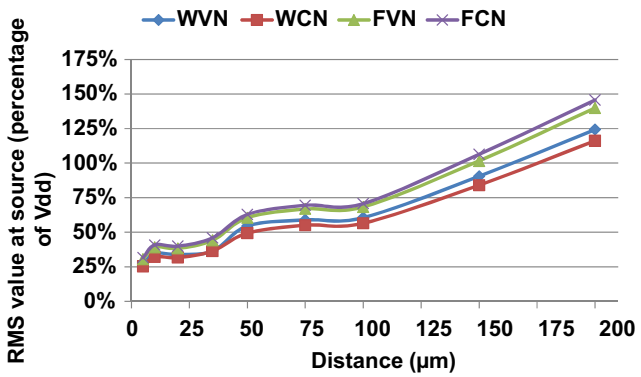

Fig. 6 Minimum noise RMS values that lead to an activation after propagation through the substrate (NMOS BBICS). The noise is applied and measured in different substrate taps, not connected to any circuit element

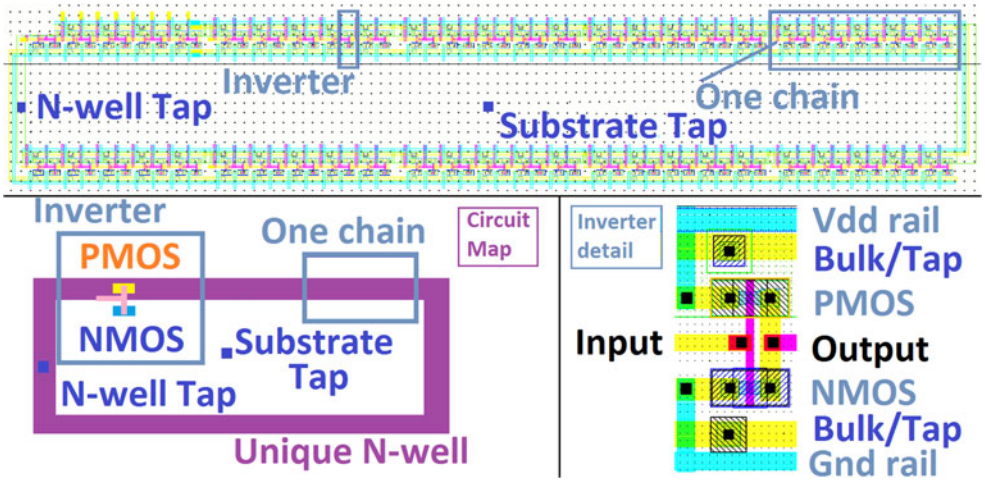

Fig. 7 Rectangular configuration of inverter chains with the measuring points indicated. A circuit map is provided for better understanding, given the size of the layout. The basic inverter is detailed

8.7 % for PMOS). However, the PMOS version of the sensor is more robust than its NMOS counterpart.

If Device Noise of a single transistor is considered, the determined limits are two orders of magnitude above the expected noise level, whose RMS level are reported to be up to several hundredth of mV for the applied technology node [9, 18]. Thus, considering Device Noise only the summation of the noise of several devices connected to the substrate might reach these noise limits.

On the other hand, noise due to Switching Activity has been reported to be in the same order of magnitude, and thus, cannot be ignored [8, 29].

4.3 Distance Analysis

In the next step, the behavior of conducted noise was analyzed for different locations of the noise source in the seen in Fig. 3 for the NMOS sensor, which is the target of this analysis. The distance between positions of input and output was changed from 5 to 200 μm. Like in the previous procedure, the RMS value of the noise was iteratively scaled with a safety margin of 2 %. Therefore, two substrate taps, one for the introduction of noise input and the other for its measurement, were added to the layout. The input and output taps can be.

As expected, the required noise RMS value that leads to activation rises with increasing distance due the noise attenuation by the substrate network (see Fig. 6). The results show a similar behavior for the four noise profiles. It can be observed that already for distances of 5 μm the required noise RMS level has to be at least 27.1 % of V_{DD} (WCN) in order to activate the sensor. This is more than 5 times higher than the required RMS value if the noise is applied directly, indicating an attenuation of 81.2 %. For a distance of 50 μm, the required RMS level for false sensor activation has to be higher than 50 % of V_{DD}. Finally, if the noise source is located farther than 175 μm, the noise RMS level has to be higher than 100 % of V_{DD}.

The size of the minimum inverter of the applied technology is ca. 1 μm^2 [28]. Hence, it can be concluded that noise

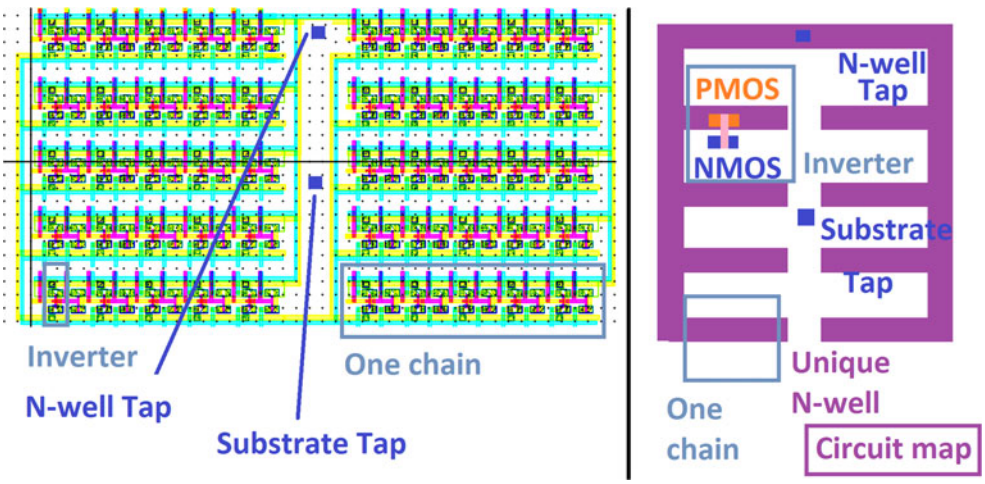

Fig. 8 Two groups of stacked inverter chains, with the measuring points (substrate and N-Well taps) indicated. A circuit map is provided for better understanding

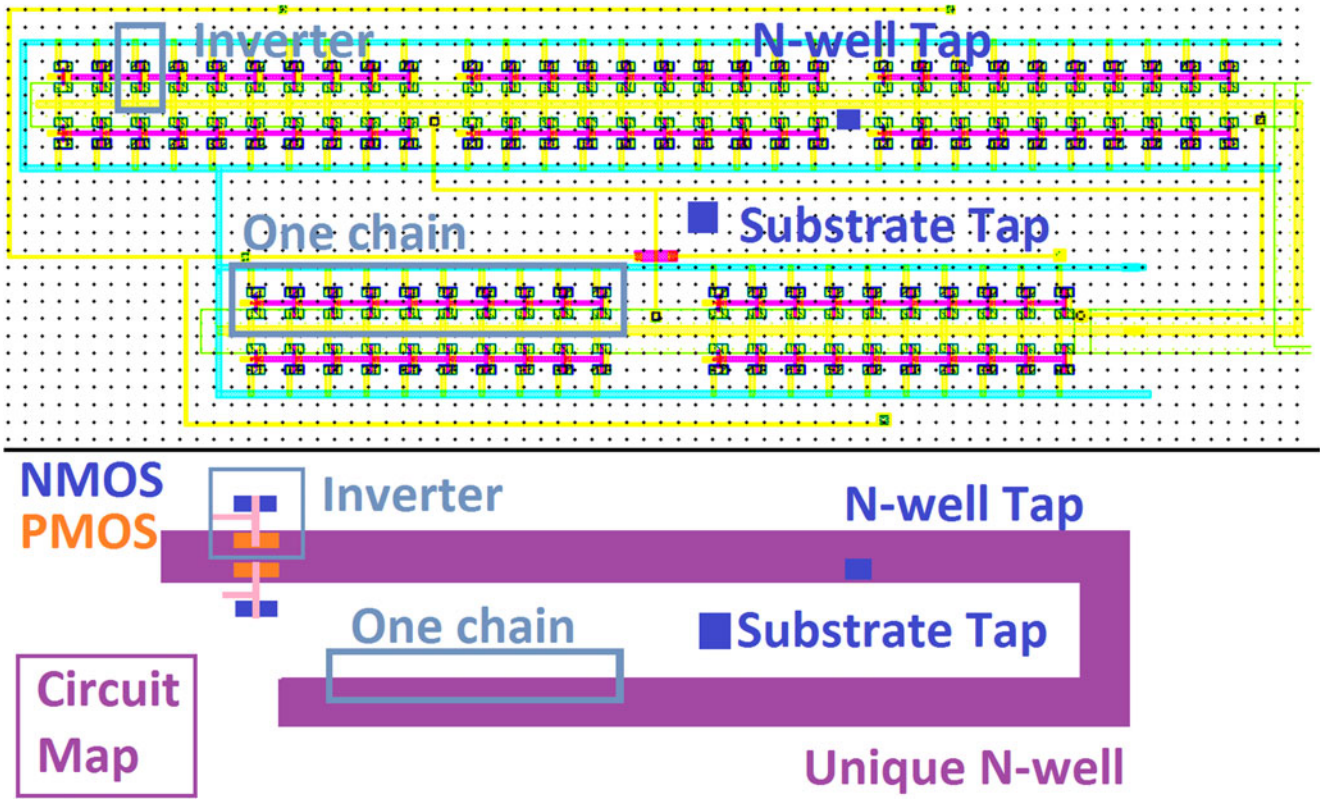

Fig. 9 Inverter chains in back-to-back configuration, with the measuring points indicated. A circuit map is provided for better understanding

sources that are located in the range of hundreds of the size of a minimum inverter can be ignored for the noise analysis.

4.4 Noise Generation by Digital Test Circuit

This analysis focused on the generation of noise due to switching activity in the applied technology. In order to simulate noise profiles due to switching, simple digital circuits operating with high frequency were designed and set in operation. All the circuits consist of ten inverter chains, each with a different spatial configuration. The inverter chains are composed of ten inverters.

The chains were stimulated by square waves with different frequencies, rise and fall times and phase shifts. The frequencies applied were 500 MHz, 750 MHz, 1 GHz, 2 GHz and 3 GHz. For each frequency, five rise and fall times were simulated, with values changing linearly from 1 % to 10 % of the waveform's period. In this environment, the inverter chains inputs had fix and unique phases. While switching, noise is introduced into the substrate due to coupling from the reverse biased source-drain junction capacitances of the transistors during switching [5]. The noise measurement was done in the same way as before by a substrate tie that was placed in the center of the circuit (see Fig. 7). Figures 7, 8 and 9 detail each of the three configurations. The configuration depicted in Fig. 7 is composed of five spatially parallel chains. The test circuit shown in Fig. 8 consists of two groups of five stacked chains. The configuration of Fig. 9 is composed of pairs of chains arranged in a back to back manner, which means the PMOS transistors of each pair share the same N-Well strip. In all three cases, the PMOS devices share the same N-Well and a substrate tap is placed in the center of the structure. N-Well taps were placed too, in order to measure the noise generated there as well.

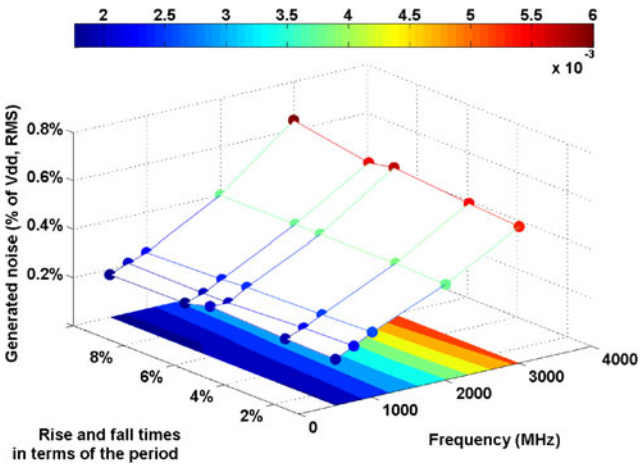

Fig. 10 Noise generated in the substrate by activition (square wave applied) of one inverter chain, for different frequencies and rise/fall times, collected at the substrate tap. The dot markers are the obtained results, while the surface and the colored x-y plane support the visualization

The intention of the following analysis is the exploration of how frequency, transition times and layout configurations affect noise generation.

It follows from the results depicted in Fig. 10 and Fig. 11 that the generated noise varies significantly more with frequency than with rise and fall times. Thereby, Fig. 10 depicts the results for one inverter chain, while Fig. 11 shows the means of the generated noise for all three configurations.

Recalling the results presented in section 4.2, one can conclude that the NMOS version of the sensor would not be activated for such values. For example, Flicker noise induced as voltage requires a RMS value of 6.2 % of V_{DD} in order to activate the sensor. In comparison, the highest generated noise value, measured for frequencies of 3 GHz, is with an RMS value of 0.6 % of V_{DD} by factor 10 lower.

However, a different situation occurs for the noises measured in the N-Well. Figure 12 displays the mean of the generated noise in the N-Well of all three test circuits. The results are similar to the noise generated in the substrate, apart from the fact that the absolute values are higher. Thus, for frequencies of 3 GHz noise RMS levels of up to 1.1 % of V_{DD} are obtained. This value is still lower than the minimum RMS level for false sensor activation of 6.9 % of V_{DD} (White noise induced as current, WCP in Fig. 5). However, both values are in the same order of magnitude. Since the test designs are rather simple, one can expect that much larger or denser circuits can generate sufficient noise to reach critical levels. Therefore, the generated noise should not be neglected. This conclusion can be extended to the NMOS sensor, given the possibility of generation of higher noise levels by more complex circuits.

Thus, even though the analyzed BBICS possess a rather low susceptibility to noise, strategies for enhancing the sensor's noise robustness [19] should be considered if there is a high probability of critical noise level, as identified in section 4.2.

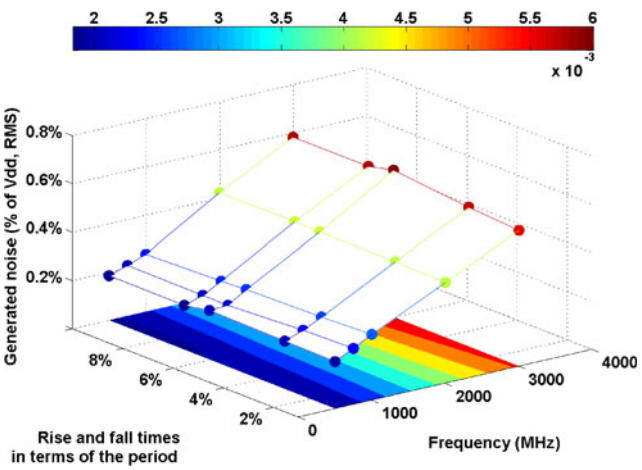

Fig. 11 Mean of the generated noise values in the substrate for varying rise and fall times and frequencies, obtained by each of the three chain configuration simulations

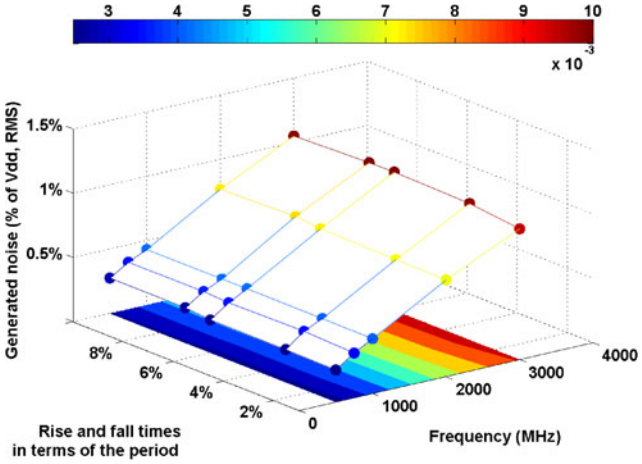

Fig. 12 Mean of the generated noise values for varying rise and fall times and frequency values, obtained by each of the three chain configuration simulations, measured at the N-Well tap

It should be noted that substrate noise not only can lead to false detection, but also might reduce the BBICS's sensibility to detect radiation induced currents. As identified in [32], the weak point is the gate-source voltage $V_{gs,Nh2}$ of the transistor N_{h2} (see Fig. 2), which is identical to the substrate voltage level. In order to activate the tail circuit, and thus, detect radiation induced event, $V_{gs,Nh2}$ must be above the threshold voltage $v_{th,Nh2}$ of N_{h2}. Therefore, the transistor N_{h1} is dimensioned such that the radiation induced current $I_{strike,min}$ that is sufficient to create a SET increases the substrate voltage, i.e., $V_{gs,Nh2}$, above $v_{th,Nh2}$ (see also Eq. 1). However, in the presence of substrate noise the substrate's voltage level might be reduced preventing the detection of a possible SET. Hence, in order to assure the functionality of the BBICS in noisy environments, the maximum expected RMS level $N_{RMS,max}$ of the substrate noise must be

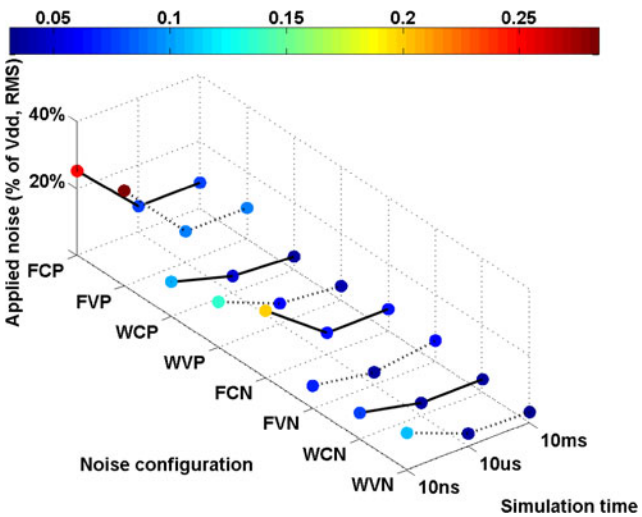

Fig. 13 Required noise RMS level for sensor activation for different duration of the exposure of the sensor to noise

considered. That means, the dimensioning of N_{h1} must be realized such that the current $I_{strike,min}$ increases the substrate voltage to $v_{th,Nh2} + N_{RMS,max}$.

In order to verify this assumption, the PMOS version of the mBBICS had been re-dimensioned considering the maximum RMS value identified in the previous analysis (see Fig. 12). Next, WGN with this RMS value had been added to the substrate while the current $I_{strike,min}$ had been induced to the sensor's input in 20 different time points. Results indicated no missed detection.

4.5 Exposure Time

Since noise possesses a stochastic nature, one could question if 10 μs is sufficient to draw reliable conclusions for the noise susceptibility of bulk sensor. Hence, different exposure times of the sensor to noise have been analyzed.

In order to study the effects caused by different exposure times, the already known iterative procedure for detection of minimum noise RMS values that lead to sensor activation was repeated for durations of 10 ns and 10 ms. The results are presented in Fig. 13.

It is possible to notice little change in the noise RMS value necessary for activation at exposure times in the orders of μs and ms. The maximum difference of 2.4 % of V_{DD} can be observed for FVN (6.1 % for 10 μs and 3.7 % for 10 ms).

However, the results for durations of 10 ns indicate significant variations. Hereby, the determined minimum noise RMS levels for 10 ns and 10 ms differ by up to 19.2 % (FVP). This can be explained by the stochastic nature of noise. Hence, with longer noise exposures, it can be expected that larger, less probable noise peaks are more likely to happen.

Consequently, it can be concluded that the chosen simulation for noise analysis of 10 μs is appropriate for the executed analysis.

The increasing amount of noise source in current designs requires a detailed analysis of noise susceptibility of integrated circuits. This is all the more important for analog sensors measuring substrate effects.

5 Conclusion

This work presents the investigation of the noise tolerance of modular Bulk Built-In Current Sensors that enable to detection of radiation induced transient faults. The analysis is based on extracted layout data, including the substrate profile and different kind of generic noise sources. The results indicate that noise sources close to the sensors lead to false detections if the RMS value is in the range of 5 % to 9 % of V_{DD}. Further, it could be determined that noise sources with distances corresponding to the size of more than 100 minimum inverters can be disregarded.

It could be indicated that noise generated by digital test circuits is lower than the extracted values for false sensor activation. However, given the proximity of the determined values and the potential complexity of the digital circuit, such noise cannot be ignored.

Finally, the results for different exposure times to noise have been compared. The obtained results could indicate that simulations in the range of several μs are sufficient for the conducted analysis.

Future works shall apply the proposed analysis flow exploration of noise in complex and mixed-signal designs. Further aspects shall be the study of the impact of aging and variation effects on the noise susceptibility of the sensors.

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References

1. Arnaud A, Galup-Montoro C (2004) Consistent noise models for analysis and design of CMOS circuits. IEEE Trans Circuits Syst I Reg Papers 51(10):1909–1915. doi:10.1109/TCSI.2004.835028
2. Bastos RP, Di Natale G, Flottes ML, Rouzeyre B (2011) How to sample results of concurrent error detection schemes in transient fault scenarios? In: Proc. 12th European Conference on Radiation and Its Effects on Components and Systems (RADECS), 19–23 Sept. 2011. pp 635–642. doi:10.1109/radecs.2011.6131361
3. Bastos RP, Torres FS, Dutertre JM, Flottes ML, Di Natale G, Rouzeyre B (2013) A Single Built-in Sensor to Check Pull-up and Pull-down CMOS Networks against Transient Faults. In: Proc. 23rd International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)
4. Baumann RC (2005) Radiation-induced soft errors in advanced semiconductor technologies. IEEE Trans Device Mater Reliab 5(3):305–316. doi:10.1109/Tdmr.2005.853449
5. Briaire J, Krisch KS (2000) Principles of substrate crosstalk generation in CMOS circuits. IEEE Trans Comput-Aided Design 19(6): 645–653. doi:10.1109/43.848086
6. Bronckers S, Van der Plas G, Vandersteen G, Rolain Y (2010) Substrate noise coupling mechanisms in lightly doped CMOS transistors. IEEE Trans Instrum Meas 59(6):1727–1733. doi:10.1109/Tim.2009.2024370
7. Checka N (2005) Substrate noise analysis and techniques for mitigation in Mixed-Signal RF Systems. Massachusetts Institute of Technology, USA
8. Checka N, Chandrakasan A, Reif R (2005) Substrate noise analysis and experimental verification for the efficient noise prediction of a digital PLL. IEEE Trans Cust Integr Cir:473–476
9. Cui Y, Niu GF, Rezvani A, Taylor SS (2008) Measurement and modeling of drain current thermal noise to shot noise ratio in 90 nm CMOS. 2008 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Digest of Papers:118–121

10. Garg R, Jayakumar N, Khatri SP, Choi GS (2009) Circuit-Level Design approaches for radiation-hard digital electronics. IEEE Trans VLSI Syst 17(6):781–792. doi:10.1109/Tvlsi.2008.2006795
11. Karnik T, Hazucha P (2004) Characterization of soft errors caused by single event upsets in CMOS processes. IEEE Trans Dependable Secure Comput 1(2):128–143. doi:10.1109/TDSC.2004.14
12. Katsikadelis J (2002) Boundary elements theory and applications. Elsevier
13. Le J, Hanken C, Held M, Hagedorn MS, Mayaram K, Fiez TS (2012) Experimental characterization and analysis of an asynchronous approach for reduction of substrate noise in digital circuitry. IEEE Trans. VLSI Syst 20(2):344–356. doi:10.1109/Tvlsi.2010.2100835
14. Leach WM (1994) Fundamentals of Low-Noise Analog Circuit-Design. IEEE P 82(10):1515–1538. doi:10.1109/5.326411
15. Leite F, Balen T, Herve M, Lubaszewski M, Wirth G (2009) Using bulk built-In current sensors and recomputing techniques to mitigate transient faults in microprocessors. In: Proc. Latin Amer Test Work, pp 147-152
16. Lyons RE, Vanderkulk W (1962) The use of triple-modular redundancy to Improve Computer reliability. IBM J Res Dev 6(2):200–209
17. Mahmutoglu AG, Demir A, Roychowdhury J (2013) Modeling and Analysis of (Nonstationary) Low Frequency Noise in Nano Devices: A Synergistic Approach based on Stochastic Chemical Kinetics. 2013 Ieee/Acm. In: Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp 500–507
18. Manghisoni M, Ratti L, Re V, Speziali V, Traversi G (2006) Noise Characterization of 130 and 90 nm CMOS Technologies for Analog Front-end Electronics. In: Proc. IEEE Nucl Sci Conf pp 214–218. doi:10.1109/Nssmic.2006.356142
19. Melo JGM, Sill Torres F, Bastos RP (2015) Exploration of Noise Robustness and Sensitivity of Bulk Current Sensors for Soft Error Detection. In: Proc. 6th International Workshop on, Salvador, Brazil
20. Miyoshi T, Arai Y, Ahmed M, Kapusta P, Ichimiya R, Ikemoto Y, Fujita Y, Tauchi K, Takeda A (2012) High-Resolution Monolithic Pixel Detectors in SOI Technology. In: Proc. 6th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging
21. Narsale A, Huang MC (2009) Variation-tolerant hierarchical voltage monitoring circuit for soft error detection. In: Proc. Int Symp Quality Electronic Design, 16–18 March 2009. pp 799–805. doi:10.1109/isqed.2009.4810395
22. Nassar M, Dabak A, Il Han K, Pande T, Evans BL (2012) Cyclostationary noise modeling in narrowband powerline communication for Smart Grid applications. In: Proc. IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), 25–30 March 2012. pp 3089–3092. doi:10.1109/ICASSP.2012.6288568
23. Neto EH, Ribeiro I, Vieira M, Wirth G, Kastensmidt FL (2006) Using bulk built-in current sensors to detect soft errors. IEEE Micro 26(5):10–18
24. Neto EH, Kastensmidt FL, Wirth G (2008) Tbulk-BICS: A built-In current sensor robust to process and temperature variations for soft error detection. IEEE Trans Nucl Sci 55(4):2281–2288. doi:10.1109/Tns.2008.920426
25. Oh Y, Jeon S, Rieh JS (2010) Variation in RF performance of MOSFETs due to substrate digital noise coupling. IEEE Microw Wirel Co 20(7):384–386. doi:10.1109/Lmwc.2010.2049431
26. Ong SN, Yeo KS, Chew KWJ, Chan LHK (2014) Substrate-induced noise model and parameter extraction for high-frequency noise modeling of sub-Micron MOSFETs. IEEE Trans Microw Theory 62(9):1973–1985. doi:10.1109/Tmtt.2014.2340375
27. QRC Substrate Technology Characterization Manual Product Version 11.1.2 (2012) Cadence Design Systems, Inc
28. Reference Manual for Generic 90 nm Salicide 1.2 V/2.5 V 1P 9 M Process Design Kit (PDK) Revision 4.3. (2008) Cadence Design Systems, Inc
29. Salman E (2009) Switching noise and timing characteristics in nanoscale integrated circuits. University of Rochester, New York
30. Shoji M (2014) Theory of CMOS digital circuits and circuit failures. Princeton University Press
31. Shomalnasab G, Zhang LH (2015) New analytic model of coupling and substrate capacitance in Nanometer Technologies. IEEE Trans Vlsi Syst 23(7):1268–1280. doi:10.1109/Tvlsi.2014.2334492
32. Sill Torres F, Possamai Bastos R (2013) Detection of transient faults in Nanometer Technologies by using modular built-In current sensors. Integrated Circuits Syst J 8(5):89–97
33. Srinivasan J, Adve SV, Bose P, Rivers JA (2004) The impact of technology scaling on lifetime reliability. In: Proc. International Conference on Dependable Systems and Networks, pp 177–186. doi:10.1109/dsn.2004.1311888
34. Stanisic BR, Verghese NK, Rutenbar RA, Carley LR, Allstot DJ (1994) Addressing substrate coupling in Mixed-mode ics - simulation and power distribution synthesis. IEEE J Solid-St Circ 29(3):226–238. doi:10.1109/4.278344
35. Uemura S, Hiraoka Y, Kai T, Dosho S (2012) Isolation techniques against substrate noise coupling utilizing through silicon via (TSV) process for RF/Mixed-signal SoCs. IEEE J Solid-State Circuits 47(4):810–816. doi:10.1109/JSSC.2012.2185169
36. Vargas F, (1994) Nicolaidis M SEU-tolerant SRAM design based on current monitoring. In: 24th Fault-Tolerant Computing Symp. FTCS-24. Digest of Papers., 15–17 Jun 1994. pp 106–115. doi:10.1109/ftcs.1994.315652
37. Velthuis JJ, Drasal Z, Hanninger G, Kohrs R, Mathes M, Reuen L, Scheirich D, Andricek L, Pascual IC, Chen X, Dolezal Z, Fischer P, Frey A, Fuster JA, Koch M, Kodys P, Kvasnicka P, Kruger H, Llacer CL, Lodomez P, Moser HG, Peric I, Raspereza A, Richter R, Rummel S, von Torne E, Wermes N (2008) A DEPFET based beam telescope with submicron precision capability. IEEE Trans Nucl Sci 55(1):662–666. doi:10.1109/TNS.2007.914031
38. Wolfel S, Herrmann S, Lechner P, Lutz G, Porro M, Richter RH, Struder L, Treis J (2007) A novel way of single optical photon detection: beating the 1/f noise limit with Ultra high resolution DEPFET-RNDR devices. IEEE Trans Nucl Sci 54(4):1311–1318. doi:10.1109/Tns.2007.901225
39. Zhichao Z, Tao W, Li C, Jinsheng Y A (2010) new Bulk Built-In Current Sensing circuit for single-event transient detection. In: Proc. 23rd Canadian Conference on Electrical and Computer Engineering (CCECE), 2–5 May 2010. pp 1–4. doi:10.1109/ccece.2010.5575124

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