Radiation Sensitivity of XOR Topologies in Multigate Technologies under Voltage Variability

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***Abstract*—Integrated Circuits are becoming more susceptible to numerous effects due to the reduction of its robustness to external noise. Additionally, the increase of uncertainty degree related to the many sources of variation in the manufacturing process contributes to the reliability issues. This work is aimed at presenting a comparative analysis of radiation sensitivity of different XOR implementations using two multigate devices: double-gate FinFET and Trigate. Trigate-based circuits have shown to be more robust than FinFET with improvement percentage from 6,2% up to 12,6% in the threshold LET. Further, voltage fluctuation can reduce the threshold LET up to 20,8%, increasing the susceptibility of the analyzed circuits.**

Keywords—Radiation Sensitivity; FinFET; Trigate; XOR logic gate; Voltage Variability

I. INTRODUCTION

Advances in microelectronics have contributed to the size reduction of the technological nodes, lowering the threshold voltage and increasing the operating frequency of the systems. Although, it has positive outcomes related to the performance and power consumption of VLSI circuits, this improvement brings new challenges such as increased soft error rates, pronounced variability effects and Short-channel Effects (SCE). For instance, particles with low energy found on the surface of the Earth, previously neglected, are now able to interfere with the operation of a circuit [1][2]. Also, electrical characteristics of devices from the same circuit can vary widely, resulting in high deviation on performance metrics and abnormal power consumption due to process, voltage and temperature variations [3][4].

To overcome the challenges imposed by the technology scaling, many works have been carried out to propose new materials or devices structures [5][6]. Multigate FET (MuGFET) devices are replacing the planar bulk CMOS at sub-22nm nodes due to its improved short-channel controllability, lower leakage and better yield. This behavior is achieved in virtue of the MuGFETs have strong electrostatic control over the channel due to the reduced coupling between source and drain region provided by multiple gate electrodes [7]. These devices can be designed either in Silicon-on-Insulator (SOI) substrate or in bulk-silicon substrate due to fabrication process similarity with the bulk CMOS one. Besides the lower fabrication cost and better process compatibility, bulk-silicon based MuGFET are widely used to improve heat transfer to the substrate [8]. Fin-like structure devices have reduced thermal conductivity due to small and confined dimensions of the fin and bulk-based substrate devices exhibit better thermal performance compared to SOI substrates devices [9].

Among of the MuGFET devices proposed in the past few years in the literature, the double-gate FinFET (Fin-Shaped Field Effect Transistor) and Trigate MOSFET (Trigate fully-depleted MOSFET) are the most indicated as promising candidates to further transistor scaling [10][11]. Three-dimensional multigate technology provides a better response to the ionizing radiation effects due to its narrow sensitivity volumes compared to planar devices [12]. The sensitive volume is defined as the critical silicon volume, which highly collects the deposited charge leading to the radiation-induced transient pulse [13]. Although multigate devices show better robustness, when the bulk technology is used over the SOI, additional charges are accumulated due to the diffusive component in the charge collection process. At SOI-based devices, the buried oxide structure suppresses this diffusion mechanism leading to eight times less of collected charge [13]. The differences in the collected charges are significant for advanced technologies where the critical charge is on the order of tens of femto coulombs.

This work focuses on the analysis of these two multigate devices in three bulk technology nodes against the effects of radiation. The set of analyzed circuits is composed of ten different topologies of exclusive-OR (XOR) logic gates due to its importance in VLSI circuits and its plurality of design implementations provided in the literature. The XOR logic gate is a fundamental component in arithmetic circuits such as full adders, multipliers, comparators, parity-generators and majority voters. Therefore, providing significant effort to analyze its sensitivity to radiation effects will enhance the robustness of systems to these effects. To the extent of our knowledge, no work has been done in order to analyze different XOR topologies to the radiation effects using advanced technologies. Ten different topologies exploiting the complementary CMOS and PTL (Pass-Transistor Logic) logic families are investigated against radiation effects using double-gate FinFET and Trigate MOSFET devices. In contrast to complementary CMOS logic family, which only allows inputs to drive gate terminals, the PTL concept allows the inputs to drive the source-drain terminal as well [14]. Because of this, a logic operation can be performed with only one transistor network (pull-down or pull-up) reducing the number of transistors compared to the CMOS implementation, which requires two complementary networks. Fig. 1 shows the ten topologies analyzed in this work.

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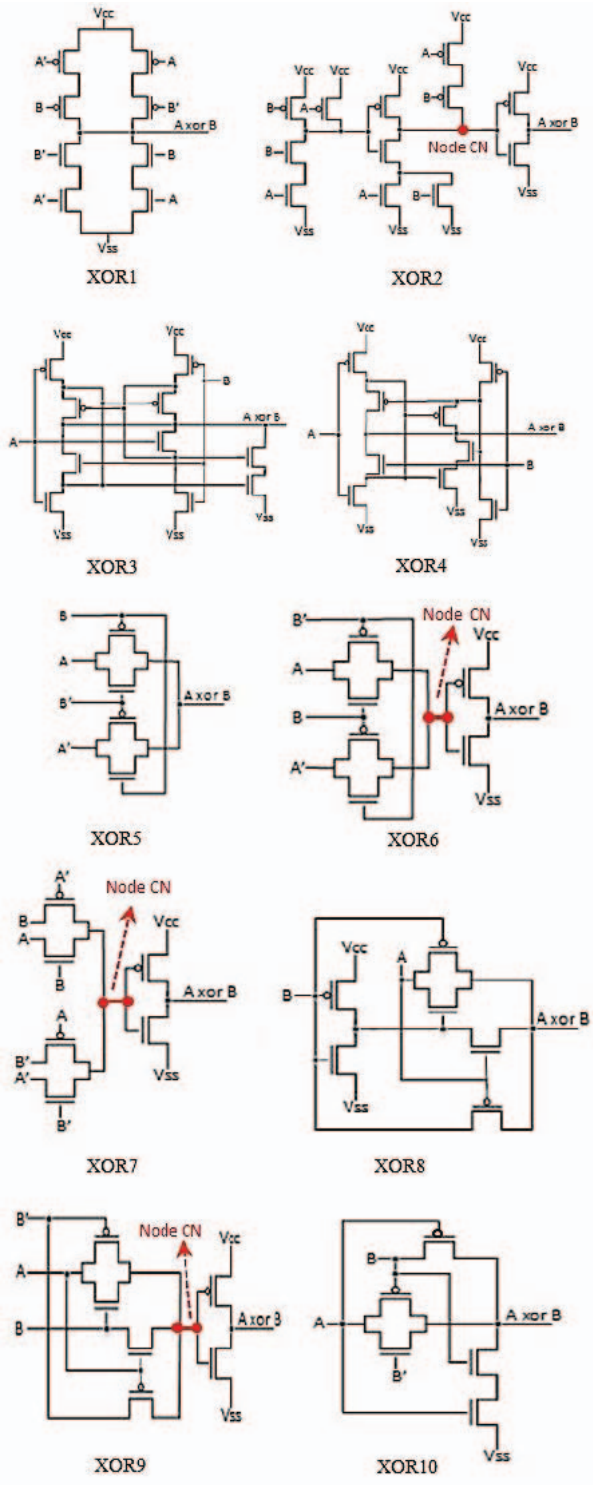


Fig. 1. Exclusive-XOR topologies. Adapted from [15].

II. Evaluation of Radiation Sensibility

In this work, it is considered two multigate devices: bulk FinFET (double-gate device) and Trigate MOSFET (triple-gate device). Both devices are simulated using the model provided by Arizona State University, through PTM (Predictive Transistor Model) at 7nm, 14nm and 20nm bulk technology node [16]. The electrical and process parameters from the model are presented in Table I. The same parameter values are used for both multigate devices, however, the FinFET devices have a hard mask (thick SiO_2 layer) on top of the fin to prevent the electrostatic influence from a third gate electrode.

TABLE I
Electrical and Process Parameters from PTM for Bulk Multigate Technology

Parameter		Technology (nm)		
		7	14	20
Supply Voltage (V)		0.70	0.80	0.90
L_G (nm)		11	18	24
H_{FIN} (nm)		18	23	28
T_{FIN} (nm)		6.5	10	15
T_{OX} (nm)		1.15	1.3	1.4
Channel Doping (m^{-3})		1e22	5e22	5e23
Source / Drain Doping (m^{-3})		3e26	3e26	3e26
Workfunction (eV)	N	4.42	4.42	4.38
	P	4.74	4.75	4.80

The fault injection simulation of a particle hit at the P-N junction of a device was carried at the circuit level using SPICE. All circuit simulations were conducted with FO1 (three-stage inverter chain). The radiation-induced current pulse has a very characteristic waveform: a very fast linear rise due to the funneling process and an exponential slow decay due to the diffusive component in the charge collection process. Accordingly, it was modeled as a double exponential transient pulse by inserting a current source at the stroke sensitive node as described in Eq. (1) [17], where Q_{coll} is the amount of charge collected due to a radiation particle strike in the sensitive region. The term τ_α is the collection time constant of the junction and τ_β is the ion track establishment time constant. For the devices used in this work, theses constants are equal to 20ps for τ_α and 2ps for τ_β [18][19].

$$\begin{cases} I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right) \\ Q_{coll} = 10.8 \times L \times LET \end{cases} \quad (1)$$

The Linear Energy Transfer (LET) is the amount of energy released by a particle per unit length crossed in sensitive region of the device. The charge collection depth (L) decreases with the technology scaling and depends on the device structure as well. Hence, the key dimensional parameter for the charge collection depth in Fin-like technology is the thickness of the fin structure [12][20].

The first step in the radiation sensitivity evaluation was to identify the most sensitive node at each XOR topology. A fault injection using a particle with LET = 60fC/μm was performed at each node of the circuits considering all possible input vectors. In these experiments, it was considered the error analyses, i.e., when the transient pulse propagates to the output of the circuit (the input vector), and its amplitude and width. This data allows to determine which node is the most sensitive, as well as the input vector and nature of the radiation-induced pulse (strike at P-type device or N-type device, i.e. 101 or 010 pulse waveform) characterizing the worst radiation sensitive case. It was found that the output node is not necessarily the most sensitive node of a circuit.

Table II summarizes the obtained results. A XOR1, that is a classical circuit in cell libraries, has a number of five sensitive nodes while the alternative topologies own only three or two. This comparison highlights that the XOR implementation usually found in such libraries is not the best option in terms of robustness to radiation effects. For reliable systems, one should reconsider the XOR implementation to increase the design radiation robustness.

TABLE II
NUMBER OF SENSITIVE NODES, CRITICAL NODE, INPUT VECTOR AND TRANSIENT NATURE FOR THE WORST RADIATION SENSITIVE CASE

	# of sensitive nodes	Critical Node	Input Vector	Transient Pulse
XOR1	5/5	Output node	01	101
XOR2	3/6	Node CN	00	101
XOR3	3/4	Output node	00	010
XOR4	3/4	Output node	10	101
XOR5	3/3	Output node	10	101
XOR6	3/4	Node CN	00	101
XOR7	3/4	Node CN	00	101
XOR8	2/2	Output node	01	101
XOR9	2/3	Node CN	00	101
XOR10	3/3	Output node	01	101

After identifying the worst radiation sensitive case for each XOR circuit, the threshold LET is obtained iteratively by changing the amount of charge collected described in the transient current source netlist description. The threshold LET was defined, according to Eq. (2), as the minimum charge needed by a transient pulse to propagate until the output node with amplitude greater than half the value of the nominal voltage. Table III summarizes the threshold LET obtained for FinFET and Trigate at 7nm, 14nm and 20nm.

$$LET_{th}\ (pC/\mu m) = \min_{I_{peak} > \frac{Vdd}{2}} \int I(t)dt \qquad (2)$$

In order to analyze the impact of voltage variability encountered at VLSI circuits, experiments were conducted considering both a 10% increase of nominal supply voltage and a decrease of 10%. As expected, the threshold LET of a circuit has a direct relation with its supply voltage. Thus, the voltage variability has a great impact in the results by increasing the threshold LET for higher supply voltages and by decreasing it for lower supply voltages (consequently, increasing the sensitivity of the circuits).

Table III also summarizes the voltage variability impact at the threshold LET. The circuit XOR5 has shown to be the most sensitive to the voltage variation at both devices in all technologies node. For both devices, it is encountered a threshold LET reduction of around 20% for 7nm and 14nm, and a reduction of around 15% for 20nm when the supply voltage equals to $0.9*VDD_{NOMINAL}$. The less sensitive to these variations were the XOR2 at 7nm FinFET and Trigate and XOR3 at 14nm both devices. At 20nm, the most robust was XOR1 for FinFET device and XOR3 for Trigate device. However, the most robust circuit to this variation is the XOR2 topology with threshold LET reduction of 18,1%.

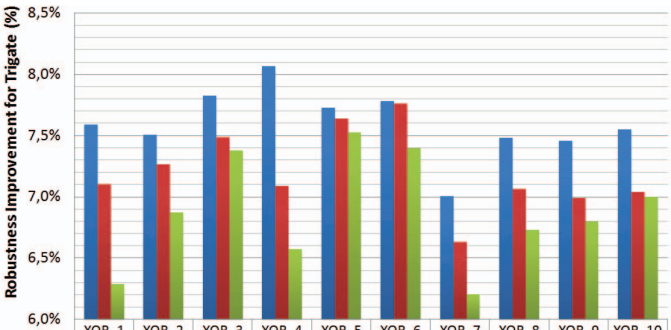
Finally, this work compares Trigate and FinFET circuits. The Trigate-based XOR circuits have performed an improved robustness compared to the FinFET technology at the three technologies analyzed in this work. This can be explained by the improved gate electrostatic control over the channel due to its additional gate electrode influence. As shown in Table III, at 7nm technology node, the XOR6 circuit has shown to be the most robust topology in both multigate devices with LET_{th} = 16.52fC/μm for Trigate and LET_{th} = 15.33fC/μm for FinFET. XOR6 topology has also proved to be the most robust circuit at 14nm and 20nm in FinFET and Trigate technologies. It has a LET_{th} = 22.83fC/μm for 14nm Trigate and LET_{th} = 20.44fC/μm for 14nm FinFET. At 20nm technology node, it has LET_{th} = 22.42fC/μm for Trigate and LET_{th} = 20.29fC/μm for FinFET.

The most sensitive circuit was the XOR4 topology with approximately 17% of reduction on the threshold LET for 7nm Trigate and FinFET. At 20nm technology node, it has a reduction of approximately 28% for Trigate and FinFET. In addition, the XOR8 circuit has shown to be the most sensitive XOR design at 14nm technology with LET_{th} = 18.43fC/μm for Trigate and LET_{th} = 16.63fC/μm for FinFET.

Figure 2 and Figure 3 shows this improvement in percentage for each circuit for 7nm and 20nm, respectively. At 7nm technology node, the improvement can range from 6.2% up to 8.1% considering the voltage variability. At nominal supply voltage (V_{DD}), the maximum robustness improvement was 7.8% over the threshold LET for the XOR6 circuit in FinFET devices. The improvement range predicted to these circuits at 14nm Trigate can range from 9.2% to 12.6%, with the maximum improvement, at nominal voltage, for the XOR5. In Figure 3, it can be observed a wider improvement range at 20nm technology node. It ranges from 7.2% to 11.2% with the minimum and maximum improvement for the XOR4 and XOR6, respectively.

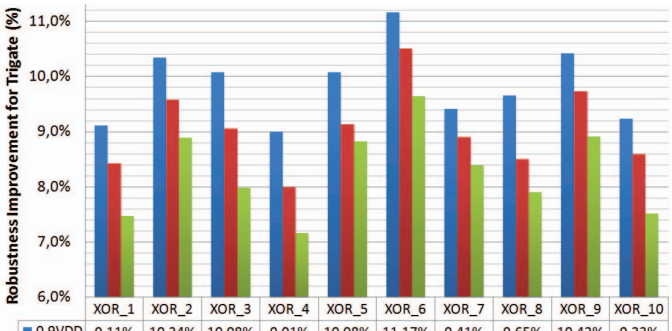
TABLE III
THRESHOLD LET FOR FINFET AND TRIGATE TECHNOLOGY
(fC/μm)

Topology	7nm						14nm						20nm					
	FinFET			Trigate			FinFET			Trigate			FinFET			Trigate		
	-10%	VDD	+10%	-10%	VDD	+10%	-10%	VDD	+10%	-10%	VDD	+10%	-10%	VDD	+10%	-10%	VDD	+10%
XOR1	10.67	13.07	15.52	11.48	14.00	16.50	14.02	17.02	20.07	15.57	18.83	22.07	13.38	15.55	18.97	14.60	16.86	18.97
XOR2	11.26	13.76	16.29	12.11	14.76	17.40	14.95	18.07	21.21	16.61	20.02	23.42	14.90	17.33	21.46	16.44	18.99	21.46
XOR3	12.48	15.26	18.07	13.45	16.40	19.40	15.60	18.79	21.98	17.33	20.80	24.27	15.15	17.61	21.61	16.67	19.20	21.61
XOR4	10.33	***12.76***	15.21	11.17	***13.67***	16.21	13.71	16.71	19.79	15.19	18.45	21.77	12.69	***14.83***	18.17	13.83	***16.02***	18.17
XOR5	11.10	14.02	17.40	11.95	15.10	18.71	14.98	18.71	22.76	16.81	21.07	25.35	15.12	17.98	22.62	16.64	19.62	22.62
XOR6	12.24	**15.33**	18.67	13.19	**16.52**	20.05	16.55	**20.44**	24.50	18.51	**22.83**	27.32	17.10	**20.29**	25.71	19.01	**22.42**	25.71
XOR7	11.21	13.82	16.50	12.00	14.74	17.52	15.35	18.79	22.35	16.87	20.64	24.40	15.08	17.80	22.29	16.50	19.38	22.29
XOR8	10.40	12.81	15.21	11.18	13.71	16.24	13.68	***16.63***	19.64	15.22	***18.43***	21.71	12.95	15.12	18.52	14.20	16.40	18.52
XOR9	10.86	13.29	15.76	11.67	14.21	16.83	14.36	17.39	20.45	15.94	19.25	22.57	14.05	16.38	20.36	15.51	17.98	20.36
XOR10	10.40	12.86	15.31	11.19	13.76	16.38	13.80	16.86	19.90	15.31	18.63	21.96	13.02	15.24	18.74	14.23	16.55	18.74



	XOR_1	XOR_2	XOR_3	XOR_4	XOR_5	XOR_6	XOR_7	XOR_8	XOR_9	XOR_10
0.9VDD	7,59%	7,51%	7,82%	8,06%	7,73%	7,78%	7,01%	7,48%	7,46%	7,55%
VDD	7,10%	7,27%	7,49%	7,09%	7,64%	7,76%	6,63%	7,06%	6,99%	7,04%
1.1VDD	6,29%	6,87%	7,38%	6,57%	7,52%	7,40%	6,20%	6,73%	6,80%	7,00%

Fig. 2. Percentage increase in Threshold LET for 7nm Trigate XOR topologies.



	XOR_1	XOR_2	XOR_3	XOR_4	XOR_5	XOR_6	XOR_7	XOR_8	XOR_9	XOR_10
0.9VDD	9,11%	10,34%	10,08%	9,01%	10,08%	11,17%	9,41%	9,65%	10,42%	9,23%
VDD	8,42%	9,57%	9,06%	7,99%	9,14%	10,50%	8,90%	8,50%	9,74%	8,59%
1.1VDD	7,47%	8,89%	7,98%	7,16%	8,82%	9,64%	8,40%	7,91%	8,92%	7,51%

Fig. 3. Percentage increase in Threshold LET for 20nm Trigate XOR topologies

III. Conclusions

A comparative analysis of radiation sensitivity at different XOR logic gate topologies based on FinFET and Trigate devices are introduced in this paper. Exploiting two widely used logic implementation concept, ten different XOR topologies were analyzed against radiation effects considering voltage variability. It was found that not necessarily the output node of a logic gate is characterized as the most sensitive node. The topologies with multiple logic stages might have the most sensitive node as an internal node, depending on the drive strength of each stage. For all analyzed circuits, trigate-based circuits have shown to be more robust than the FinFET-based. XOR6 has shown to be the least sensitive to radiation effects for all three technologies in study, considering both devices. Further, at 7nm and 20nm, XOR4 is the most sensitive in both devices while XOR8 is the most sensitive at 14nm. Considering the variability, XOR5 was the most sensitive circuit to the supply voltage variation while XOR2 or XOR3 were the most robust. As future work, it is proposed to analyze the radiation robustness of majority voter topologies using XOR logic gates. The majority voters constitute a critical point of failure in reliable systems, in which it is applied hardware redundancy through TMR, for example.

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