Exploring Multi-level Design to Mitigate Variability and Radiation Effects on 7nm FinFET Logic Cells

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***Abstract*—This work evaluates the advantages of adopting multi-level design on logic cells instead of complex gates to mitigate process variability and radiation effects. At nominal conditions, as expected, the best choice is to use complex gate topology to minimize the power consumption and increase the performance. On the other hand, the use of multi-level arrangements became the functions up to 50% less sensitive to the transient faults and at least 30% more robust to the process variability effects. For designs with the emphasis on area constraints, a trade-off needs to be done.**

***Index Terms*—reliability, process variability, radiation effects, FinFET technology.**

I. Introduction

Bulk CMOS technology has reached its physical limit. This technology suffers from the undesirable leakage currents, soft errors and Short-Channel Effects (SCE) [1][2]. The use of multi-gate devices is an option to overcome these obstacles and continue the technology scaling because these devices provide better control of SCE, lower leakage currents and better yield [3]. FinFET (Fin-Shaped Field Effect Transistor) technology is used as the main multi-gate device replacing MOSFET devices in sub-22nm technology nodes [4].

The technology scaling has increased the importance of studying the reliability issues of integrated circuits. Two of the most significant adverse effects on the reliability of digital design are Process Variability and Radiation Effects [5][6]. These variations can compromise entire blocks of cells or reduce the performance and energy efficiency of the chip. Few works address these two effects together on the circuit design. Transistor arrangement is a technique explored to design faster circuits [7], deal with Bias Temperature Instability (BTI) effects [8] and improve design robustness against permanent and transient faults. Adoption of complex gates reduces the number of transistors, delay and power consumption. However, they can introduce challenges related to regularity and reliability that might be avoided with more regular and basic cells.

The primary objective of this work is to evaluate the impact of process variability and Single Event Transient (SET) on a set of complex logic gates considering different transistor topologies at the layout level. A comparison is made between complex logic gates in their traditional versions and a multi-level of basic logic gates that implement the same function using only NAND2 cells in 7nm FinFET technology.

II. Methodology

This work explores different transistor arrangements for a set of seven logic functions at the layout level to evaluate the process variability impact and radiation effects. Two different topologies of transistor arrangement are investigated: 1) complex gate: optimized functions designed as a complex logic gate CMOS topology; and 2) the multi-level of NAND2 gates: the functions are converted using De Morgan's theorem into the only NAND2 transistor arrangements.

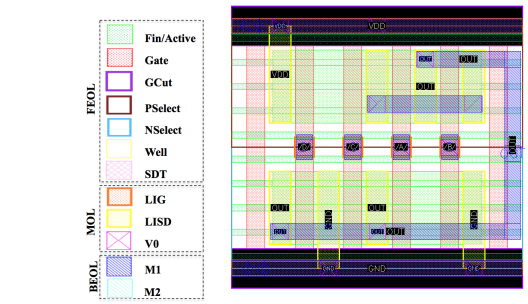
All layouts were designed using the 7nm FinFET ASAP7 Process Design Kit (PDK), developed by Arizona State University in partnership with ARM [9]. Table I summarizes the key devices parameters and the main layout layers from ASAP7. The nominal supply voltage is 0.7V, and all cells adopt three fins as transistor sizing. The cell height is set to 7.5 tracks of metal 2 (M2) that correspond to 0.27μm for all cells evaluated. In this technology, it is necessary to insert a TAP cell to connect the PFET and NFET back-gates to the source pins V_{DD}/G_{ND}, respectively. This is a PDK restriction, and this procedure is necessary for the proper circuit operation. The TAP cell layout an area of $0.02916\mu m^2$.

As an example, the layout of AOI211 gate is presented on Fig. 1a and Fig. 1b. All layouts were validated by Design Rule Check (DRC) and Layout Versus Schematic (LVS) steps. The extracted netlist with parasite capacitances is obtained and it was used for the process variability analysis and radiation effects evaluation. From the extracted netlist, SPICE simulations are performed. The input switching frequency is set at 500MHz and inverters are connected to the input sources introducing realistic delays to the cells. All cells drive a Fanout 4 output capacitance. The project flow carried out in this work can be seen in Fig. 2.

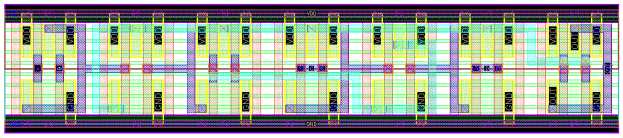
The analyses of this work were divided into three stages presented below. In addition to comparing the results obtained in each stage, a general comparison of the results is also performed. The objective is to highlight which transistor arrangement presents the best results aiming process variability and transient faults.

A. Nominal Conditions

Nominal values are used as a form of reference values to evaluate the variability and radiation effects. Propagation times



(a) AOI211



(b) AOI211_NAND

Fig. 1. AOI211 layout in the two topologies: (a) complex and (b) multi-level of NAND2.

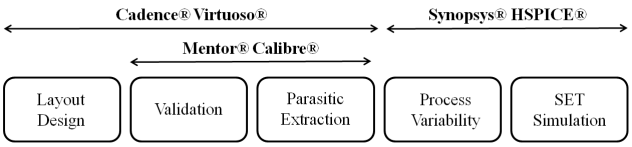


Fig. 2. Project flow for all analyzes.

and the power consumption of the seven cells in different arrangements are compared considering the worst case. Typical characteristics of each gate and arrangement were analyzed.

B. Process Variability

Metal gate devices suffer from the work-function fluctuation (WFF) caused by the misalignment of metal grains in the gate. This fluctuation exhibits a multi-nominal distribution, which can be approximated by a Gaussian distribution if the number of grains on the surface of metal-gate is high enough (>10) which corresponds to the FinFET ASAP7 model characteristics. Thus, the WFF of each device is varied according to a Gaussian distribution with a 3-sigma deviation of 3% the WFF [10]. Two thousand simulations were run for each logic gate [11]. Timing and power consumption measurements were taken for each Monte Carlo simulation. Robustness analysis was performed using the sigma/mean ratios of each delay arc, always aiming at the worst case.

C. Radiation Effects

The third stage considers the effects of radiation through the insertion of transient faults. The SET fault injection is modeled as the Messenger's equation shown in Eq. 1, where $Qcoll$ is the collected charge, τ_α $(1.64 \times 10^{-10}s)$ is the collect charge timing constant, τ_β $(5 \times 10^{-11}s)$ is the timing constant to establish the ion track and L $(2\mu m)$ is the charge collection depth [12]. This effect is reproduced on the SPICE simulation as a current source, simulating the SET effects on the transistors.

$$I(t) = \frac{Qcoll}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) \qquad (1)$$

$$Qcoll = 10.8 \times L \times LET$$

This work follows the parameter and methodology presented in [13], investigating the effects of SET 010 and 101 in all devices of the two inverter circuits. Thus, a current source is inserted into each internal node and the output of the circuit. Also, this evaluation considers all the input vectors for the selected logic gates.

The simulation adopts a linear energy transfer (LET) of $1MeV - cm^2/mg$. The fault is detected if the output of the circuit is bigger than $V_{DD}/2$ for logic level '0' and smaller than $V_{DD}/2$ for logic level '1'; otherwise, the fault is considered masked. The fault masking is determined by Eq. 2, considering the ratio between the number of faults detected and the total faults inserted, i.e., a fault inserted in each internal node and the output, for each test vector of the circuit.

$$Fault\ Masking = \frac{Faults\ Detected}{Total\ Inserted\ Faults} \qquad (2)$$

III. Results

These functions implemented with different transistor arrangements have an impact on the area that only with layout analysis it is possible to measure. Table II shows the area for each logic gate in the two topologies used. All gates designed with the multi-level topology show an increase in the area at least 40%.

TABLE I
THE DEVICE PARAMETERS AND LAYOUT LAYERS FROM ASAP7 [9]

Device Parameters			Layout Layers (nm)		
Gate Length (LG)		21nm		Width	Pitch
Fin Width (WFIN)		6.5nm	**Fin**	6.5	27
Fin Height (HFIN)		32nm	**Active**	54	108
Oxide Thickness (Tox)		2.1nm	**Gate**	21	54
Channel Doping		$1\times10^{22}m^{-3}$	**SDT/LISD**	25	54
Source/Drain Doping		$2\times10^{26}m^{-3}$	**LIG**	16	54
Work	**NFET**	4.3720eV	**VIA0-3**	18	25
Function	**PFET**	4.8108eV	**M1-3**	18	36

TABLE II
AREA USED FOR EACH LOGIC GATE IN BOTH TOPOLOGIES

Logic Functions	Area (μm^2)	
	Complex	**Multi-level**
AOI21	0.085	0.271
OAI21	0.085	0.271
AOI22	0.102	0.271
OAI22	0.102	0.475
AOI211	0.102	0.475
OAI211	0.102	0.407
XOR	0.203	0.339

A. Nominal Conditions

Complex gates are used to reduce delay, power and area. Fig. 3 and Fig. 4 show the results at nominal conditions, demonstrating how the reduced number of transistors contribute to smaller propagation times and power for all seven gates evaluated. OAI211 gate shows the best comparison between complex and multi-level styles, but with an increase of 31.8% on the propagation time. However, the multi-level design alternative can insert a degradation over 80% on the delay. Observing the power consumption, Fig. 4 shows that AOI211 cell also presents the worst results. This cell presents the higher power consumption among all the cells and an increase in power around 145% compared to complex topology.

B. Process Variability

However, the nominal behavior changes under process variability and radiation effects. Table III presents the results of delay and power, showing the mean (μ) and standard deviation (σ) obtained from the Monte Carlo evaluation for all the gates and topologies explored in this work under process variability. For complex topologies, the process variability effects on the mean of delay and power are very close to the nominal behavior but with a significant standard deviation. All complex cells presented significant higher standard deviation compared to multi-level topologies.

To allow a comparative evaluation is important to evaluate the complex cell standard deviation about the mean values. Fig. 5 shows the normalized standard deviation by mean (σ/μ) for each layout. Under process variability, all gates show a larger deviation in the complex arrangement. In the delay results that difference may overcome 90% in comparison with the NAND2 arrangement. Delay deviation of NAND2 topologies is always smaller than 11%, showing more robustness to process variability impact. OAI211 and XOR cells are the least sensitive cells in the complex topology. However, even in these cases, the delay deviation is about 45% greater than the deviation using NAND2 topology. The behavior of the AOI211 cell highlights the relevance of the NAND2 topology to mitigate process variability effects: the complex version presents the highest deviation, over 21%, but with NAND2 topology, this deviation is reduced to approximately 10%,

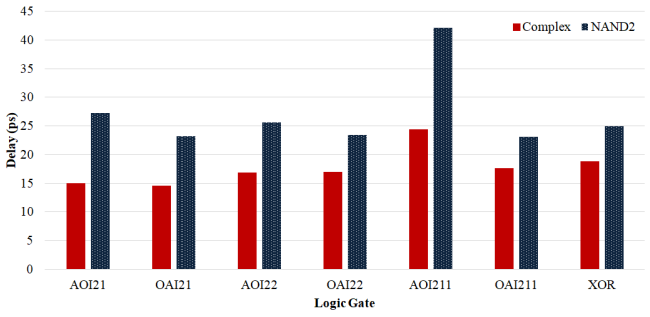


Fig. 3. Delay at nominal conditions.

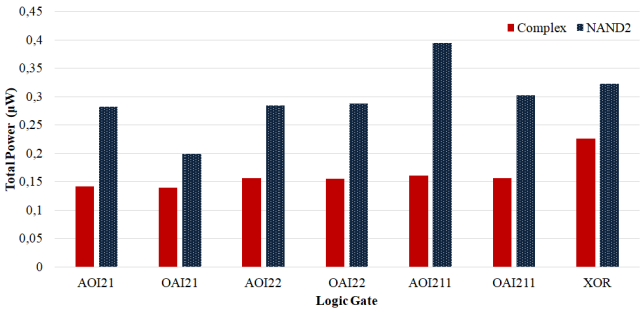


Fig. 4. Total power at nominal conditions.

TABLE III
PROCESS VARIABILITY IMPACT ON LAYOUT

Logic Function	Metric	Complex		Multi-level	
		μ	σ	μ	σ
AOI21	Delay (ps)	15.87	3.24	27.69	2.84
	Power (nW)	142.03	5.83	283.03	10.62
OAI21	Delay (ps)	15.84	3.25	23.84	2.54
	Power (nW)	140.26	5.60	200.46	8.052
AOI22	Delay (ps)	17.99	3.60	26.16	2.58
	Power (nW)	156.17	6.34	285.35	10.52
OAI22	Delay (ps)	17.77	3.61	24.14	2.55
	Power (nW)	155.62	6.18	289.69	11.81
AOI211	Delay (ps)	26.04	5.53	43.08	4.17
	Power (nW)	161.39	6.76	395.98	15.22
OAI211	Delay (ps)	17.92	2.98	23.75	2.52
	Power (nW)	157.34	6.53	303.39	12.49
XOR	Delay (ps)	19.60	3.13	25.55	2.69
	Power (nW)	222.52	9.34	325.33	13.19

becoming the most stable cell of the work. Power deviation is equivalent for complex and NAND2 topologies for all analyzed cells, as can be seen in Fig. 6. At 7nm layout, delay deviation shows to be about five times more relevant than power deviation for complex cells, and about 2.5 times superior for multi-level arrangements.

C. Radiation Effects

Table IV presents the fault analysis considering the total faults inserted, the masked/detected faults and the fault masking (FM). Multi-level topologies have a higher number of faults inserted, especially for the 4-input functions, due to the high number of internal nodes in these layouts

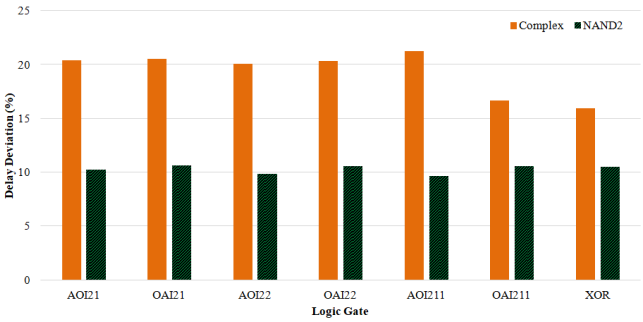


Fig. 5. Delay deviation due to process variability.

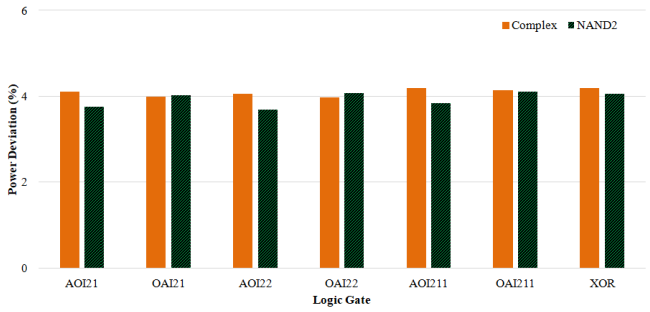


Fig. 6. Power deviation due to process variability.

that must be considered during fault evaluation. Also, multi-level arrangement masked a considerable number of faults, improving the fault masking (lower FM) and presenting better SET robustness than Complex topologies. Fig.7 shows the comparative fault masking of the two explored topologies. OAI22 cell presents the best improvement on SET robustness with NAND2 topology adoption, reducing by about 28% the fault masking. NAND2 topology improves by up to 50% the SET impact for the evaluated layouts.

TABLE IV
FAULT ANALYSIS

Logic Function	Topology	Fault Analysis			
		Inserted	Detected	Masked	FM
AOI21	Complex	24	13	11	0.54
	Multi-level	64	27	37	0.42
OAI21	Complex	24	13	11	0.54
	Multi-level	64	19	45	0.29
AOI22	Complex	64	40	24	0.62
	Multi-level	128	54	74	0.42
OAI22	Complex	64	36	28	0.56
	Multi-level	224	63	161	0.28
AOI211	Complex	64	26	38	0.41
	Multi-level	224	78	146	0.35
OAI211	Complex	64	25	39	0.39
	Multi-level	192	58	134	0.30
XOR	Complex	20	12	8	0.60
	Multi-level	40	19	21	0.47

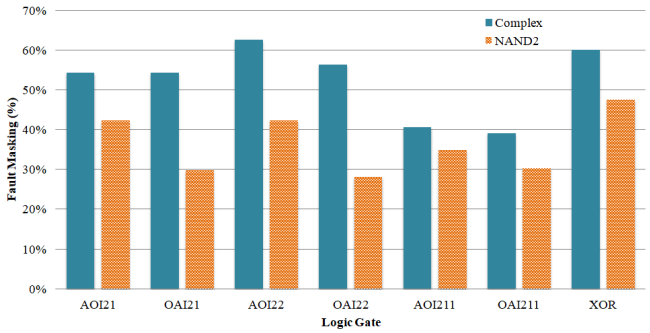


Fig. 7. Fault Masking evaluation.

IV. CONCLUSIONS

This work explored the multi-level design of a set of functions to evaluate the advantages of this strategy to mitigate the process variability and radiation effects using ASAP7 PDK. Post-layout evaluation is relevant because make possible to consider the parasitic effects and others impacts due to design rules that can compromise the variability and radiation sensibility. At nominal conditions, the complex topology presents the best results. Under the effects of SETs or process variability, multi-level arrangements are the best option. Despite the area impact, multi-level topology mitigate at least 30% of the impact on delay due to process variability, reaching more than 50% of improvement compared to complex gates. AOI211 cell presented the lowest sensitivity to process variability. Also, multi-level topology improves by up to 50% the fault masking evaluation from SET effects for these layouts. Among the seven functions studied, the OAI22 cell is the least sensitive to SETs.

ACKNOWLEDGMENT

The authors would like to thank to CNPQ, CAPES, FAPERGS and PGMICRO for supporting partially this project.

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