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SOFT ERRORS IN COMMERCIAL INTEGRATED CIRCUITS

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The once-ephemeral soft error has recently caused considerable concern for manufacturers of advanced silicon technology as this phenomenon now has the potential for inducing the highest failure rate of all other reliability mechanisms combined. We briefly review the three radiation mechanisms responsible for causing soft errors in commercial electronics and the basic physical mechanism by which ionizing radiation can produce a soft error. We then focus on the soft error sensitivity trends in commercial DRAM, SRAM, and peripheral logic devices as a function of technology scaling and discuss some of the solutions used for mitigating the impact of soft errors in high reliability systems.

Keywords: soft error rate, radiation effects, single event upset

1. Introduction

Radiation effects have long been one of the most serious issues in spacecraft and aviation electronics[1,2]. The harsh high-energy particle fluxes experienced in orbital and flight altitude environments demand that the electronics be shielded, have redundant components, and that they be radiation hardened, thereby increasing their cost and reducing their performance. In the more benign terrestrial environment where most commercial microelectronics are used, the most common radiation-induced effect is the soft error*. In stark contrast to the many "hard" reliability failure mechanisms such as gate oxide breakdown, metal interconnect stress- and electro-migration, transistor negative bias temperature instability, etc., soft errors corrupt the data state of devices while not permanently damaging the devices themselves. So when new data is rewritten into the device, it operates correctly. As the dimensions and operating voltages of commercial integrated circuits (ICs) are reduced to satisfy the ever-increasing demand for higher density (functionality) and lower power (portability), their sensitivity to radiation has increased dramatically. Soft errors have recently become a huge concern in advanced commercial ICs because they can induce a product failure rate that is higher than all the other reliability mechanisms combined. For example, in a qualified manufacturing silicon process technology the typical failure rate for the hard reliability mechanisms

* Soft errors include a plethora of different failure modes. Single-event upsets (SEUs) are errors in which an individual memory or register component is corrupted by radiation directly. Single-event transients (SETs) are radiation-induced transients in combinatorial logic that when propagated and latched create SEUs. Single-event functional interrupts (SEFIs) occur when an SEU or latched SET corrupts critical data causing a system interrupt or lock-up. Lastly, non-destructive single-event latch-up (SEL) occurs when a latch-up is induced by an ionization event but the current is limited by the circuit parametrics so that it is not permanently damaged. Of course the circuit must be powered-down to release the latch-up condition and this in itself causes system lock-ups. In most microelectronics in terrestrial applications SEUs are the predominant soft error failure mechanism.

collectively is 10-100 FIT while the soft error rate (SER) can easily exceed 50,000 FIT (one FIT or Failure-in-Time is equivalent to one failure in a billion device hours). For single-chip consumer systems even an SER of 50kFIT is usually not problematic, but for high-reliability systems composed of multi-chip assemblies such a failure rate is intolerable.

In the last two decades three radiation mechanisms have been identified to cause soft errors in ICs at terrestrial altitudes[3]. In the late 1970s, alpha particles emitted from the natural radioactive decay of uranium, thorium, and daughter isotopes present as impurities in packaging materials were found to be the dominant cause of SER in DRAMs[4]. During the same period, it was demonstrated that the ionizing reaction products created from the interaction of cosmic high-energy neutrons with device materials could cause soft errors[5], and by the mid-1990s it had been established that high-energy cosmic radiation was the dominant source of soft errors in DRAM devices[6-8]. More recently a third mechanism was identified– soft errors from low-energy cosmic neutron interactions with ^{10}B in device materials[9], specifically in the borophosphosilicate glasses (BPSG)[10] used extensively as insulating layers in integrated circuits. This mechanism has been shown to be the dominant SER mechanism in 0.25 and 0.18 um CMOS SRAMs fabricated with BPSG.[11,12]

Significant improvements in the SER performance of microelectronics can be obtained by eliminating or mitigating the sources of radiation. To reduce alpha emissions in the final packaged IC, high purity materials and processes are employed. In products requiring high reliability, uranium and thorium impurities have been reduced below one hundred parts per trillion (in the case of eutectic lead-tin solder this is not sufficient since radioactive Pb isotopes remain that cause the in-growth of high activity daughter products months after the sample is produced)[13]. Going from conventional IC packaging to ultra-low alpha packaging materials the alpha emission can be reduced from 5-10 alphas/cm^2-hr to less than 0.001 alphas/cm^2-hr. Another method used to reduce the impact of alpha particles is exclusion zones, where materials with high alpha emission (such as solder bumps) are kept physically separated from sensitive circuit components[14]. Thick (5-10 μm) polyimide coatings are often deposited on the IC prior to its encapsulation to reduce package alpha emission[15]. To reduce SER induced by the ^{10}B activation by low-energy neutrons, BPSG is replaced by other insulators which do not contain boron, and any processes using boron precursors are scrutinized for ^{10}B content prior to introducing them into the manufacturing process. When all these mitigation techniques are used, the SER of the IC is reduced significantly, but ultimately limited by cosmic high-energy neutron interactions that cannot be easily shielded.

The mechanism by which a soft error is produced occurs after an energetic ionizing particle has been brought to rest in the silicon near sensitive device nodes (floating or weakly-driven reverse-biased junctions). Along the path it traverses, the charged particle produces a dense radial distribution of electron-hole pairs as illustrated in figure 1a (an n+/p junction is shown, but a similar situation occurs for p+/n junctions except that the collected charge is holes instead of electrons). If the resultant ionization track traverses the depletion region, carriers are rapidly (over several picoseconds) collected by the electric field, thereby compensating the charge stored in the junction (reducing the voltage on the node permanently if the node is floating and temporarily if the node is driven). Outside the depletion region the non-equilibrium charge distribution induces a temporary funnel-shaped potential distortion[16] along the trajectory of the event, further enhancing charge collection by

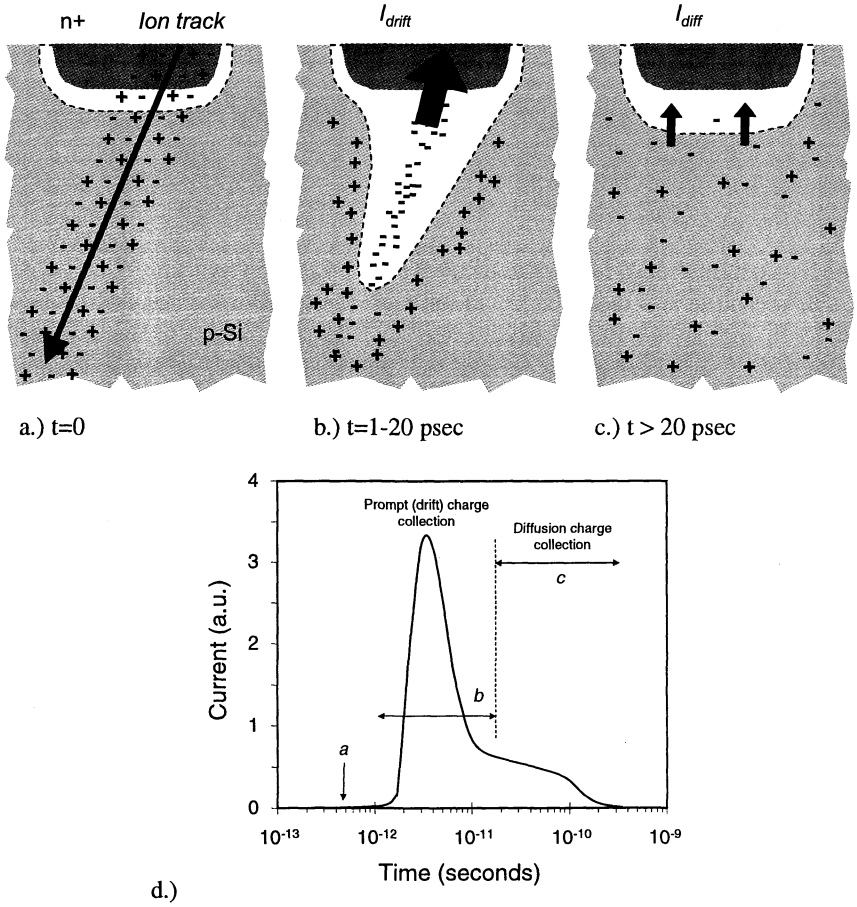

Fig. 1 Schematic representation of charge collection in a silicon junction immediately after an ion strike a.), during prompt (drift) collection (b.), and during diffusion collection (c.). A graph of the junction current induced as a function of time is shown in d.).

drift (figure 1b). This "prompt" collection phase is typically completed within tens of picoseconds, and as the funnel collapses (as the potential distortion relaxes), diffusion then dominates the collection process (figure 1c) until all excess carriers have been collected, recombined, or diffused away from the junction area (~ nanoseconds). The transient charge collected from the radiation event produces a current pulse at the junction as illustrated in figure 1d – note the distinctive shape of the curve defined by the different collection mechanisms. In general, the farther away from the junction that the event occurs, particularly if the track does not cross the junction, the less charge is collected, and the less likely it is that the event will cause a soft error. For modern submicron CMOS technologies, the current transient typically lasts 200 psecs with the bulk of the charge collection occurring within 2-3 microns of the junction region[17]. Of course these time constants depend strongly on the type of ion, its initial energy, and the specifics of the process technology.

If enough of the charge is collected by a node the data state of the circuit may be compromised. The collected charge (Q_{coll}) is a function of the ionizing particle's energy and trajectory, silicon substrate structure and doping, and the local electric field. If Q_{coll} is greater than the critical charge (Q_{crit}) then a soft error occurs. Q_{crit} is defined as[18]:

$$Q_{crit} = C_n \cdot V_n + I_{rstr} \cdot t_{sw} \qquad \text{(eq. 1)}$$

where C_n and V_n are the node capacitance and voltage, and I_{rstr} is the restoring current provided by feedback and t_{sw} is the time required for the circuit to switch to its opposing data state. The second term in equation 1 will obviously be zero for circuits such as dynamic random access memories (DRAM) where there are no external means to maintain the data state. For circuits which have some form of feedback, such as static random access memory (SRAM), flip-flops, or latches, the second term will be non-zero and represents the additional charge provided by the current feedback driving the node – if enough charge is provided before the memory bit's characteristic switching time, then Q_{crit} will be greater than Q_{coll} and a soft error is avoided. Unfortunately in high-speed, low-power SRAM designs, I_{rstr} and t_{sw} are minimized so this restoring term is often negligible.

Several process technologies can be used to improve SER performance either by reducing Q_{coll} and/or increasing Q_{crit}. One common approach is the use of additional well isolation (triple-well and guard-ring structures) which reduce the amount of charge collected by creating potential barriers that limit the efficiency of the funneling effect and reduce the likelihood of parasitic bipolar collection paths[19]. While these isolation methods can improve SER they are expensive because they require additional processing steps (masking and implant) and in the case of guard rings, additional chip area. In deep-submicron technologies where most of the charge collection is reduced to within a micron or two of the junction, triple well-isolation loses its effectiveness. Another popular approach is to replace bulk silicon with silicon-on-insulator (SOI) substrate material. Because the active device volume is greatly reduced (due to the thin silicon device layer on the oxide layer) direct charge collection is significantly reduced in SOI devices[20] and initially drastic reductions in SER were expected. Ultimately though, parasitic bipolar action and/or charge multiplication enhances floating body effects in SOI technologies limiting the SER performance from the same as to about 2x better than bulk[21]. However, recent work with fully depleted SOI substrates is more encouraging and shows a 10x reduction in SER over conventional bulk devices[22]. Unfortunately SOI substrates are more expensive than conventional bulk substrates. For this reason, in high reliability commercial products, design techniques based on adding redundant circuitry and/or software coding methods are often favored to provide much more significant reductions in SER.

2. Scaling trends for memory devices

To create the functionality provided by today's electronic systems and appliances several distinct components must be integrated together. At the core of each system is a microprocessor or digital signal processor with large embedded memories (usually SRAM) interconnected with sequential logic. In larger systems, discrete external main memory

(usually DRAM) is also used. Finally, all systems have some analog or digital input/output components to allow the device to respond and interact with the user and the outside world. As we shall see, the SER performance of these various components is affected differently by technology scaling.

It is somewhat ironic that soft errors were first discovered to be a problem in DRAM because, after many generations, it is currently one of the more robust electronic devices. Originally though, as DRAM technologies were scaled (in the late 1980s) DRAM SER was becoming a major problem because the planar capacitor cells that stored the signal charge in large reversed-biased area junctions were becoming more and more sensitive to ionizing radiation as they were scaled down in size (Q_{coll} was not shrinking as fast as Q_{crit} so SER increased). Interestingly, charge coupled devices (CCDs) and CMOS image sensors that are the mainstay of the digital camera industry get their high sensitivity to photon-induced charge by using large two-dimensional arrays of junctions that float during "exposure" similar to old DRAM designs. To address the DRAM soft error sensitivity issue and increase the packing density, manufacturers developed cell designs in which the large storage junction was replaced by a minimal storage contact (source-drain contact of the pass gate transistor used to "write" or "read" charge from the storage cell) connected to a three-dimensional (3-D) capacitor cell. The move to 3-D capacitor cells greatly reduced DRAM SER because the Q_{crit} of the cell was increased significantly while its charge collection efficiency was reduced with the sizable reductions in junction area[23]. In scaling from 1 Mbit (this was the first DRAM node to migrate to 3D cell designs) to 1 Gbit technology, the DRAM bit SER (solid diamonds) has been reduced by nearly five times per generation as illustrated in figure 2. This continuous

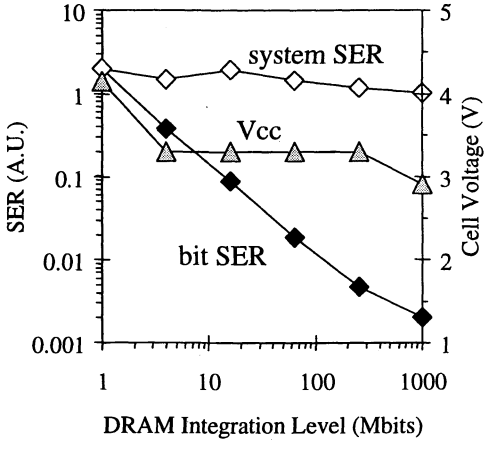

Fig. 2. DRAM bit (solid diamonds) and system SER (open diamonds) and operating voltage (gray triangles) as a function of technology scaling.

reduction in DRAM bit SER is also related to the relatively gradual (compared to logic devices) voltage scaling (gray triangles). Despite the DRAM bit SER having been reduced by nearly 1000x over six generations, the DRAM system SER (open diamonds) has remained essentially unchanged because system memory requirements have increased the memory density (bits/system) almost as fast as the SER reduction provided by technology scaling.

Therefore commercial DRAM system reliability has remained roughly constant over many generations. With DRAM technology scaling, operating frequencies have increased. At frequencies below 50Mhz DRAM SER is dominated by cell hits, but as frequencies are increased, the probability of sense-amplifier and bit-line hits increases since there are more sensing operations in a given time period during which the bit-line is floating (sensitive to soft errors) for a larger percentage of the DRAM cycle time. Therefore, as DRAM is scaled to operate at higher speeds the SER is expected to increase in proportion to the increases in DRAM operating frequencies.

In contrast to early DRAM, SRAM was once far more robust against soft errors because of its higher operating voltage and the fact that data was stored as an active state in the bi-stable circuit made up of two large cross-coupled inverters, each strongly driving the other to keep the SRAM bit in its programmed state. According to equation 1 shown earlier, Q_{crit} for the SRAM cell is defined by the charge on the node capacitance and a second term related to the size of the transistor (its current drive capability) keeping the node voltage at the proper value – the bigger the transistor, the higher Q_{coll} must be for the node to reach the switching threshold. With scaling, the SRAM junction area has been deliberately minimized to reduce capacitance, leakage, and cell area, while simultaneously the SRAM operating voltage has been aggressively scaled down to minimize power. Initially, with each successive SRAM generation, reductions in cell collection efficiency due to shrinking cell depletion volume were swamped out by large reductions in operating voltage and reductions in node capacitance. So SRAM bit SER initially increased with each successive generation as illustrated in figure 3a. However, as feature sizes have been reduced below 0.35 μm the SRAM bit SER has

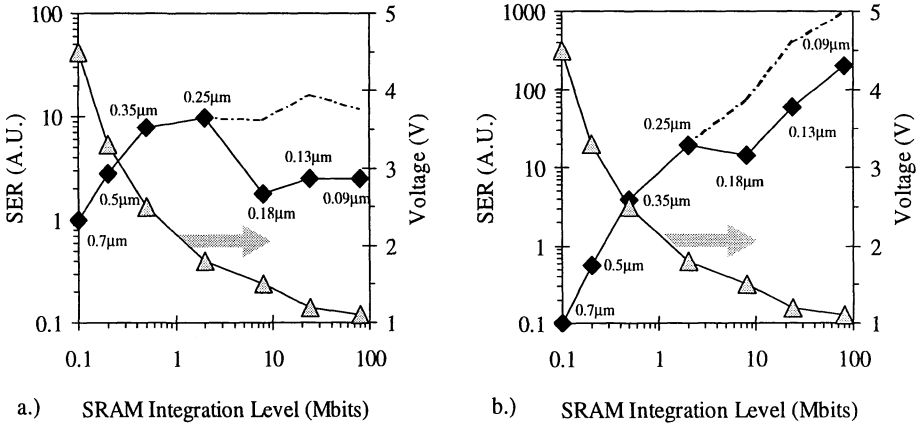

Fig. 3. SRAM voltage (gray triangles), SRAM bit SER (a.) and SRAM system SER (b.) as a function of technology scaling. Dashed line represents SER for SRAM processes still employing BPSG in their production process.

saturated. This saturation is due to the fact that further reduction in operating voltage (gray triangles) is limited by the threshold or turn-on voltage of the transistors, reductions in junction collection efficiency, and increased charge sharing with neighboring nodes. As can be seen by the dashed line, SRAM fabricated with BPSG will have an SER which is about eight times higher than that of SRAMs with no BPSG. Ultimately, as with DRAM, scaling also

implies increased density, so saturation in SRAM bit SER does not translate to saturation in the SRAM system SER as is seen in figure 3b. The exponential growth in the amount of embedded SRAM in electronics has led the SRAM system SER to increase with each generation, with no end in sight. This trend is of great concern to chip manufacturers since SRAM constitutes a large part of all advanced integrated circuits today. As SRAM operating frequencies increase, the probability that soft errors will occur during reading/sensing operations increases (since the SRAM cell Q_{crit} is lowered during sensing[24]). In a manner similar to DRAM, above a certain operating frequency, it is expected that the SRAM SER will increase with increasing frequency.

By far the most effective method of dealing with soft errors in memory is error detection and/or correction. In its simplest form, error detection consists of adding a single bit to store the parity (odd or even) of each data word (regardless of word-length). Whenever data is retrieved, a check is run comparing the parity of the stored data to its parity bit. If a single error has occurred the check will reveal that the parity of the data does not match the parity bit. Thus the parity system allows for the detection of a soft error for a minimal cost in terms of circuit complexity and memory width (only a single bit is added to each memory word and the parity checker utilizes minimal additional chip area). The two disadvantages of this system is that the detected error cannot be corrected since the parity cannot localize the error, and if an even number of errors has occurred, the parity check will not register that any error has occurred, since the parity bit will match the parity of the corrupted data in the word (even + first error => odd: odd plus second error => even). The next commonly employed solution is to implement error detection and correction (EDAC) or error correction circuits (ECC)[25]. EDAC/ECC requires that more bits be assigned to each data word. For a 64-bit wide memory, usually eight correction bits are used. These eight correction bits allow up to two errors to be detected and a single error to be corrected (more correction bits can be added to correct for more than a single error). Since most soft error events are single bit errors (it is rare that multiple bits in the same data word are effected since in most memory designs physically adjacent bits do NOT make up the same memory word) EDAC/ECC protection will provide a significant reduction in failure rates. EDAC/ECC incurs a higher cost in terms of design complexity and the additional memory required. Since time is required to check parity and correct for errors, error detection and/or correction schemes trade memory bandwidth for reliability performance. In high-reliability applications where EDAC/ECC has been implemented, the system SER is no longer dominated by memory.

3. Scaling trend for peripheral logic devices

Peripheral logic is usually predominantly made up of sequential logic components. Sequential logic elements include latches and flip-flops that provide storage to hold system event signals and to buffer data before it goes in or out of the chip, and combinatorial logic components whose output is based on a logical relation to the inputs (AND, OR, XOR, etc.) with no capability for retention. The system impact of errors in sequential logic is much harder to quantify since the period of vulnerability (when the devices are sensitive to soft error effects) varies widely depending on the circuit design, frequency of operation, and algorithm.[26] Latches are similar to the SRAM cell in that they use a cross-coupled inverter

circuit. However, they tend to be more robust because they are usually designed with larger and/or more transistors (higher Qcrit), that more easily compensate for spurious charge collected during radiation events. Flip-flops are even more robust as they are constructed of two stages, again with larger and more transistors. As illustrated in figure 4, the SER of sequential logic is several orders of magnitude lower than that of SRAM cells. However,

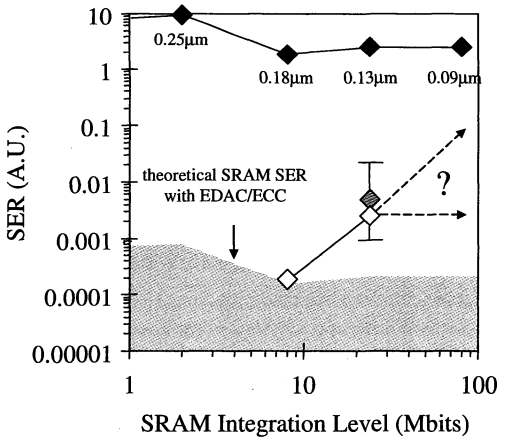

Fig. 4. Simulated (open diamonds) and experimental data (gray diamond with error bars) for flip-flop/latch SER and SRAM SER (solid diamonds) as a function of technology scaling. Note that the shaded region represents the SRAM SER when EDAC/ECC is used.

from the 0.18 to the 0.13 μm node, the logic SER has increased by 20x. Thus sequential logic SER may be increasing with technology scaling. Logic SER is particularly a concern in high reliability systems where the memory has been protected from soft errors with parity or EDAC/ECC. In such systems the peripheral logic failure rate will limit the impact of memory error correction and will ultimately limit the reliability of the product. It should be noted that there is another soft failure mode related to combinatorial logic. If enough radiation-induced charge is collected so that the voltage on the input of a combinatorial gate exceeds the threshold between a "one" and "zero", the event will generate a SET or transient in the output of the device. Since the charge collection occurs on a short timescale, the "glitch" is propagated to the output of the device only as long as the event itself. A soft error is induced by a SET only if the glitch is propagated to the input of a memory element at the same time that the element is being latched or written to. With older technologies this was not a concern since the glitch was shorter than the response of the logic and thus SETs were not readily propagated through the circuit. With the shorter propagation delays of modern technologies, the SET will become a larger component of the observed logic SER.

To mitigate SER in sequential logic involves the use of redundant logic paths[27] and/or time redundancy[28]. In the circuit redundancy approach, three identical logic paths feed into a majority voting circuit in which the two matching inputs (out of three) are assumed to represent the correct data (since the probability of a soft error in two of the circuits is low) and thus this "correct" data is propagated to the next stage. In the temporal approach a single circuit sends the data through the logic pathway multiple times and the results of the multiple

passes are then compared to establish the correct result. The most robust method combines the spatial and temporal redundancy scheme so that the same signal is passed down three identical circuits but out of phase – thus the probability that a single event will upset more than one signal with different delays is significantly reduced (assuming the delays are longer than the current transient). These methods unfortunately require three times the chip area and/or a significant reduction in system speed. Since correcting for logic SER/SET is extremely expensive from a performance and area standpoint, simulations to identify the critical logic paths are needed so that only the most critical paths are hardened.

4. Conclusion

We have shown how transient charge generated when an energetic ion is brought to rest in the silicon substrate can lead to soft errors in semiconductor devices. At terrestrial altitudes three mechanisms are responsible for soft errors: alpha particles emitted from trace radioactive impurities in the device materials, the reaction of low-energy cosmic neutrons with high concentrations of ^{10}B in the device, and the reaction of high-energy cosmic neutrons with silicon and other device materials. With proper screening and choice of manufacturing processes, the SER induced by alpha particles and ^{10}B reaction products can be reduced to the point where they are a small fraction of the total SER – dominated by cosmic high-energy neutrons that cannot easily be shielded. The soft error sensitivity of various memory and logic components has been considered as these components are scaled to smaller dimensions, higher integration densities, and lower operating voltages. While shrinking junction sizes have led to reductions in direct charge collection and enhanced charge sharing with neighboring cells (thereby reducing the charge collected by any one device), cell voltage and capacitance reductions have decreased the critical charge as well. The impact of these changes has been dependent on the type of technology. DRAM system SER has been relatively independent of technology scaling, because reductions in cell sensitivity have been matched by increased memory density (more bits/system). In contrast, while SRAM system SER used to be minimal, it has increased rapidly with each new technology node. The SER of both memory types is expected to increase with increasing operating frequencies. Finally, we have shown how sequential logic elements, once insensitive to SER, are now becoming much more sensitive - indeed, in high reliability systems where memory error correction is employed, the failure rate is limited by SER and latched SETs in the sequential logic.

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