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# Towards high-sensitive built-in current sensors enabling detection of radiation-induced soft errors

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ABSTRACT

Soft error resilience is an increasingly important requirement of integrated circuits realized in CMOS nanometer technologies. Among the several approaches, Bulk Built-in Current Sensors (BBICS) offer a promising solution able to detect particle strikes immediately after its occurrence. Principal challenges for its wide application in common designs are area costs and robustness, both directly related to the sensor's sensitivity. Following this requirement, this work presents strategies enabling the design of high-sensitive BBICS. In detail, we are proposing three approaches based on gate voltage control, body biasing, and stack forcing that can be integrated in all *state-of-the-art* BBICS architectures. In order to verify the feasibility of this approaches, the proposed techniques have been integrated in a modular BBICS realized in a commercial 65 nm technology. Simulation results indicate an increase of the detection sensitivity by up to factor 6, leading to 17% area overhead, response times around 1 ns, a negligible power penalty, and high robustness against wide variations of temperature and process parameters.



## 1. Introduction

CMOS remains the dominating technology for integrated circuits, mainly due to its miniaturization capability and high integrability. However, the continuously reduction of technology sizes results in designs that are susceptible to several fault sources like parameter variations [1], oxide breakdown [2], and radiation [3]. In case of the latter, energetic particles inject electrical charge into sensitive regions of the semiconductor devices, creating transient currents that can result in soft errors. For years, researches on radiation-induced soft errors concentrated mainly on memories and application intended for avionics and aerospace environment. However, as current technologies reached nanometer scale, soft error resilience is also required for applications on ground level as well as the combinational parts of the circuits. Several concurrent error detection and/or correction techniques have been presented to circumvent the effects of soft errors. This includes the application of multiple clocking schemes [4], checker-based arithmetic units [5], and selective redundancy [6]. In contrast to gate and system level techniques, Bulk Built-in Current Sensors (BBICS) are a promising approach on transistor level, which enables the detection of radiation-induced particle strikes immediately after its occurrence [7–10]. BBICS offer fast error detection and low cost in terms of power. On the downside, BBICS design is a challenging task, as these sensors tend to be prone to parameter and temperature variations and/or require a considerable amount of area [11–13]. Previous works introduced several different kinds of BBICS architectures, including the single BBICS [14], the modular BBICS [15,16], the dynamic BBICS [17], a low-leakage BBICS [18], as well as an architecture based on transistors with different threshold voltages [19]. Despite the diversity of BBICS architectures, there is still a demand for further improvements. Principal requirements are reduction of area costs and robustness.

This work presents several new concepts leading to considerable enhanced sensitivity, and thus, to notably improved area costs, response time, and robustness. The proposed techniques can be employed by all reported BBICS architectures turning the results of this work into an important step towards the consolidation of the BBICS approach.

The rest of the paper is organized as follows. Section 2 introduces basic information and the BBICS method, while Section 3 details the new strategies. Section 4 is related to simulation results. Finally, Section 5 draws the conclusion.

## 2. Preliminaries

This section discusses the generation of transient faults induced by radiation on integrated circuits and introduces the BBICS approach.

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### 2.1. Transient faults and soft errors

Unintentional transient signal variations in integrated circuits are defined as transient faults. A transient fault can turn into a soft error when it propagates to the input of a sampling element or affects directly a node within the sampling element, for example a latch or flip-flop.

There are several sources for transient faults like cross-talk, ground bounce, or radiation-induced energetic particles [20]. The latter are critical for reversed-biased p-n junctions, as it is the case for drain or source regions of transistors in cut-off state. In the event of a particle strike, the electron-hole pair track formed in the path of the energetic particle affects the electrical field in the depletion region to shortly adopt the shape of a funnel towards the substrate [21]. This starts the so-called carrier collection that is observed as transient voltage on the affected node. The subsequent phase of carrier collection is defined by a slower phenomenon in which carriers are conducted through the depletion region due to diffusion. The corresponding current pulse is traditionally modeled by a double-exponential function $I_{coll}$ by following equation [22]:

$$I_{coll}(t) = \frac{Q_{coll}}{t_f - t_r}\left(e^{\frac{-t}{\tau_f}} - e^{\frac{-t}{\tau_r}}\right) \quad (1)$$

Hereby, $Q_{coll}$ is the total collected charge, and $t_r$ and $t_f$ represent the time constants for the funnel collection and he second phase of carrier collection.

### 2.2. BBICS detecting transient faults

The idea behind BBICS is to monitor anomalous currents in the transistor bulk in case of a particle strike [7,12]. Consequently, it enables the detection of radiation-induced currents that might lead to soft errors.

The principal idea of BBICS shall be introduced with the aid of the modular BBICS (mBBICS) reported in [15]. It consists of functional blocks named as head and tail (see Fig. 1). The head circuits are connected to the bulk of the monitored devices, *i.e.*, the Block Under Test (BUT) in Fig. 1, and act as sensing elements. The outputs of several heads (wire $head_{NMOS}$) are latched by the tail circuit. As most of *state-of-the-art* BBICS, the mBBICS approach comprises a NMOS type able to detect transient faults in NMOS devices and a complementary PMOS version.

Fig. 1 illustrates an NMOS-mBBICS in which the gate of transistor Nh1 is connected to VDD and the drain to the NMOS bulk of the monitored transistors in the BUT. In normal operation, the drain of Nh1 acts as a virtual GND, while the head output (*i.e.*, drain of Nh2) is at VDD level. In case of a particle strike, the fault current in the bulk is conducted through Nh1, resulting in a voltage drop over Nh1 that increases the gate voltage of Nh2. If this voltage exceeds the threshold voltage $v_{th,Nh2}$ of Nh2, this device is switched on and the signal $head_{NMOS}$ is pulled down, leading the tail circuit to latch this signal and set an error flag. The circuit remains in this logic state until the reset transistor Pt3 is activated, turning the sensor ready for another detection [15].

The PMOS-mBBICS, which permits the detection of transient faults in PMOS devices, has a complementary behavior and structure and is omitted herein for the sake of simplicity.

The sensitivity of a BBICS relates to the amplitude of a radiation-induced bulk current that can be detected. The amplitude of this current correlates with the collected charge and the capacitive load of the sensor's input [23]. The latter is directly related to the number of monitored devices. Hence, the higher the BBICS's sensitivity the greater the number of devices a single BBICS can monitor and, consequently, the lower the area penalty [24].

Note that the processing of the generated error flag in case of a transient fault is realized on higher abstraction layers and is not discussed in this work. Further information can be found in [25–29].

## 3. Strategies for improving BBICS

This section presents the strategies for improving the sensitivity of BBICS architectures, leading to enhanced response time, area costs, and robustness. All techniques are applied exemplarily for the mBBICS architecture. Nevertheless, we would like to emphasize the universality of the approaches for different types of BBICS architectures.

For the sake of simplicity, the discussions relate solely to the NMOS version, but it can be carried over directly to the complementary PMOS type.

### 3.1. Adjustable gate voltage on sensing transistor

A common element of BBICS architectures is the sensing device that converts the bulk current into a voltage signal [12,17,18,30]. In case of the mBBICS, transistor Nh1 is this element (see Fig. 1 and Section 2.2). At the onset of a particle strike and a resulting bulk current, the voltage drop at the drain of Nh1 must be sufficient to activate Nh2, and thus switching the signal $head_{NMOS}$. It is, therefore, desired that the current through Nh1 results into a high voltage drop over Nh1. On the other side, it has to be assured that the bulk voltage must be kept at GND level in fault-free operation mode. Previous BBICS [8,11,15,18] achieved these goals by using a transistor with small W/L ratio that operates in linear mode, *i.e.*, a gate-source voltage equal to VDD. Consequently, the sensor sensitivity can be calibrated by adjusting the gate length of

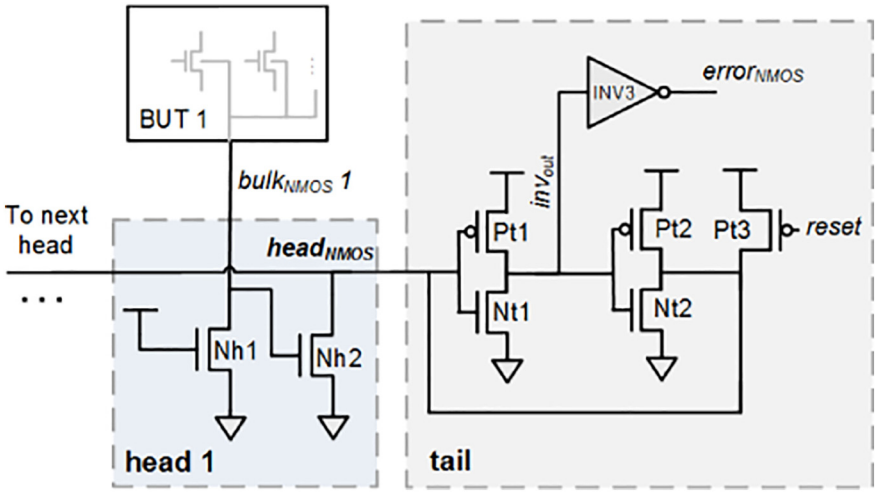


**Fig. 1.** mBBICS architecture (head + tail, NMOS type) able to detect transient faults in the monitored blocks defined as BUT.

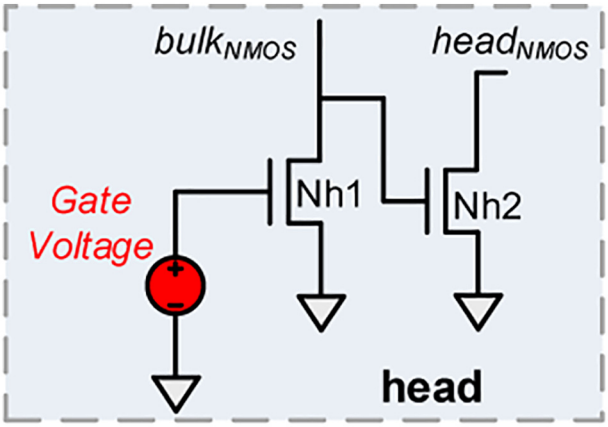


**Fig. 2.** Adjustable gate voltage applied on sensing transistor.

Nh1. This parameter is directly related to the channel resistance, and thus, the voltage drop over Nh1 in case of a fault current. However, this solution turns out to be costly in terms of area.

We propose the application of a minimum sized transistor and adjustable gate voltage as illustrated in Fig. 2. Here, the voltage drop over Nh1 is controlled by the gate-source voltage $V_{gs\_Nh1}$ of Nh1, which controls the channel resistance. This solution proved to be area efficient, since it permits the application of a transistor with minimum length and width. Moreover, it also enables sensitivity adjustments during runtime.

It is mandatory to assure that the bulk stays at GND level during normal operation in order to avoid variations of the threshold voltage of the monitored devices due to the body-effect [31]. Hence, it must be ensured that the chosen gate-source voltage allows the passing of noise and bulk leakage currents.

Further, during physical design of the chip, distribution of voltages with values below the supply voltage has to be considered. However, this is a common problem and has been tackled in several related work [32,33].

### 3.2. Threshold voltage modification via body-biasing

A further element of the sensing part of BBICS is the transistor that works as a trigger and whose gate input is connected to the bulk [8,11,15,18]. In the event of a particle strike, the voltage drop on the bulk caused by the bulk current that passes the sensing transistor activates the trigger device. In case of the mBBICS, the transistor Nh2 assumes this function (see Fig. 1 and Section 2.2). It is activated as soon as the bulk voltage crosses Nh2's threshold voltage $v_{th,Nh2}$. In order to achieve high sensitivity, it is desired to have a low value for $v_{th,Nh2}$.

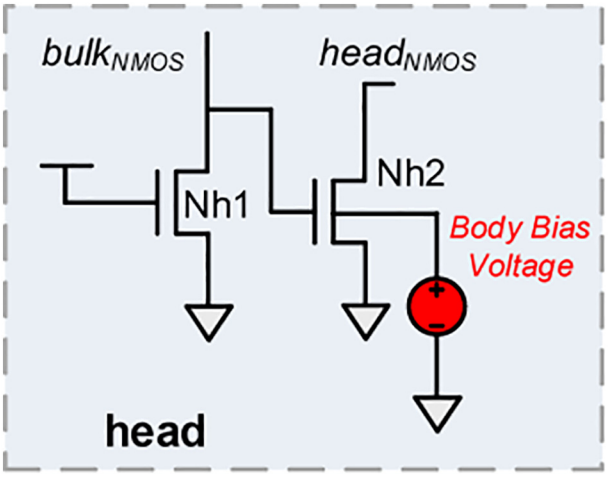


**Fig. 3.** Body-biasing of the trigger device Nh2.

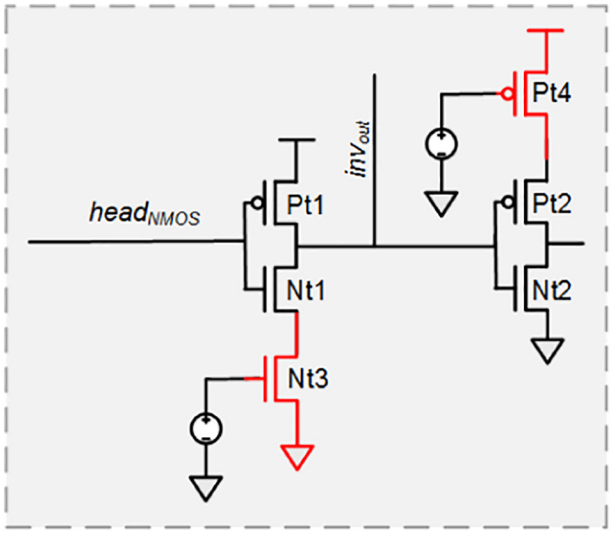


**Fig. 4.** Stack-forcing in the tail circuits.

The threshold voltage $v_{th}$ of a CMOS device can be modeled with [34]:

$$v_{th} = v_{\text{th0}} + \gamma a_1 V_{sb} - \eta a_2 V_{ds} \quad (2)$$

with $v_{th0}$ is the zero-bias threshold voltage, $\gamma$ is the body-bias coefficient, $a_1$ and $a_2$ label technology constants, $\eta$ corresponds to the Drain Induced Barrier Lowering (DIBL) coefficient, $V_{sb}$ labels the source-body voltage, and $V_{ds}$ is the drain-source voltage. From Eq. (2) follows that the threshold voltage also depends on the body voltage, which is known as the aforementioned body-effect [31]. We propose to increase the sensor's sensitivity by biasing the body of Nh2. Thereby, the body terminal is connected to a positive voltage source as illustrated in Fig. 3. Consequently, $V_{sb}$ turns negative leading to reduction of $v_{th\_Nh2}$.

The downside of this approach is an increasing sub-threshold leakage current $I_{sub}$ due to lower threshold voltage [34]. Also, in order to separate its bulk, Nh2 has to be placed in an isolated N-well, leading to higher area costs.

### 3.3. Stack-forcing

Most of the reported BBICS architectures apply feedback inverter structures to latch the signal that this generated *via* the sensing part [11,12,18]. Consequently, the performance of this structure is critical for the response time $t_{resp}$ of the sensor.

**Table 1**
Transistor sizes in nm for the applied mBBICS whereas the 1st number indicates the width and the 2nd the length.

| NMOS | | PMOS | |
|---|---|---|---|
| Name | Size | Name | Size |
| Nh1 | 135/65 | Ph1 | 135/65 |
| Nh2 | 810/65 | Ph2 | 945/65 |
| Pt1 | 540/65 | Pt1 | 135/65 |
| Nt1 | 135/65 | Nt1 | 675/65 |
| Nt3 | 135/325 | Pt3 | 135/650 |
| Pt2 | 135/65 | Pt2 | 135/65 |
| Nt2 | 135/260 | Nt2 | 135/65 |
| Pt4 | 135/1300 | Nt4 | 135/1300 |
| Pt3 | 270/65 | Nt3 | 200/65 |

**Table 2**
Voltage levels applied to the mBBICS circuits.

| NMOS | | PMOS | |
|---|---|---|---|
| Voltage | Value | Voltage | Value |
| $V_{gate\_Nh1}$ | 0 mV | $V_{gate\_Ph1}$ | 1.2 V |
| $V_{body\_Nh2}$ | 700 mV | $V_{body\_Ph2}$ | 500 mV |
| $V_{gate\_Pt4}$ | 700 mV | $V_{gate\_Pt3}$ | 500 mV |
| $V_{gate\_Nt3}$ | 500 mV | $V_{gate\_Nt4}$ | 400 mV |

In case of the mBBICS, the latching is executed in the tail circuits (see Fig. 1 and Section 2.2). Hence, in order to lower $t_{resp}$, the signal $inv_{out}$ must perform a fast state transition ($0 \rightarrow 1$) when a particle strike is detected. This way, both inverters INV1 and INV2 created by the transistors Nt1/Pt1 and Nt2/Pt2 should have switching voltages that favor a $0 \rightarrow 1$ transition of $inv_{out}$ as well as a $1 \rightarrow 0$ transition of $head_{NMOS}$ (see Fig. 1). Consequently, the channel resistances of Nt1 and Pt2 should be higher than their counterparts in the inverters. This goal can be achieved by decreasing the W/L ratio of both devices. However, this leads to higher input capacitances that, consequently, increase the capacitive load of both inverters resulting in higher $t_{resp}$.

We propose the addition of a stacked device in row with Nt1 and Pt2, respectively (see Fig. 4). The gate of both stacked transistors is connected to a voltage source, which assures that both devices operate in linear mode. This configuration leads to higher resistance of the pull-down path in INV1 and the pull-up paths in INV2 at constant input capacitances. Hereby, the increase of the path resistance follows on the one hand from the additional channel resistance due to the stacked device. Additionally, the increased potential of the source of Nt1 as well as Pt2 results in higher threshold voltages due to elevated source-body voltage $V_{sb}$, which increases the body-effect (see Eq. (2)).

## 4. Analysis

This section presents the simulation results of the proposed improvement strategies. All techniques have been applied exemplarily for the mBBICS architecture [15].

### 4.1. Test environment

The tests were based on a commercial 65 nm technology, with triple-well option and a supply voltage of 1.2 V. Chains of ten minimum sized inverters consisting of low threshold transistors ($L_{drawn}$ = 60 nm, $W_{drawn\_NMOS}$ = 200 nm, $W_{drawn\_PMOS}$ = 280 nm) implemented in a triple-well form the circuits to be monitored. The bulks of all devices of an inverter chain are connected to one head circuit. Hereby, NMOS devices are connected to a NMOS type mBBICS and PMOS devices to a PMOS type mBBICS. Moreover, several chains can be connected to a single head circuit. Each tail block is connected to six head blocks, following the results of previous works [15,16]. It should be noted that the sensors circuits are located outside the well regions of the monitored devices.

### 4.2. Sizing and voltage levels

Following discussions relate to the NMOS type mBBICS but can easily be adopted for the complementary PMOS type.

Table 1 lists the results of the sizing process, which was executed based on an iterative method similar to the one proposed in [35]. Notable outcomes of this step are the minimum sizes of Nh1 and the high W/L ratio of Nh2 in the head circuits (see Fig. 2). The first results from the proposed reduced gate voltage, while the latter follows from the requirement to have a high discharge current of the $head_{NMOS}$ in case of a detection.

Further, the devices in the tail circuits have been sized to favor a $0 \rightarrow 1$ transition of the signal $inv_{out}$ (Fig. 4). Consequently, Pt1 received a high W/L ratio, while Nt1 is minimum sized. Likewise, the devices Pt2/Nt2 should provide a fast $1 \rightarrow 0$ transition of $head_{NMOS}$, *i.e.*, Pt2 should be minimum sized and Nt2 should have a high W/L ratio. However, during our analysis we could observe that the leakage through Nt2 is critical as it discharges the node $head_{NMOS}$. Therefore, Nt2 is minimum sized, leading to lower leakage. Alternatively, high-$V_{th}$ devices could be applied [30]. Further, the devices utilized for stack-forcing, *i.e.*, Nt3 and Pt4 (see Fig. 4 and Section 3.3), are sized with very low W/L ratio leading to high channel resistances. Finally, the reset device Pt3 possesses a slightly increased width in order to restore the $head_{NMOS}$ to VDD in reasonable time. Also, the inverter INV3 is minimum sized.

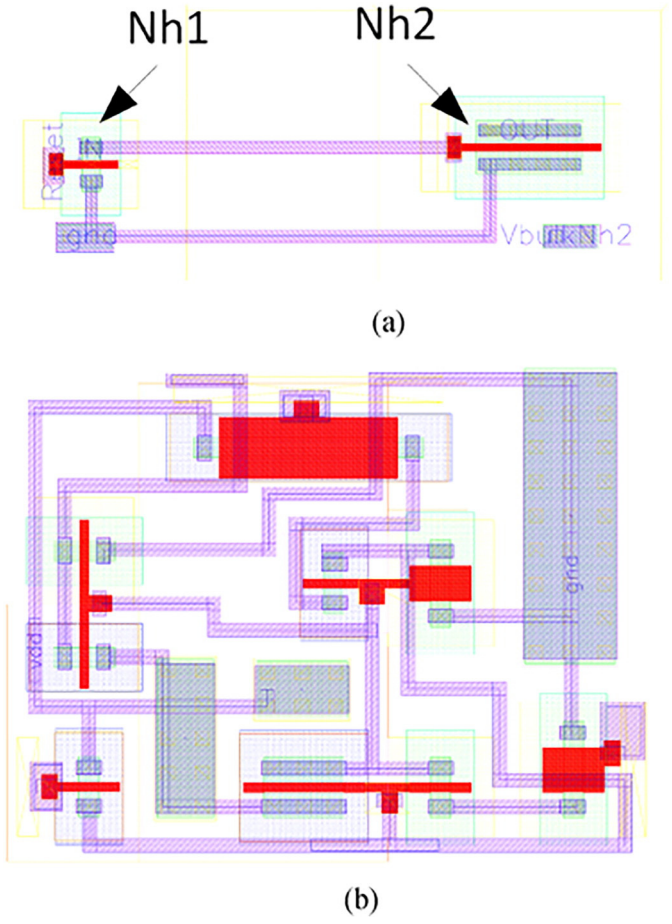


**Fig. 5.** Layouts of NMOS type mBBICS (a) head and (b) tail.

Table 2 lists the results of the determination of the voltage levels. It includes the gate voltages $V_{gate}$ of Nh1 in the head circuit (see Fig. 2) and the stacked transistors in the tails (see Fig. 4), as well as the voltage $V_{body\_Nh2}$ of the bulk terminal of Nh2 (see Fig. 3). With exception of $V_{gate\_Nh1}$ and $V_{gate\_Ph1}$ all voltages have been defined *via* an iterative method similar to the one proposed in [35].

As detailed in Sub-section 3.1, the gate voltage $V_{gate\_Nh1}$ of Nh1 should be as small as possible, but must be high enough to assure that the bulk remains at GND level. Therefore, the design was operated for 1 s in normal mode, *i.e.*, no strike current was applied, while the bulk was monitored. It could be determined that even for $V_{gate\_Nh1}$ = GND the bulk continuously staid at GND level.

**Table 3**
Layout sizes of mBBICS blocks and inverter (desigend in 65 nm technology).

| | NMOS | PMOS | INV |
|---|---|---|---|
| Head | 13.4 μm² | 5.9 μm² | – |
| Tail | 14.3 μm² | 15.7 μm² | – |
| Head + 6 tails | 94.7 μm² | 51.4 μm² | – |
| Cell area | – | – | 3.5 μm² |

**Table 4**
Number of monitored INVS vs. response time.

| NMOS ($Q_{coll}$ = 3.15 fC) | | PMOS ($Q_{coll}$ = 3.5 fC) | |
|---|---|---|---|
| N° INV | $t_{resp}$ [ns] | N° INV | $t_{resp}$ [ns] |
| 10 | 0.24 | 10 | 0.45 |
| 20 | 0.27 | 20 | 0.50 |
| 30 | 0.35 | 30 | 0.66 |
| 40 | 0.54 | 40 | 1.04 |
| 50 | 0.94 | 50 | 2.08 |
| 60 | 1.74 | 60 | 9.56 |
| 70 | 3.35 | | |
| 80 | 8.10 | | |

In order to determine the exact area costs for each sensor, all blocks have been implemented as layout (see Fig. 5). Table 3 lists the sizes of the head and tail blocks of each types, the area of a set of six heads and a tail and the cell area of a minimum sized inverter.

### 4.3. Characterization

The proposed sensor was submitted to simulations in order to analyze its detection sensitivity and response time for typical conditions, *i.e.*, temperature Temp = 25 °C and typical process corners. During the characterization, all chains were operated with independent input signals with a frequency of 1 GHz.

In a first attempt, we determined the minimum charge that leads to a transient fault at the output of the inverter chain. Therefore, a particle strike was simulated by a current pulse based on Eq. (1) with adjustable $Q_{coll}$ at the output node of the 9th inverter of the chain. All injected transient currents were defined with $t_r = 1$ ps and $t_f = 10$ ps to keep the typical shapes of transient faults: short rise time and longer fall time [36,37]. A transient fault was registered when the output voltage of the chain crossed VDD/2.

The estimated values are $Q_{coll} = 3.15$ fC for particle strikes in a NMOS device and $Q_{coll} = 3.5$ fC in case of a PMOS transistor. Next, the response time for increasing amount of monitored inverter chains per head was analyzed. This analysis considers that the voltage peak on the bulk, which activates the device Nh2 in case of a particle strike, depends on the amount of monitored transistors [23]. The simulations had been realized for NMOS and PMOS type mBBICS with the $Q_{coll}$ that results in a transient fault in the corresponding circuit.

The results shown in Table 3 indicate that the NMOS type mBBICS has a response time lower than 1 ns for up to 50 monitored inverters, while the PMOS type mBBICS achieves a similar response time for only 40 inverters. This difference can be explained by the greater width of the PMOS transistors ($W_{drawn\_NMOS}$ / $W_{drawn\_PMOS}$ = 200 nm / 280 nm), which leads to higher capacitive load on the bulk.

**Table 5**
Detection capability of the proposed BBICS. TF indicates the occurrence of a transient fault, DTCN indicates whether the error flag was set.

| | NMOS (50 INV) | | | PMOS (40 INV) | | |
|---|---|---|---|---|---|---|
| $Q_{coll}$ (fC) | TF | DTCN | $t_{resp}$ [ns] | TF | DTCN | $t_{resp}$ (ns) |
| 1.8 | No | ✗ | – | No | ✗ | – |
| 2.0 | No | ✓ | 6.2 | No | ✗ | – |
| 2.3 | No | ✓ | 3.14 | No | ✗ | – |
| 2.5 | No | ✓ | 2.03 | No | ✓ | 11.64 |
| 2.7 | No | ✓ | 1.44 | No | ✓ | 3.15 |
| 3 | No | ✓ | 1.09 | No | ✓ | 2.03 |
| 3.2 | **Yes** | ✓ | **0.86** | No | ✓ | 1.49 |
| 3.4 | **Yes** | ✓ | **0.71** | No | ✓ | 1.20 |
| 3.6 | **Yes** | ✓ | **0.60** | **Yes** | ✓ | **1.06** |
| 3.8 | **Yes** | ✓ | **0.53** | **Yes** | ✓ | **0.88** |
| 4.0 | **Yes** | ✓ | **0.47** | **Yes** | ✓ | **0.80** |
| 4.3 | **Yes** | ✓ | **0.43** | **Yes** | ✓ | **0.72** |
| 4.5 | **Yes** | ✓ | **0.40** | **Yes** | ✓ | **0.67** |

Bold entries highlight detected transition faults.

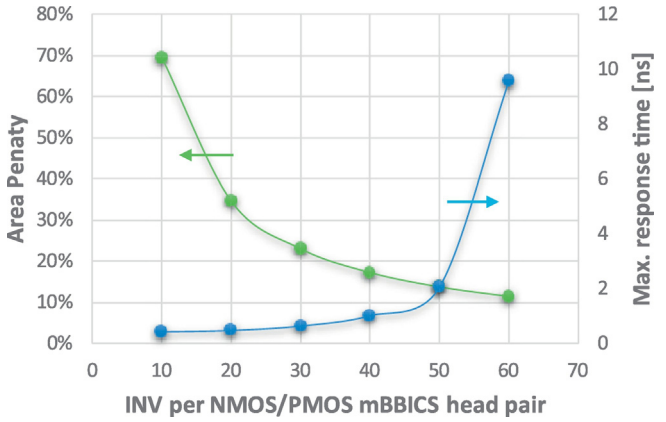


**Fig. 6.** Area penalty and maximum response time *versus* number of monitored inverters per NMOS/PMOS mBBICS pair (one tail per six heads).

Next, it was analyzed the sensitivity of the proposed mBBICS for different values of the collected charge $Q_{coll}$. Therefore, the NMOS type mBBICS was monitoring 50 inverters, while the PMOS version was connected to 40 inverters. As can be concluded from Table 4, an increase of $Q_{coll}$ leads to a reduction of the response time $t_{resp}$. This is an expected result, as larger collected charges result in higher bulk currents (see also Eq. (1)).

However, the results in Table 5 also reveal that the proposed mBBICS is more sensitive than required, *i.e.*, it indicates a transient fault even if the collected charge is not sufficient for changing the output signal of the inverter chain. Depending on high layer processing, this false detection might lead to a performance penalty of the integrated design. It is up to the designer to trade-off the sensitivity with the sensor's robustness against variations.

Fig. 6 depicts the area penalty and maximum response time in relation to the number of inverters monitored by a NMOS and PMOS type mBBICS pair. It had been considered that a tail connects to six heads [15]. The results indicate that the monitoring of 40 to 60 inverters per head leads to an area penalty between 10 and 20%, while the related maximum response time is between 1 and 2 ns.

Finally, the cost in power consumption was estimated for a configuration of 40 monitored inverters per NMOS/PMOS mBBICS pair. Therefore, the chains were simulated for a frequency of 1 GHz and an activity of 20%. The increase of the power dissipation due to the application of mBBICS was estimated with 0.3%.

### 4.4. Robustness analysis

In this work, we consider robustness as the resilience of a system against technological process variations and environmental influences, *e.g.*, temperature fluctuations.

In order to determine the impact of environmental factors, we studied the impact of the temperature on the response time $t_{resp}$ of the

**Table 6**
Response time versus temperature.

| | NMOS type mBBICS ($Q_{coll}$ = 3.2 fC, 50 INV) | PMOS type mBBICS ($Q_{coll}$ = 3.6 fC, 40 INV) |
|---|---|---|
| Temp [°C] | $t_{resp}$ [ns] | $t_{resp}$ [ns] |
| −55 | No detection | 1.50 |
| −20 | 1.26 | 1.26 |
| 0 | 1.05 | 1.16 |
| 25 | 0.86 | 1.06 |
| 50 | 0.80 | 0.98 |
| 75 | 0.67 | 0.91 |
| 90 | 0.60 | 0.87 |
| 125 | No detection | 0.76 |

**Table 7**
Response time for different process corners and Monte-Carlo simulations.

| | $t_{resp}$ [ns] of NMOS type ($Q_{coll}$ = 3.2 fC, 50 INV) | $t_{resp}$ [ns] of PMOS type ($Q_{coll}$ = 3.6 fC, 40 INV) |
|---|---|---|
| FF | 0.33 | 0.55 |
| FS | 0.50 | 1.57 |
| SF | 1.85 | 0.76 |
| SS | 4.20 | 2.24 |
| MC (3σ) | 3.75 | 2.01 |

proposed sensor. Therefore, the NMOS type mBBICS was simulated with 50 inverters and $Q_{coll}$ = 3.2 fC, while the PMOS version was simulated with 40 inverters and $Q_{coll}$ = 3.6 fC. The devices sizes of each sensor are taken from Table 1.

The results listed in Table 6 indicate that the NMOS type mBBICS could not detect transient faults for temperatures lower than −20 °C and higher than 90 °C. In contrast, the PMOS type mBBICS proved to work over the complete analyzed temperature range of −55 °C to 125 °C. The reduction of $t_{resp}$ with increasing temperature follows mainly from the inverse relation between temperature and transistors threshold voltage [38]. Thus, at higher temperatures $v_{th,Nh2}$ decreases, which results in lower $t_{resp}$ (see also Sections 2 and 3).

Next, the impact of process variations on the response time was analyzed. Therefore, following corner cases, which are offered by the chosen technology, had been selected: fast-fast (FF), slow-slow (SS), fast-slow (FS) and slow-fast (SF), whereas the first term relates to the NMOS devices and the second to the PMOS ones. Further, for each sensor 1000 Monte-Carlo simulations have been executed and the 3σ-delay was determined [39]. The latter refers to the maximum delay over 99.86% of all simulations. In call cases, the temperature was set to 25 °C.

The results are listed in Table 7. It follows that in all cases the sensors could detect a transient fault. Although, it was only in FF and FS process corners (for NMOS type mBBICS) and FF and SF (for PMOS type mBBICS) that the fault could be detected in less than 1 ns. The higher response times for the corners SF (NMOS) and FS (PMOS) as well as for the Monte-Carlo simulations follow from the impact of Nh2 and Ph2 on $t_{resp}$ (see also Section 3.2).

### 4.5. Comparsion with related works

In a final step, the proposed mBBICS was compared to its unmodified version, similar to the one presented in [15]. Therefore, the sensor was implemented with the recommended parameters reported in [15] and the values for $Q_{coll}$ were set such that a transient fault occurred in the monitored inverter chains. The simulation results indicated that the unmodified sensor could solely monitor 10 inverters per head (NMOS and PMOS type). Hence, the proposed modifications increased the sensor's sensitivity by factor 6, in case of the PMOS type, and factor 8 for the NMOS type sensors. The response times are with 0.36 ns for the NMOS and 0.67 ns for the PMOS type roughly 50% lower than for the modified version. Differences to the results in [15] follow from the applied technologies, as a predictive 16 nm technology was chosen.

Table 8 compares the results of the proposed sensor to reported BBICS. The table list the area and power penalty to the monitored circuits, the minimum collected charge $Q_{coll}$ that could be detected and the related rise time $t_r$, as well as the applied technology. It should be noted that, following from Eq. (1), the smaller $Q_{coll}$ and the pulse width the lower the detection capability of the sensor. The comparison indicates that the proposed sensor offers an auspicious relation between detection sensitivity and area offset in comparison to the applied technology.

**Table 8**
Comparison to state-of-the-art BBICS architectures.

| Name/ref. | Area penalty | Power penalty | Min $Q_{coll}$ | $t_r/t_f$ | Technology |
|---|---|---|---|---|---|
| BBICS [7] | 29% | Not reported | 3.4 fC | 5/10 ps | 100 nm |
| S-BBICS [11] | 23% | +26% | 7.5 fC | 50/150 ps | 32 nm |
| DynBBICS [8] | 18% | Not reported | 55 fC | 2/50 ps | 130 nm |
| mBBICS_16nm [15] | 25% | 4% | 2 fC | 1/5 ps | 16 nm |
| mBBICS_65nm (this work) | 70% | 2% | 3.2 fC | 1/10 ps | 65 nm |
| This work | 17% | 0.3% | 2 fC | 1/10 ps | 65 nm |

**Table 9**
Comparison of hardware approaches for Soft Error Detection (SED).

| Name/ref. | Area penalty | Delay penalty | SED capability |
|---|---|---|---|
| Transient detection on Flip-Flops [41,42] | 44% | 25% | Partial |
| Time redundancy [40] | 0% | 96% | Partial |
| Duplication with comparison [43] | 112% | 10% | Full |
| This work | 17% | 0% | Full |

Table 9 compares the presented sensor with hardware approaches for soft error detection in terms of area and delay penalty as well as the capability to detect all soft errors. The techniques Transient detection on Flip-Flops and Time redundancy are not able to detect all soft errors, as both do not consider soft errors that last longer than a clock period [40–42]. It can be noted, that the proposed sensor has, compared to related approaches, a considerable area overhead and stands out with the absence of any delay penalty.

## 5. Conclusions

The application of Bulk Built-in Current Sensors (BBICS) is a promising solution to cope with increasing problems due to soft errors in nanometer technologies. However, these sensors demand high detection sensitivity in order to detect required level of collected charges, fast response times, high robustness against variations and reasonable area penalty. The proposed modification for BBICS includes adjustable voltage of the sensing transistors, body-biasing, and stack forcing to mitigate these problems. Simulations of a modified sensor in a commercial 65 nm technology indicated that the proposed sensor could detect all injected transient faults with response times close to 1 ns for the nominal case, and near 4 ns under wide process and temperature variations. This could be achieved with a reasonable area offset of 17% and very low increase in power dissipation. Further, in comparison to the unmodified version of the sensor, the sensitivity could be increased by up to factor 6, while the response time decreased by more than 50%. It should be noted, that the proposed design strategies are applicable on all *state-of-the-art* BBICS architectures.

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