The Impact of Aging Effects and Manufacturing Variation on SRAM Soft-Error Rate

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***Abstract*—This paper describes modeling and hardware results of how the soft-error rate (SER) of a 65-nm silicon-on-insulator SRAM memory cell changes over time, as semiconductor aging effects shift the SRAM cell behavior. This paper also describes how the SER changes in the presence of systematic and random manufacturing variation.**

***Index Terms*—Critical charge (Qcrit), radiation event, single event upset (SEU), soft-error rate (SER), soft errors.**

I. Introduction

SOFT ERRORS due to radiation, such as alpha particles and cosmic-ray neutrons, are a significant reliability concern in CMOS technologies, even though these particles do not permanently damage circuits. Unless error protection, such as an error-correction code, is employed, the soft-error rate (SER) of an SRAM array can exceed the rate of hard failures by orders of magnitude [1]. SRAMs are particularly susceptible to soft errors because the critical charge (Qcrit) required to upset a cell is exceptionally small [2]. With device scaling, low-power designs, and increased circuit density, the Qcrit of flip-flops and latches is approaching the SRAM Qcrit. Hence, the SER of these logic elements is a growing concern [3], and analyzing the SER in SRAM helps predict and design for upcoming problems in these elements.

Aging effects in semiconductors include well-known breakdown mechanisms (e.g., gate-oxide breakdown) and parametric degradation (e.g., negative bias temperature instability (NBTI) and hot-carrier effects). In deep-submicrometer technologies, the SRAM arrays are susceptible to Vmin problems, where the minimum voltage, at which an array functions, increases due to a combination of NBTI-induced threshold-voltage shifts and gate-oxide breakdown [4], [5].

We study the impact of aging, process variation, and environmental conditions on the SER of the 0.65-μm^2-thin-cell SRAM cell offered as part of the IBM 65-nm silicon-on-insulator (SOI) device technology [6]. Alpha-particle experiments using a ^{232}Th foil measured the SRAM SER dependence on temperature and gate length. Both alpha-particle accelerated tests and SRAM lifetests were used to observe the SER before and after high-voltage high-temperature stresses that caused Vmin shifts in the tested arrays. Modeling results using Qcrit values generated by circuit simulations track the experimental results well. Consequently, simulation tools are used to develop insight into the SER dependence on aging effects.

Manuscript received August 16, 2007; revised October 3, 2007. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under Contract NBCH30390004.

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Digital Object Identifier 10.1109/TDMR.2007.912983

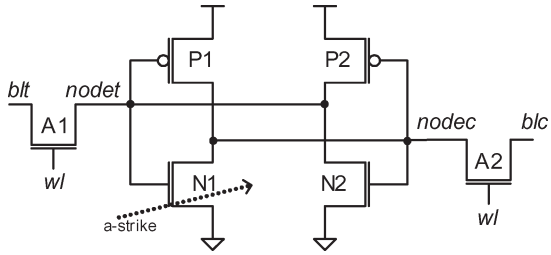

Fig. 1. High-density SRAM cell used for modeling and experiments.

II. Methodology

SER experiments and simulations in this paper use a symmetric six-transistor SRAM cell, as shown in Fig. 1. Alpha-particle and lifetest experiments were conducted according to the JEDEC standards JESD89-2 and JESD89-1, respectively [7], [8]. The alpha-particle experiments were conducted on a 1-Mb array of SRAM cells at wafer level, where the thorium foil was placed directly on top of the array with no air gap. The wafer temperature was controlled by a heat chuck, and tests used a logical checkerboard/checkerboard inverse pattern. The test duration was generally set to observe about 100 soft errors per test condition. Some longer tests included between 900 and 1300 soft errors, and the longest single test recorded over 4000 soft errors. Lifetests using 198 32-Mb arrays were conducted in Burlington, VT. The SRAMs were packaged on a ceramic substrate using a flip-chip technology.

Qcrit modeling was conducted according to the circuit-modeling methods described in [9]. The collection of charge generated in a radiation event was modeled as a current pulse from the drain to the body of the struck device. The magnitude of the current pulse was increased until the circuit just upsets, and Qcrit was determined as the charge delivered by this critical current pulse. The circuit model captures the gain from the parasitic bipolar transistor which is turned on by the charge collected in the device body.

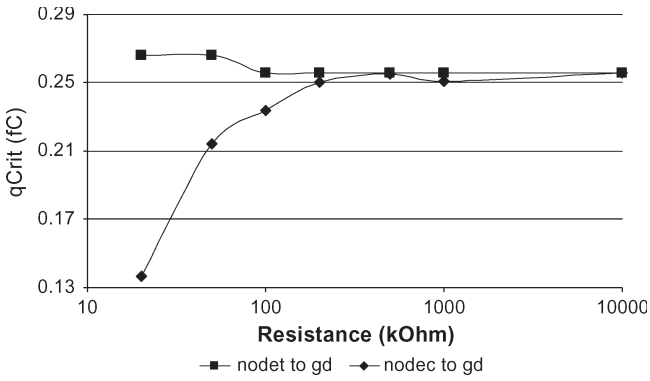

Fig. 2. Simulated Qcrit in the presence of gate-oxide breakdown.

The IBM proprietary SER simulation code SEMM2 models radiation events in circuits based on the radiation source and the circuit geometry [10]. In SOI technologies, only charge generated in the thin SOI layer contributes to upsets. Hence, SOI SRAMs have much lower SER than comparable bulk SRAMs (see [11] and references therein). SEMM2 can simulate alpha particles from the thick thorium foil used in the accelerated testing, as well as alpha particles from packaging materials (such as lead–tin solder) relevant in lifetests and eventual products. By sampling different alpha-particle events—alpha-particle birth location, birth energy, and angle—SEMM2 determines the probability that an alpha-particle event deposits more than Qcrit in the struck device. The simulated fail rate is proportional to the simulated fail probability. SEMM2 does not require fitting parameters; the user inputs include physical information about doping profiles, device layout, metallization layers, alpha source, and Qcrit values from circuit simulations.

III. Aging Effects

In this section, we investigate how Qcrit and the SER of an SRAM cell shift over time as aging effects degrade the NMOS and PMOS transistors. We model gate-oxide breakdown, NBTI, and hot-carrier effects. These three mechanisms are widely recognized in the semiconductor industry as the most prominent lifetime reliability concerns for transistors [12].

A. Gate-Oxide Breakdown

We model gate-oxide breakdown using the technique described in [5]. This technique connects a resistor between the true node (nodet) and ground, or the compliment node (nodec) and ground, representing the resistance of the gate-oxide-breakdown-induced leakage path in one of the pulldown devices. The resistance values were scaled from previous technology measurements. In all of our simulations, we injected charge into the N1 pulldown NFET device (from Fig. 1).

Fig. 2 shows how adding a resistor between nodet and ground (i.e., gate-oxide breakdown in the struck device) had a negligible impact on Qcrit. In contrast, adding a resistor between nodec and ground (i.e., gate-oxide breakdown in the opposite pulldown device, N2) shows the Qcrit falling linearly as the breakdown becomes catastrophic. In this realm of catastrophic breakdown, we anticipate a functional failure as well as an increased soft-error sensitivity (as the Qcrit drops from 0.25 to 0.15 fC, the alpha-particle and cosmic-ray SER contributions increase less than 50%).

B. NBTI

We model NBTI effects using a threshold-voltage shift indicative of stress and aging of PMOS devices. Our conditions of interest include nominal and worst case threshold-voltage shifts after burn in and at end of life.

Fig. 3 shows that Qcrit is unaffected by symmetric threshold-voltage shifts in both PFETs. An asymmetric threshold-voltage shift which weakens P1 (the pullup device above the struck device) causes the SRAM cell to become more sensitive to soft errors. This result follows the trend in Section IV-C since a threshold-voltage shift in P1 will move the SRAM Qcrit in the worst case direction. An asymmetric threshold-voltage shift which weakens P2 (the pullup device above the opposite inverter) makes the SRAM cell more robust since this device is now slower to react to noise on nodec. In the asymmetric NBTI cases, the largest effect on Qcrit is seen for the end of life, worst case device.

C. Hot Carrier

We model hot-carrier degradation as a decrease in NMOS transistor drive strength. We look at the nominal and worst case effects caused by burn in. Fig. 4 shows that the hot-carrier effects did not alter the device behavior enough to have an appreciable effect on Qcrit.

D. Vmin

Recent generations of SRAM are becoming more sensitive to cell-stability issues during the useful lifetime of the part. These cell-stability issues can be caused by combinations of several different reliability mechanisms (such as NBTI and gate-oxide leakage). One way to monitor SRAM cell stability is by looking at Vmin, which is the minimum voltage at which the SRAM operates. Parametric shifts over time due to device aging or defects will cause Vmin of the SRAM to increase.

We performed lifetest and alpha-particle experiments to look at the effects of reliability aging on the SER of SRAMs. A lifetest is a nonaccelerated test where the SRAMs are run in standard operating condition with no externally applied radiation sources. A lifetest was performed on 198 32-Mb SRAMs before and after a high-voltage high-temperature stress that simulated aging. The SRAM Vmins were also recorded before and after the stress. The lifetest was performed at nominal conditions for the SRAM and at ambient temperature in Burlington, VT, using a checkerboard/checkerboard inverse pattern. Both alpha particles and cosmic-ray neutrons contribute to the lifetest SER, where the alpha-particle contribution is dominant.

The SER values measured in the pre- and poststress lifetests are shown in Fig. 5. The lifetest measurements have large statistical uncertainties because few soft errors were observed. The

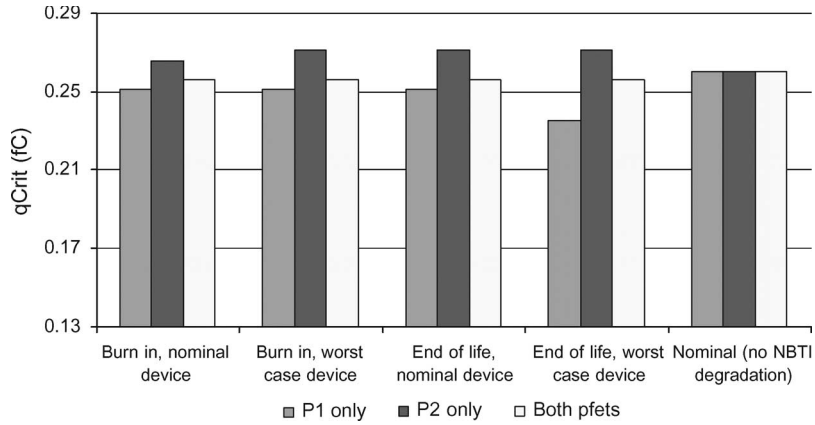

Fig. 3. Simulated Qcrit in the presence of NBTI shifts from aging.

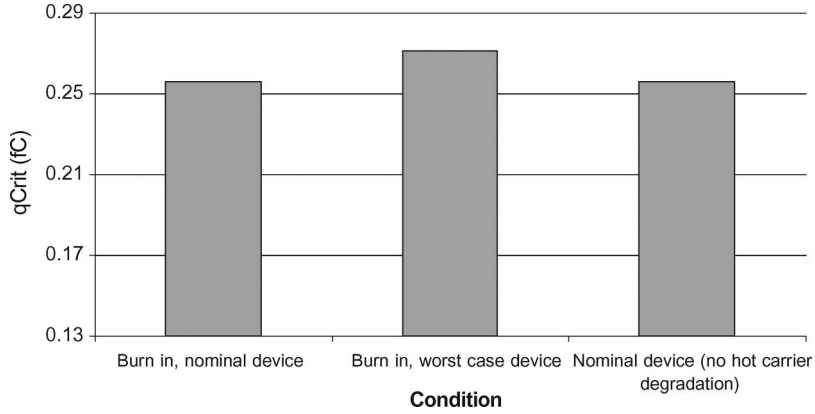

Fig. 4. Simulated Qcrit in the presence of hot-carrier aging effects.

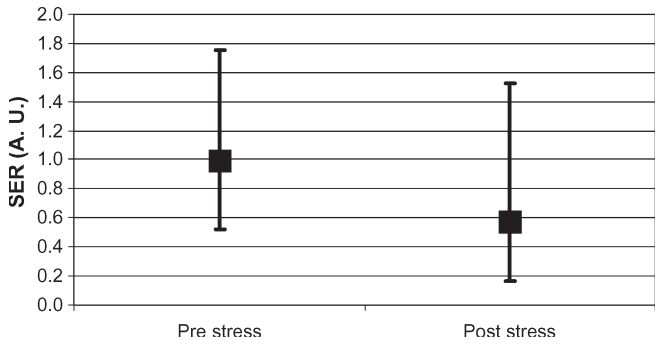

Fig. 5. Measured SER in normalized units for lifetest conducted before and after the aging stress.

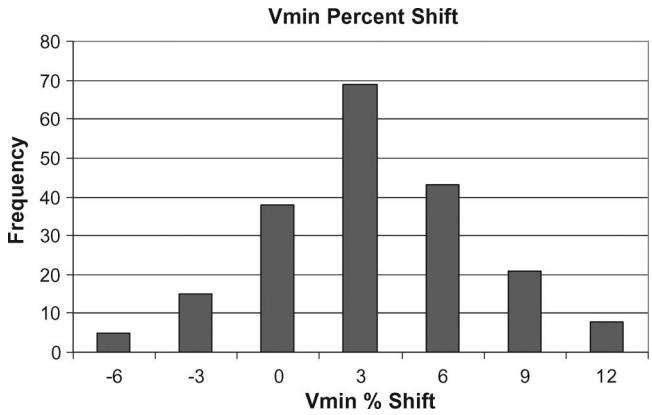

Fig. 6. Distribution of Vmin shift after the high-voltage high-temperature stress of lifetest population.

pre- and poststress SER statistical confidence bounds overlap significantly, which means that their values agree within statistical uncertainty.

The Vmin values before and after stress are shown in Fig. 6. As can be seen in the figure, the SRAM Vmin of the population after stress increased on average by 2.3%.

Alpha-particle tests were conducted on one chip at 25 °C and 1.0 V. The thorium-foil-induced fail rate was measured before and after a high-voltage high-temperature stress. The stress caused Vmin to shift 3%. The experimental results are shown in Fig. 7. We observed many more soft errors in the accelerated alpha-particle tests than in the lifetests, and the pre- and poststress fail rates agree within the tighter statistical uncertainty.

These lifetest and alpha-particle tests demonstrate that aging does not have a significant impact on the SER of an SRAM array. While a high-voltage high-temperature stress induces aging, as measured by the Vmin shift, it does not impact the SER. This is consistent with simulations which show that NBTI and hot-carrier-induced threshold-voltage shifts and non-catastrophic gate-oxide breakdown have very little impact on Qcrit. In the SRAM array, the small aging-induced Qcrit shift induces an insignificant SER shift.

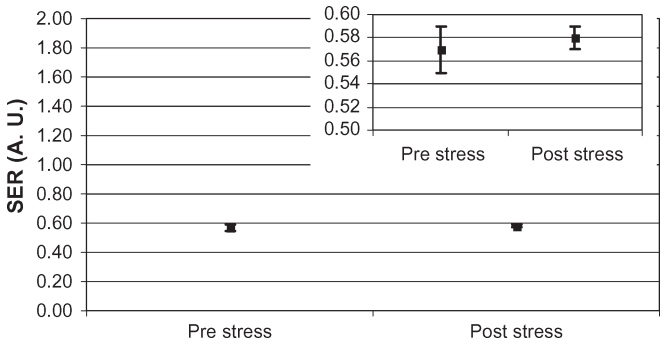

Fig. 7. Measured fail rate under a thorium foil in normalized units before and after the aging stress.

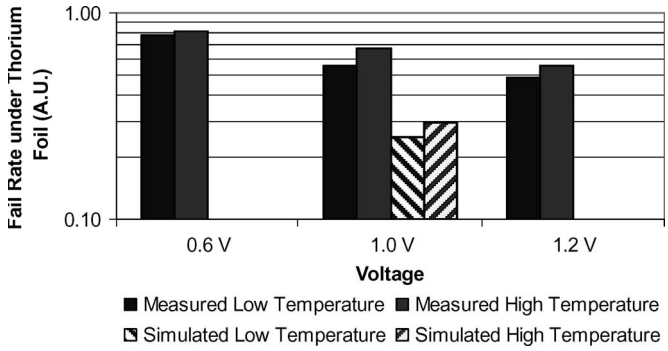

Fig. 8. Measured and simulated fail rates under a thorium foil at low (25 °C or ambient.) and high (100 °C) temperatures.

IV. Process Variation and Environmental Conditions

Within-chip variability has become a serious problem in current deep-submicrometer technologies. This is particularly true for SRAM designs. Arrays have the smallest devices on the chip and tend to be most sensitive to technology issues. Process variations between neighboring transistors, such as random dopant fluctuations, can degrade the SRAM cell performance and stability, making it more sensitive to external effects and environmental conditions. Hence, it is necessary to account for the impact of variability and environmental conditions on the robustness of array designs.

In previous SER studies, simulated Qcrit values in bipolar SRAMs were reported to change by more than 2x with process variations [13]. More recent studies have predicted process variation to influence Qcrit more modestly at tens of percent [9], [14], [15], with corresponding SER changes up to 15% [15], [16]. Parameters affecting transistor drive current—such as gate length, gate width, and threshold voltage—most directly impact Qcrit.

We performed experimental and simulation studies to quantitatively understand the SER dependence on process variation and environmental conditions.

A. SER Versus Temperature

Temperature effects on SER were measured in alpha-particle tests at three voltages. We tested three chips from two distinct process lots at high and low temperatures. For high-temperature tests, a heat chuck held the wafer at 100 °C during the testing. For two chips, the low-temperature tests were at 25 °C, whereas the third chip was tested at ambient temperature. Fig. 8 shows the fail rate measured in thorium-foil experiments, along with the simulated fail rates. Qcrit versus temperature was previously studied in [9]. Fig. 9 shows the results from this prior work. Qcrit decreases with increasing temperature. Mobility decreases with temperatures; consequently, at high temperature, the restoring transistor can less effectively counter the current from the struck transistor, making the circuit easier to upset. We simulated the fail rate induced by a thorium foil with SEMM2, using a thick thorium foil as the alpha source, and the Qcrit values from Fig. 9. At all voltages, the high-temperature fail rate exceeds the low-temperature fail rate. Averaging over the test voltages, the high-temperature fail rate is 13% larger. At 1.0 V, the simulated high-temperature fail rate is 18% larger than the low-temperature fail rate. The simulations track the SER trend with temperature extremely well, and the overall agreement is quite good, particularly with no fitting parameters to adjust the overall fail rate. The linear offset in Fig. 8 would typically be corrected with a fitting parameter.

B. SER Versus Channel-Length Variation

Alpha-particle tests at ambient temperature and three voltages were conducted on arrays processed to have short, nominal, and long channel lengths. We tested two chips from each process split. Qcrit versus channel length was previously studied in [9]. Fig. 10 shows the results from this prior work. Qcrit increases slightly with gate length; increasing the gate length makes the device more resistive, reducing the parasitic bipolar gain and making the circuit more difficult to upset [9]. Parasitic charge amplification is not a dominant mechanism in bulk technologies, where transistor gate length primarily impacts the SER through the drive strength of restoring devices. In a bulk technology, a long channel process split would have a higher SER because of the reduced drive strength of the restoring devices [15]. Fig. 11 shows the experimental measurements and the accompanying simulations. Averaging over voltage, the fail rate for short channel chips is about 10% higher than for nominal channel chips, whereas the fail rate for long channel chips is 4% lower than for the nominal channel. The simulations predict the correct trend but underestimate the magnitude of the SER changes. The simulated fail rate of a cell with short channel devices is 3% higher than for nominal channel devices, and long channel devices have a 1% lower fail rate.

C. Intrinsic Threshold-Voltage Variation

Previous investigations of the SRAM cell stability (see [17] and the references contained therein) showed that the threshold-voltage fluctuations (σV_{t}) of the six SRAM cell transistors are inversely proportional to the device dimensions, i.e., L and W, as follows:

$$\sigma V_{\mathrm{t}} \propto \sqrt{\frac{1}{L \times W}}. \tag{1}$$

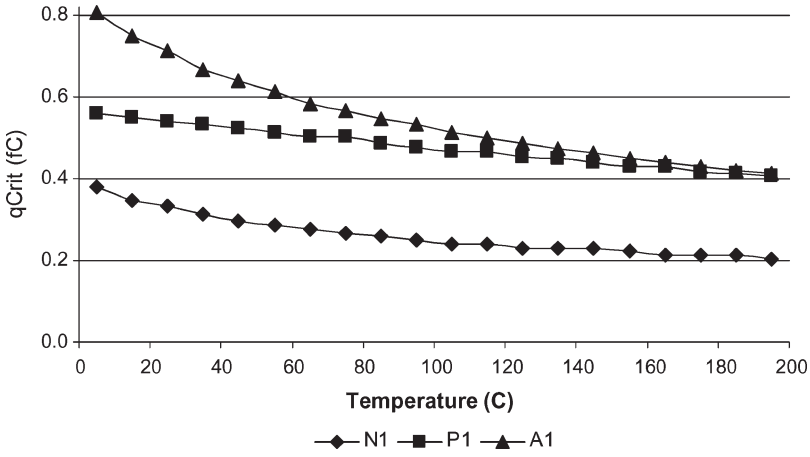

Fig. 9. Temperature sweep of Qcrit for SRAM cell.

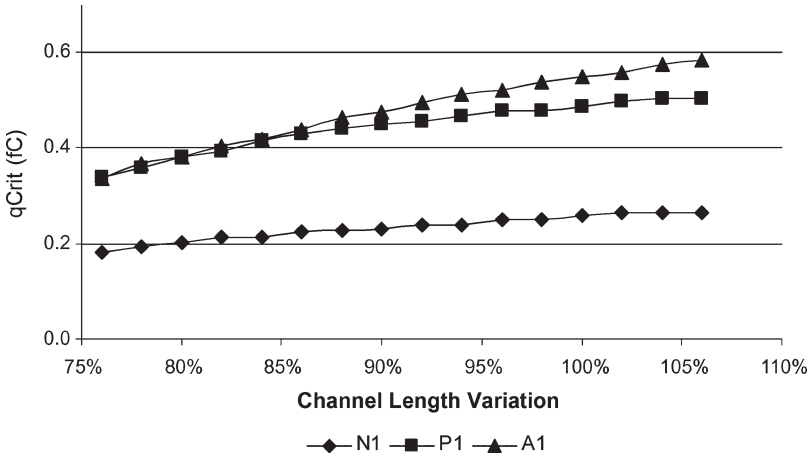

Fig. 10. Channel-length sweep of Qcrit for SRAM cell.

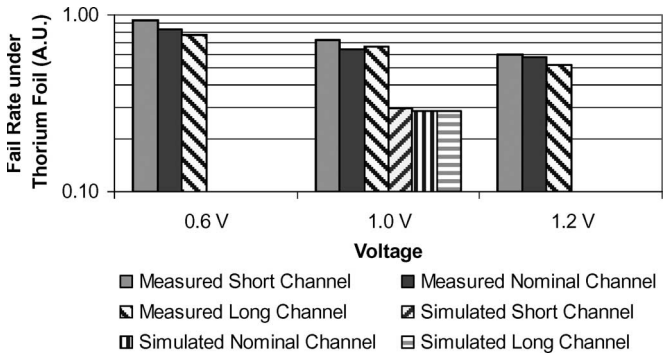

Fig. 11. Measured and simulated fail rates under a thorium foil for short, nominal, and long channel devices.

We studied the impact of threshold-voltage variability on the vulnerability of the SRAM cell to the soft errors by looking at deviations in the cell Qcrit.

We first performed a 2^k factorial analysis [18] to study the significance of device-by-device Vt variations on the overall cell Qcrit. The following paragraphs describe how we conducted our modeling.

We have six devices in the SRAM cell, and each device in a factorial experiment can either have or not have a Vt variation. This means that we have $2^6 = 64$ Vt variation possibilities.

When a given Vt variation is turned on, it is set in a worst case systematic direction which reduces the cell Qcrit. Table I illustrates these directions. We determined Qcrit for each of the 64 cases. We then repeated the set of 64 Qcrit simulations with the degree of Vt variation ranging from 1 to 5σ.

The next step was to determine the device-by-device contributions to the overall cell Qcrit. For each device, we averaged both the Qcrit values over the 32 cases where the Vt variation was turned on and the Qcrit values over the 32 cases where the Vt variation was turned off (for a fixed degree of Vt variation, e.g., 1σ). The difference between these two averaged Qcrit values tells us the relative contribution of that device's Vt variation to the overall cell Qcrit. The normalized device-by-device contributions to the cell Qcrit, for 1 to 5σ variation, are reported in Table II. Entries with larger values in each row indicate that the cell is more sensitive to the threshold-voltage variation of the corresponding device.

When device N1 is exposed to radiation, electron–hole pairs are created in its body. Electrons diffuse out of the body, leaving the holes, which increase the body potential and generate a parasitic bipolar current [9]. The parasitic bipolar current discharges the N1 drain, i.e., nodec. As the voltage on nodec decreases, device N2 turns off, device P2 turns on, and the voltage on nodet begins to rise. This increase in nodet voltage

TABLE I
WORST CASE Vt SHIFTS FOR Qcrit DEGREDATION

	A1	P1	N1	A2	P2	N2
Device Characteristic	Strong	Weak	Strong	Strong	Strong	Weak
Direction of Vt Shift	Negative	Positive	Negative	Negative	Negative	Positive

TABLE II
NORMALIZED AVERAGE EFFECT OF EACH DEVICE ON THE SRAM CELL Qcrit

	N1	N2	P1	P2	A2	A1
1σ	1.00	0.26	0.68	0.37	0.00	0.00
2σ	1.00	0.27	0.63	0.57	0.00	0.00
3σ	1.00	0.18	0.51	0.54	0.0	0.01
4σ	1.00	0.19	0.49	0.51	0.00	0.06
5σ	1.00	0.18	0.35	0.47	0.00	0.04

turns on device N1 even harder, which reinforces the logical perturbation.

Table II shows that device N1, the struck device, always has the largest effect on the cell Qcrit. The worst case threshold-voltage variation for this device makes it stronger and more likely to discharge the nodec. The two PFET pullup devices also have a significant impact on the Qcrit. Device P2 propagates the radiation event by pulling up nodet, whereas device P1 restores nodec during a radiation event. The opposing pulldown device, N2, is less significant than the pullup devices because it is a tertiary contributor. It fights device P2 to hold nodet at its initial voltage. The passgate transistors A1 and A2 only weakly contribute to the soft errors via leakage currents. Other forms of process variation that affect the transistor drive strength, such as gate length or width variation, will impact the SRAM Qcrit in a similar fashion.

Note that in the bulk technology studied in [14], the relative importance of the pulldown transistors N1 and N2 is reversed compared with the SOI technology in this paper. The parasitic bipolar current that dominates the soft errors in SOI technologies is not an important factor in bulk technologies; thus, the threshold voltage of the struck transistor is not the most important factor that determines the cell Qcrit.

D. Random Process Variation

We used the methodology proposed in [19] to obtain the statistical distribution of Qcrit values for the SRAM cell in the presence of random dopant fluctuations (resulting in random Vt shifts) in each of the six devices.

First, we generated a sample of SRAM cells with different realizations of the Vt variations. We injected a charge Qinj into each cell in the sample and determined the probability of a cell having a Qcrit less than Qinj (e.g., if a cell flipped, the cell's Qcrit was less than Qinj). We varied Qinj from Qmin to Qmax to determine the cumulative distribution function (cdf) for Qcrit. We used the important sampling methodology proposed in [18] to distort the sample to emphasize cells with Qcrit close to Qinj. The commonly used Monte Carlo methods require much larger sample sizes to determine near-tail probabilities corresponding to Qinj values 2–3σ from the mean. We adaptively determined the range of Qinj based on our desired cdf range.

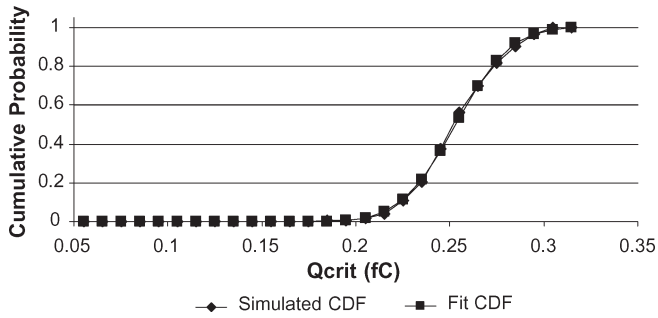

Fig. 12. Qcrit cdf fits well into a normal distribution.

Fig. 12 shows the simulated cdf of Qcrit. The cdf can be read as follows. If x amount charge is injected, then the probability of the cell having a Qcrit lower than x is $y\%$. If we assume that the probability density function (pdf) is Gaussian, with the form

$$\text{pdf}(\text{Qcrit}) = \frac{1}{(\sqrt{2\pi})\sigma} e^{-\frac{(\text{Qcrit}-Q_0)^2}{2\sigma^2}} \tag{2}$$

where Q_0 and σ are the mean and standard deviation, respectively, the cdf has the form

$$\text{cdf}(\text{Qcrit}) = 0.5\left[1 + \text{erf}\left(\frac{\text{Qcrit} - Q_0}{\sqrt{2}\sigma}\right)\right] \tag{3}$$

where $\text{erf}(x)$ is the error function.

We fit the cdf to the simulations and obtained $Q_0 = 0.25$ fC and $\sigma = 0.023$. The fitted cdf is also shown in Fig. 12. Note that the mean Qcrit value from fitting the cdf compares well with the Qcrit simulated with nominal process parameters, i.e., 0.26 fC.

The SER of a circuit is a function of Qcrit, and the alpha-particle-induced SER has a stronger Qcrit dependence than the cosmic-ray-induced SER [11]. We modeled the SRAM SER caused by alpha particles from the lead–tin solder as a function of Qcrit and fit it to an exponential decay of the form

$$\text{SER}(\text{Qcrit}) = A \times e^{-\beta \times \text{Qcrit}} \tag{4}$$

where A and β are constants. For an array with a distribution of Qcrit values, the mean SER, $\langle \text{SER} \rangle$, of the array is

$$\langle \text{SER} \rangle = \int_0^\infty [\text{pdf}(\text{Qcrit}) \times \text{SER}(\text{Qcrit})]\, d\text{Qcrit}. \tag{5}$$

Since the SER is not a linear function of Qcrit, the mean SER of an array will not be equal to the nominal SER, i.e., $\text{SER}(Q_0)$. By assuming a Gaussian distribution of Qcrit values, as in (2),

and an exponential dependence of SER on Qcrit, as in (4), the mean SER is related to the nominal SER by

$$\langle \mathrm{SER} \rangle = \mathrm{SER}(Q_0) \times e^{\frac{\beta^2 \sigma^2}{2}}. \quad (6)$$

Note that to derive (6), we extend the lower limit of the integral to negative infinity. This is a reasonable approximation since the pdf of Qcrit must become negligible at a positive Qcrit value to maintain the cell stability. In the 65-nm SOI technology that we study, the mean lead–tin solder SER, i.e., $\langle \mathrm{SER} \rangle$, differs by the nominal lead–tin solder SER, i.e., $\mathrm{SER}(Q_0)$, by less than 1%. While cells in an array have a distribution of Qcrit values (and, thus, of SER values) due to random threshold-voltage variations, fully accounting for the distribution of the Qcrit values is a negligible correction to the SER at nominal Qcrit.

V. Conclusion

In this paper, we studied the impact of aging effects on the SER of a 65-nm SOI six-transistor SRAM cell. We found that aging effects have very little impact on the SRAM SER. As a corollary investigation, we conducted experiments and modeling of manufacturing variation. We found that our SER simulations of temperature and gate length track the trends measured in our experimental data. We also analyzed how the variations of each device (from aging, manufacturing, or environment) contribute to the overall cell Qcrit. We found that process variations in the struck NFET device were the primary contributor to Qcrit shifts, followed by the two pullup PFETs, the opposite pulldown NFET, and then the passgate NFETs. Finally, we analyzed the effects of considering a Gaussian distribution of Qcrit values (due to process variation) rather than Qcrit of a nominal cell. We found that accounting for the Qcrit distribution produced a negligible correction to the SER.

Acknowledgment

The authors would like to thank their colleagues within IBM for fruitful discussions regarding this paper. The authors would also like to thank R. Dennard, M. Gordon, D. Heidel, T. Ning, C. Plettner, K. Rodbell, and H. Tang. Finally, the authors would like thank S. McAllister and C. Montrose for invaluable testing support.

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