RTD2522
Flat Panel Display Controller

Revision 0.81

June 20, 2003

General
- Embedded dual DDC can support DDC1, DDC2B, DDC/CI
- Embedded 3 programmable PWM
- Zoom scaling up and down
- Embedded pattern generator
- No external memory required.

Analog RGB Input Interface
- Integrated 8-bit triple-channel 140MHz ADC/PLL
- Support up to 140MHz (SXGA@ 75Hz)
- Support Sync On Green (SOG) and de-composite sync modes
- On-chip high-performance PLLs

Digital Input Interface
- Support 8-bit video (ITU 656) format input
- Built-in YUV to RGB color space converter & de-interlace

DVI Compliant Digital Input Interface
- Single link on-chip YMDS receiver
- Operation up to 165Mhz
- Direct connect to DVI compliant TMDS transmitter
- High-Bandwidth Digital Content Proection (HDCP)
- Enhanced protection of HDCP secret key

Auto Detection /Auto Calibration
- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for phase and image position calibration

Scaling
- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement

Color Processor
- Digital brightness and contrast adjustments
- sRGB compliance
- Gamma correction
- Dithering logic for 18-bit panel color depth enhancement

Output Interface
- Built-in display timing generator and fully programmable
- 1 and 2-pixel/clock panel support and up to 140MHz
- Scaler internal LSB/MSB swap, odd/even swap and red/blue group swap.
- Programmable TCON function support
- Reduced EMI and Power saving feature
- Dual LVDS Interface Output
- Integrated Spread-Spectrum DCLK PLL.

Host Interface
- Support MCU serial bus interface

Embedded OSD
- 12*18 dot font per character.
- Embedded fully functional OSD support multi-language
- Embedded 256 characters and symbols including 16 multi-color symbols.
- User’s font ram, which make customer can program 128 special symbols.
- 32 programmable color font
- 7 background color and 8 character color.
- Programmable width and height control.
- 4 background window.
- Selectable shadow color for windows and characters.
- Intensity, blinking effect.
- Fade-in/out effect.
- Frame shadowing and independent row shadowing.
- Frame bordering and independent row bordering.
- 3 channels 8 bits PWM output, and selectable PWM clock frequency.
- Row-to-Row spacing to maintain constant display height.
- Window alpha-blending effect.

Power & Technology
- 2.5V/3.3V power supplier
- 128-pin QFP package.

RTD2522 Pin-Out Diagram

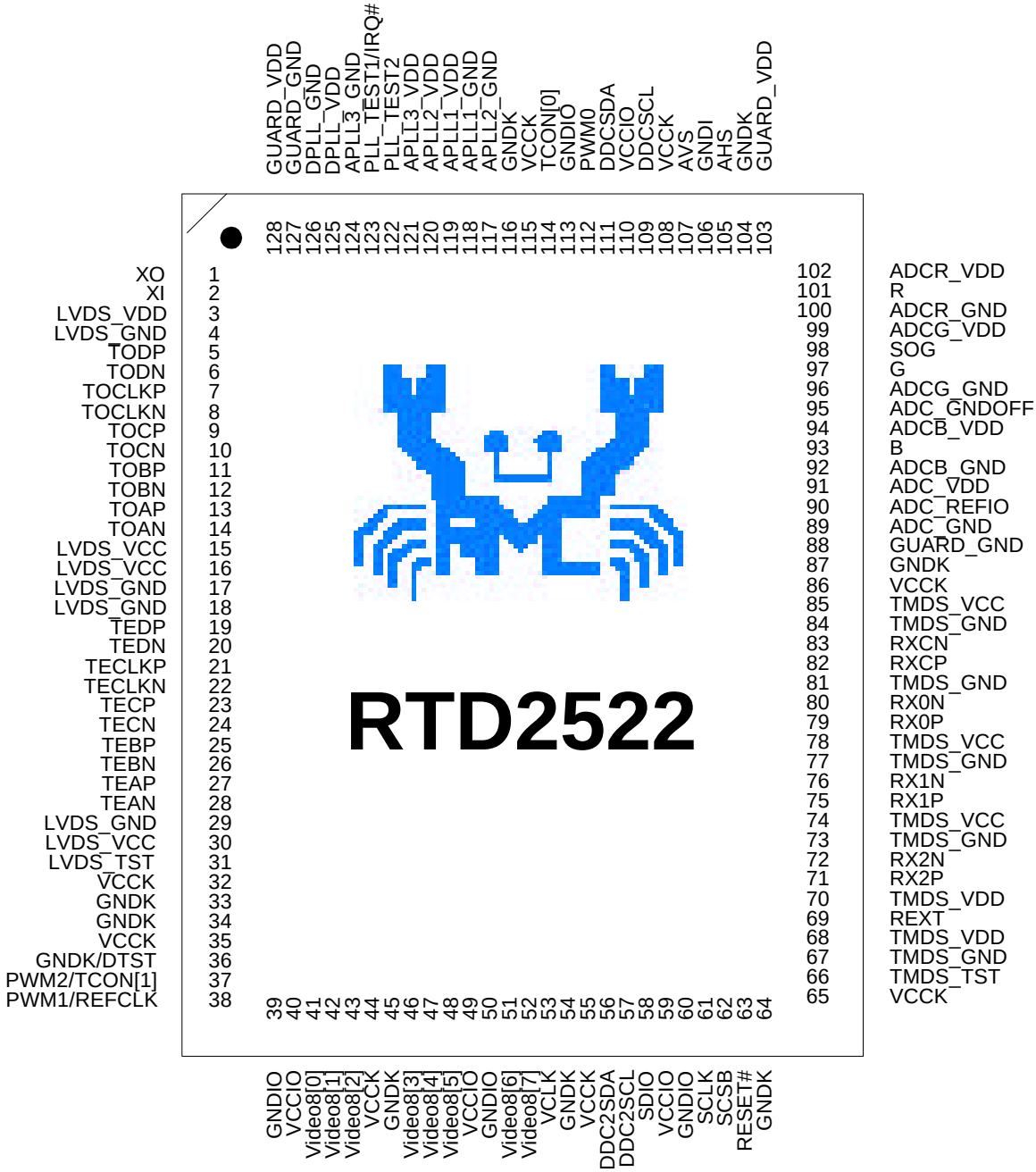


Figure 1 RTD2522 Pin-Out Diagram

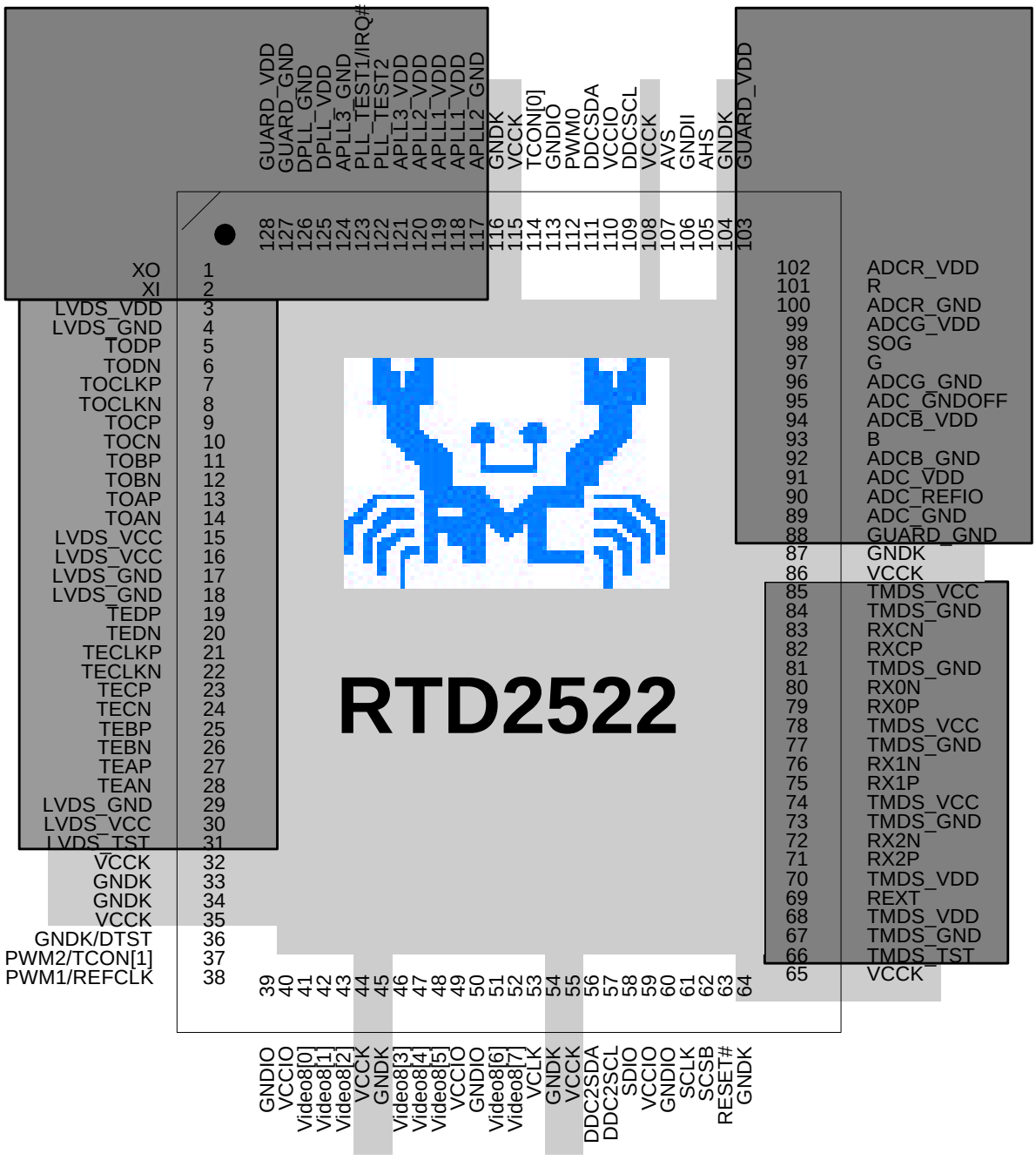


Figure 2 Board Power Plane Design

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

ADC: 16 pins

Name	I/O	Pin No	Description	Note
ADC_GUARD_GND	AG	88	ADC guard-ring ground	
ADC_GND	AG	89	ADC clock/band-gap ground	
ADC_REFIO	AP	90	ADC band-gap voltage de-couple	1.20V
ADC_VDD	AG	91	ADC clock/band-gap power	(3.3V)
ADCB_GND	AG	92	Analog ground for BLUE channel	
B	AI	93	Analog input from BLUE channel	
ADCB_VDD	AP	94	Analog power for BLUE channel	(3.3V)
ADC_GNDOFF	AI	95	ADC differential reference GND	
ADCG_GND	AG	96		
G	AI	97	Analog input from GREEN channel	
SOG/ADC_TEST	AIO	98	SOG in / ADC test pin	
ADCG_VDD	AP	99		(3.3V)
ADCR_GND	AG	100	Analog ground for RED channel	
R	AI	101	Analog input from RED channel	
ADCR_VDD	AP	102	Analog power for RED channel	(3.3V)
ADC_GUARD_VDD	AP	103	ADC guard-ring power	(3.3V)

PLL: 14 pins

Name	I/O	Pin No	Description	Note
XI	AI	2	Reference clock input	
XO	AO	1	Reference clock output	
PLL_GUARD_VDD	AP	128	PLL guard-ring power	(3.3V)
PLL_GUARD_GND	AG	127	PLL guard-ring ground	
DPLL_GND	AG	126	Ground for digital PLL	
DPLL_VDD	AP	125	Power for digital PLL	(3.3V)
APLL3_GND	AG	124	Ground for hvmti PLL, hvana PLL	
PLL_TEST1	AIO	123	Test Pin 1 / IRQ#	
PLL_TEST2	AIO	122	Test Pin 2	
APLL3_VDD	AP	121	Power for hvmti PLL, hvana PLL	(3.3V)
APLL2_VDD	AP	120	Power for analog PLL	(3.3V)
APLL1_VDD	AP	119	Power for multi-phase PLL	(3.3V)
APLL1_GND	AG	118	Ground for multi-phase PLL	
APLL2_GND	AG	117	Ground for analog PLL	

Control Interface: 4 pins

Name	I/O	Pin No	Description	Note
SCSB	I	62	Serial control I/F chip select	(2), (3), (5) (2), (3), (6)
SCLK	I	61	Serial control I/F clock	(2), (3), (5) (2), (3), (6)
SDIO	I/O	58	Serial control I/F data in	(1), (2), (3) /, 2mA
RESET#	I	63	RESET# for Controller;	(2), (3), (5)

TMDS: 20 pins

Name	I/O	Pin No	Description	Note
TMDS_VDD	P	85		
TMDS_GND	G	84		
RXC-/RXC+	I	83,82	Differential Clock Input	
TMDS_GND0	G	81		
R0-/R0+	I	80,79	Differential Data Input	
TMDS_VDD0	P	78		
TMDS_GND1	G	77		
R1-/R1+	I	76,75	Differential Data Input	
TMDS_VDD1	P	74		
TMDS_GND2	G	73		
R2-/R2+	I	72,71	Differential Data Input	
TMDS_VDD2	P	70		
EXT_RES	A	69	Impedance Match Reference.	
TMDS_VDD3	P	68		
TMDS_GND3	G	67		
TMDS_TEST	AIO	66	TMDS_TEST Pin	

Digital Input: 13 pins

Name	I/O	Pin No	Description	Note
AHS	I	105	VGA-port Horizontal Sync;	(2), (4), (5)
AVS	I	107	VGA-port Vertical Sync;	(2), (4), (5)
VCLK	I	53	Video-port input clock;	(1), (2)
VIDEO8 [7:0] / ADC_OUT [7:0] / TMDS_OUT [7:0]	I O	52,51, 48,47, 46,43, 42,41,	Video-port input data (ITU-R-BT656) / ADC test data output / TMDS test data output	(1), (2), (3) 8mA, slew
TCON [0]	IO	114	TCON [0] output	8mA, No slew

PWM Interface: 3 pins

Name	I/O	Pin No	Description	Note
PWM_0	O	112	PWM_0 output;	2mA, skew
PWM_1 / REFCLK	IO	38	PWM_1 / (In / out) testpin for DCLK / Video8 even-odd signal	(2) 2mA, slew
PWM_2 / TCON [1]	O	37	PWM_2 output / TCON [1] output	8mA, No slew

DDC Channel: 4 pins

Name	I/O	Pin No	Description	Note
DDCSCL #1	I	109	DDC serial control I/F clock	(2), (3), (5)
DDCSDA #1	IO	111	DDC serial control I/F data input DDC serial control I/F data output	(2), (3), (5), (6) 8mA, No slew
DDCSCL #2 (HDCP)	I	57	DDC serial control I/F clock	(2), (3), (5)
DDCSDA #2 (HDCP)	IO	56	DDC serial control I/F data input DDC serial control I/F data output	(2), (3), (5), (6) 8mA, No slew

LVDS Interface: 29pins

Name	I/O	Pin No	Description	Note
LVDS_VCC	AP	3	Analog LVDS Output Power	(3.3V)
LVDS_GND	AG	4	Analog LVDS Output Ground	
TODP	AO	5	LVDS Odd Output TD+	
TODN	AO	6	LVDS Odd Output TD-	
TOCLKP	AO	7	LVDS Odd Output CLK+	
TOCLKN	AO	8	LVDS Odd Output CLK-	

TOCP	AO	9	LVDS Odd Output TC+	
TOCN	AO	10	LVDS Odd Output TC-	
TOBP	AO	11	LVDS Odd Output TB+	
TOBN	AO	12	LVDS Odd Output TB-	
TOAP	AO	13	LVDS Odd Output TA+	
TOAN	AO	14	LVDS Odd Output TA-	
LVDS_VCC	AP	15	Analog LVDS Output Power	(3.3V)
LVDS_VCC	AP	16	Analog LVDS Output Power	(3.3V)
LVDS_GND	AG	17	Analog LVDS Output Ground	
LVDS_GND	AG	18	Analog LVDS Output Ground	
TEDP	AO	19	LVDS Even Output TD+	
TEDN	AO	20	LVDS Even Output TD-	
TECLKP	AO	21	LVDS Even Output CLK+	
TECLKN	AO	22	LVDS Even Output CLK-	
TECP	AO	23	LVDS Even Output TC+	
TECN	AO	24	LVDS Even Output TC-	
TEBP	AO	25	LVDS Even Output TB+	
TEBN	AO	26	LVDS Even Output TB-	
TEAP	AO	27	LVDS Even Output TA+	
TEAN	AO	28	LVDS Even Output TA-	
LVDS_GND	AG	29	Analog LVDS Output Ground	
LVDS_VCC	AP	30	Analog LVDS Output Power	(3.3V)
LVDS_TST	O	31	LVDS Test-pin	

Power & Ground: 25 pins

Name	I/O	Pin No	Description
3.3V Power	P	40, 49,59, 110	VCC33: 4
3.3V Ground	G	39,50, 60,106, 113	GNDO: 5
2.5V Power	P	32,35, 44,55, 65,86, 108,115	VCCK: 8
GNDK / DTST	IO	36	GNDK/Digital Test Input
2.5V Ground	G	33,34, 45,54, 64,87, 104,116	GNDIK: 8

Note: (1) TTL compatible CMOS Input (Vt=1.7V); VCC=3.3V;
(2) 5V tolerance pad;
(3) Internal 75K Ohms pull high resistor.
(4) Internal 75K Ohms pull low resistor.
(5) Schmitt trigger CMOS Input (Vt=1.4-~2.2V);
(6) Open-Drain, Output Drive low & Pull-high.
(7) Bi-directional input/output

General Description

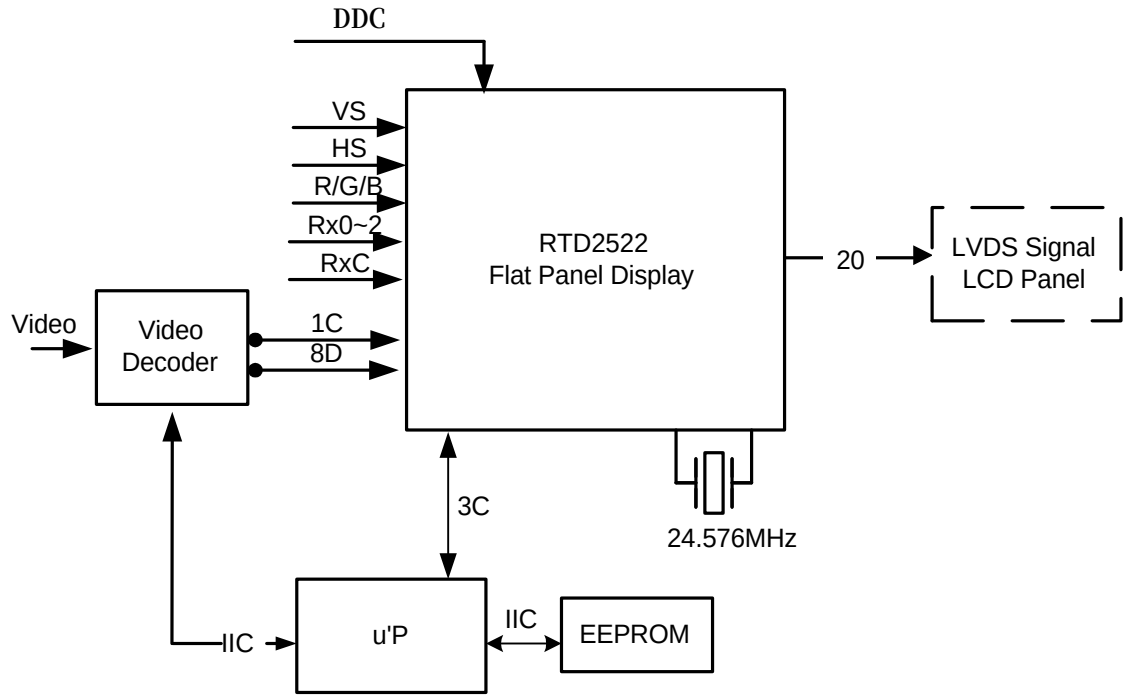


Figure 3 Application System Block Diagram

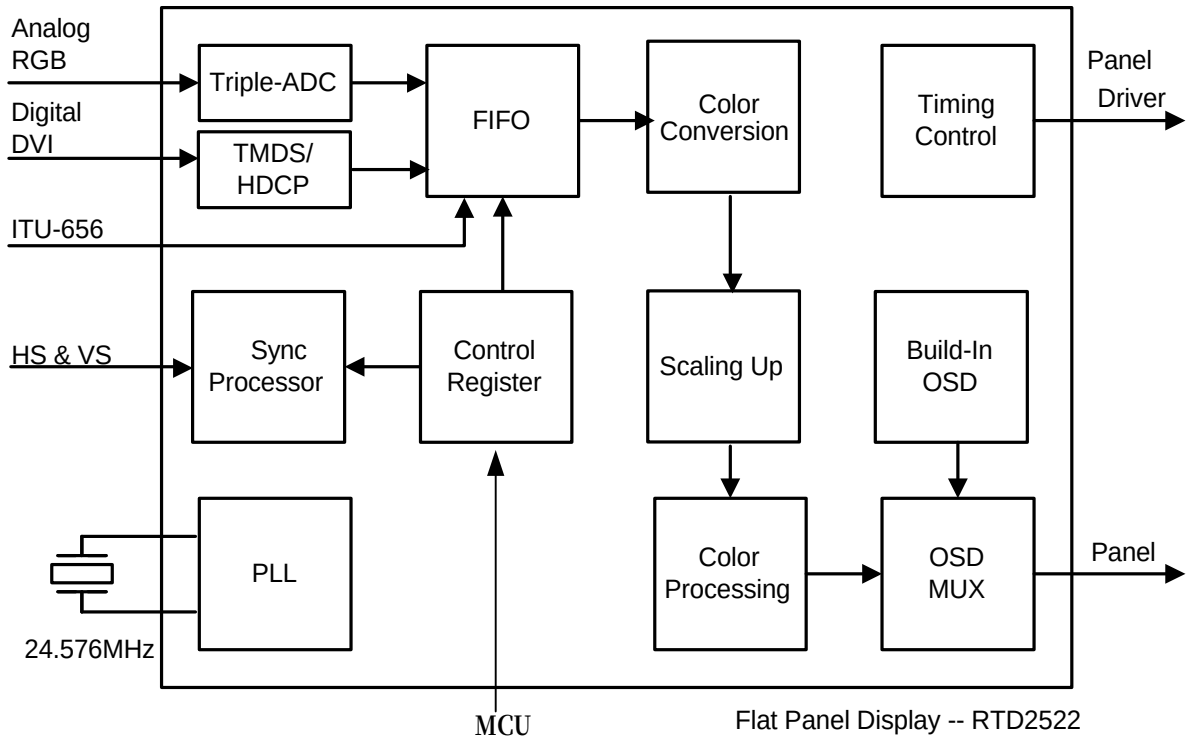


Figure 4 Chip Functional Block Diagram

Functional Description

Input

1.1.1 *Digital Input (ITU 656)*

RTD2522 is designed to connect the interface of digital signal from video decoder. Input data is latched within a capture window defined in registers. The timing scheme designed for input devices are showed in the following diagram.

There are not H sync、V sync signals provided by the video decoder with ITU BT.656, these synchronal signals have to be generated by decoding the EAV & SAV timing reference signals.

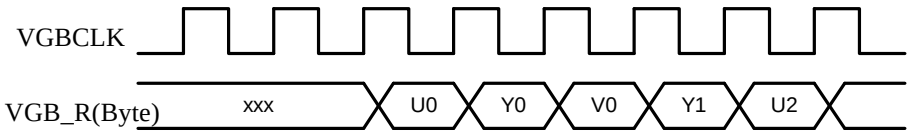


Figure 5 Input YUV 4:2:2(8-bits) Timing

Only 254 of possible 256 8-bit words may be used to express a signal value, 0 and 255 are reserved for data identification purposes. Video 8 data stream is as below:

Blanking period			Timing reference code				720 pixels YUV 422 DATA									Timing reference code				Blanking period		
…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	Cb2	Y2	…	Cr718	Y719	FF	00	00	EAV	80	10	…

Cbn: U(B-Y) colour difference component
Yn : luminance component
Crn: V(R-Y) colour difference component

SAV/EAV format

Bit 7	Bit 6(F)	Bit 5(V)	Bit 4(H)	Bit 3(P3)	Bit 2(P2)	Bit 1(P1)	Bit 0(P0)
1	Field bit 1st field F=0 2nd field F=1	Vertical blanking bit V=1 Active video V=0	H=0 in SAV H=1 in EAV	Protection bits			

Hardware can recognize the occurrence of EAV & SAV by detecting the 0xff , 0x00 , 0x00 data sequence, and then generate the Hsync、Vsync、Field signals internally by decoding the fourth word of the timing reference signal(EAV、SAV). F & V change state synchronously with the EAV(End of active video) reference code at the beginning of the digital line.

Bits P0, P1, P2, P3, have states dependent on the states of the bits F, V and H as shown below. At the

receiver this permits one-bit errors to be corrected and two-bits errors to be detected.

Protection bits

F	V	H	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

Error correction

A = P1 xor F xor V
B = P2 xor F xor H
C = P3 xor V xor H
D = F xor V xor H xor P3 xor P2 xor P1 xor P0

F' = F xor (D. A . B. C#)
V' = V xor (D. A. B#. C)
H' = H xor (D. A#. B. C)

SAV/EAV one-bit error occurs when D. (A + B + C)
SAV/EAV two-bit error occurs when D#. (A + B + C)

1.1.2 *Analog Input*

RTD2522 integrates three ADC's (analog-to-digital converters), one for each color (red, green, and blue). The sync-processor can deal with Separate-Sync, Composite-Sync, and Sync-On-Green. And the PLL can generate very low jitter clock from HS to sample the analog signal to digital data. Input data is latched within a capture window defined in registers refer to VS and HS leading edge.

1.1.3 *TMDS Input*

RTD2522 integrates high-speed single link receiver and high bandwidth content protection (HDCP) function. It can operate up to 165Mhz.

1.1.4 *Input Capture Window*

Inside RTD2522, there are four registers IPH_ACT_STA, IPH_ACT_WID, IPV_ACT_STA & IPV_ACT_LEN to define input capture window for the selected input video on either ADC or TMDS or Video8 input port while programmed analog input mode. The horizontal sync (IHS) & vertical sync (IVS) signals are used from the selected port to determine the capture window region.

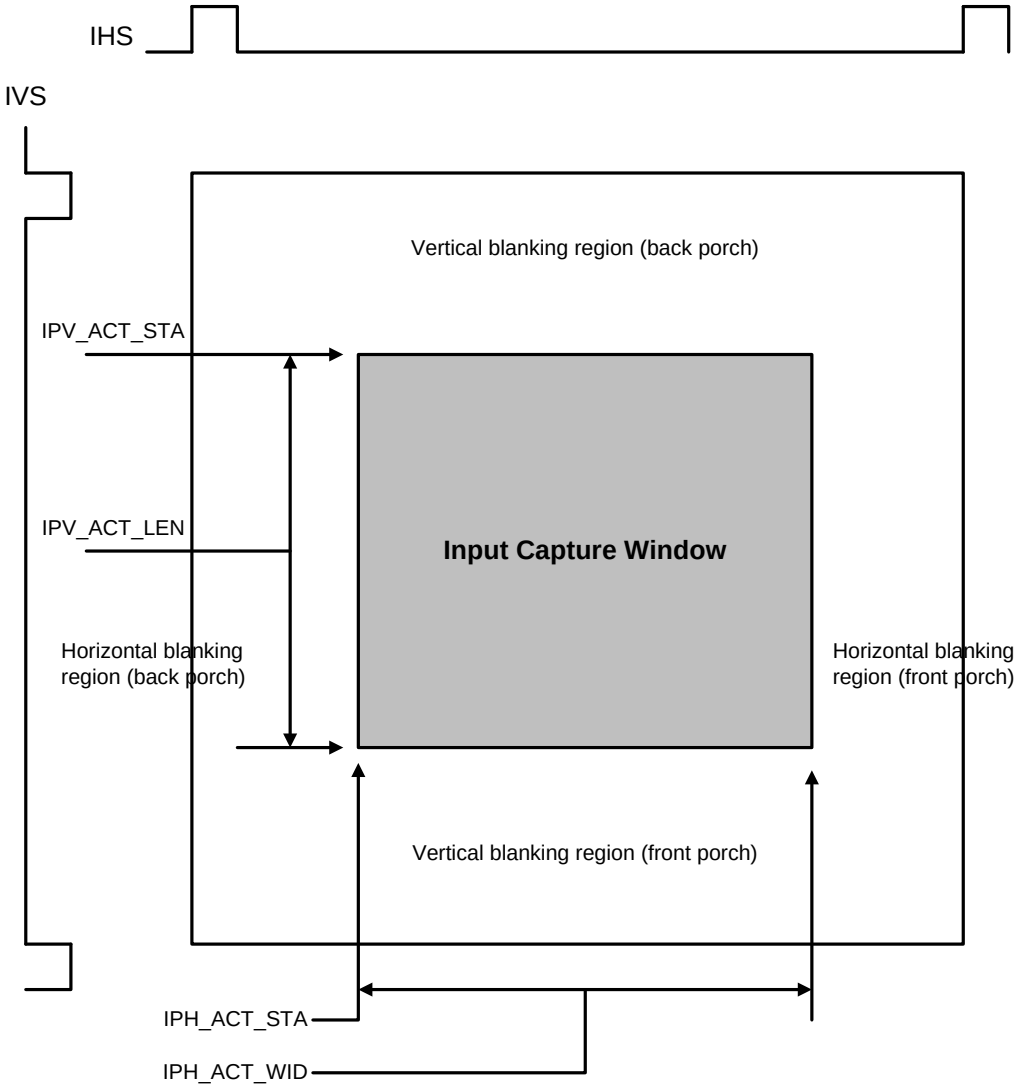


Figure 6 Input Capture Window

Output

1.1.5 *Display Active Window*

These registers to define the display active window are showed us below in application with frame buffer. In the case of without frame buffer that means frame sync mode, the definitions of these registers are quiet different from the description below. There are two frame sync modes applied to RTD2522 chip for various applications. Refer to the register description for detailed.

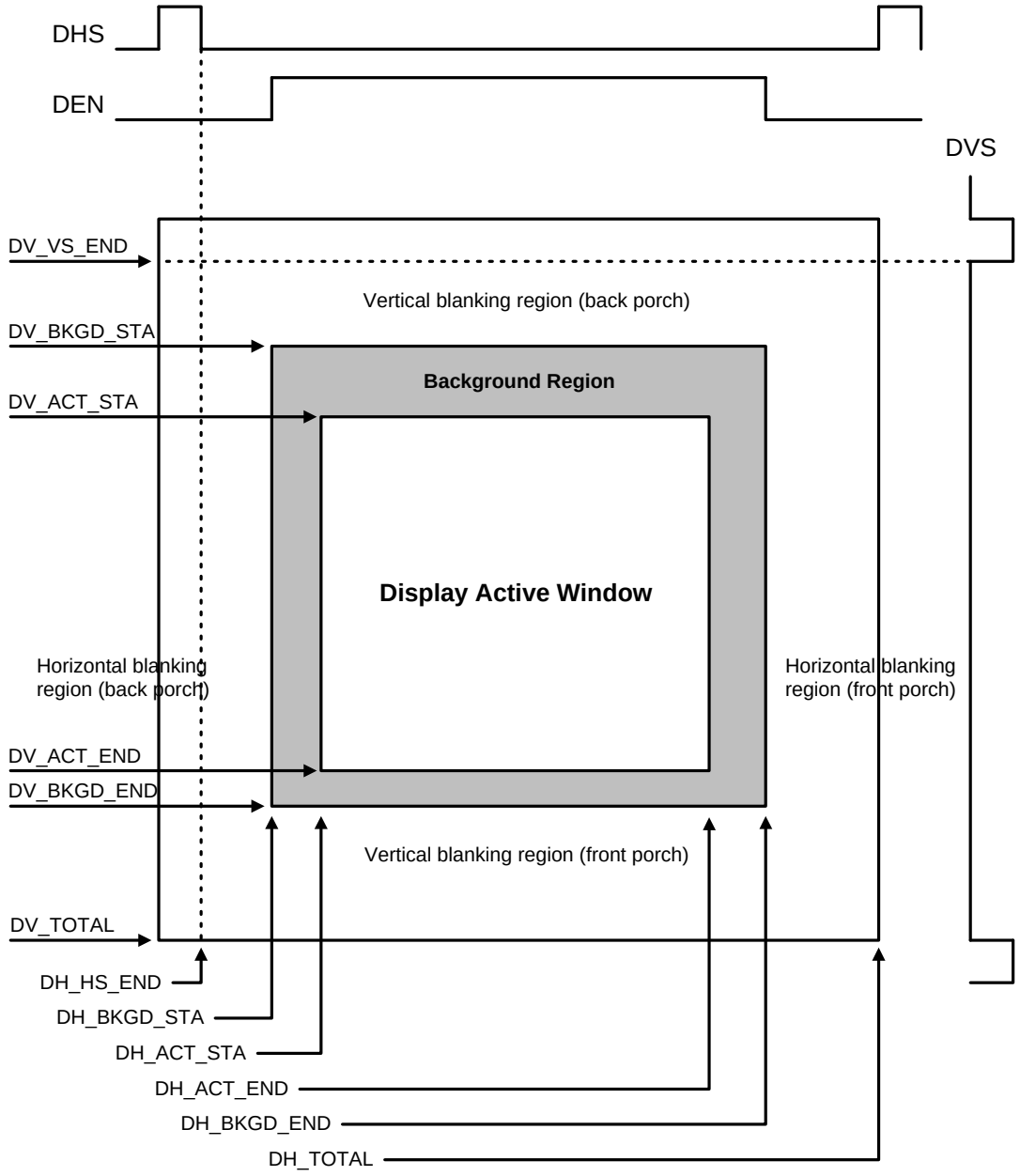


Figure 7 Display Active Window Diagram

Color Processing

Digital color R & G & B independent channel contrast & brightness controls are built in RTD2522. The contrast control is performed a multiply value from 0/128, 1/128, 2/128… to 255/128 for each R/G/B channel. The brightness control is used to set an offset value from –128 to +127 also for each R/G/B channel.

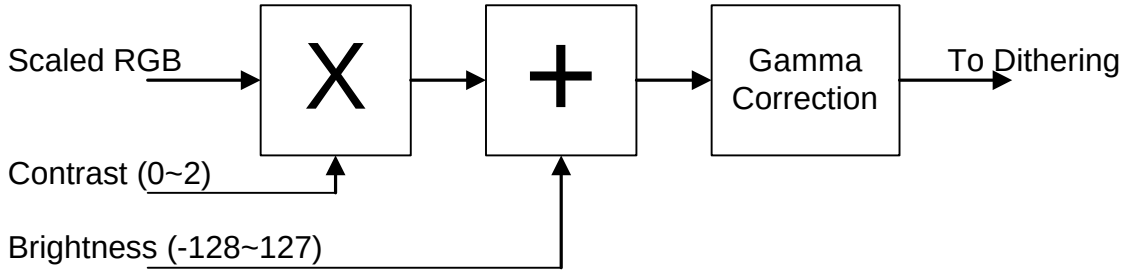


Figure 8 Brightness, Contrast & Gamma Correction block diagram

OSD & Color LUT

1.1.6 *Build-In OSD*

The detailed function-description of build-in OSD, please refer to the application note for RTD2011 embedded OSD.

1.1.7 *Color LUT & Overlay Port*

The following diagram presents the data flow among the gamma correction, dithering, overlay MUX, OSD LUT and output format conversion blocks.

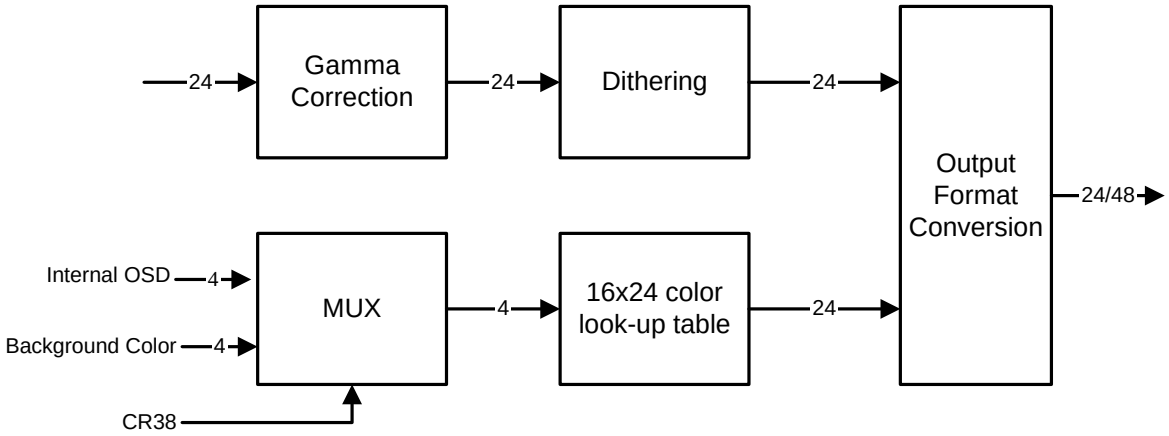


Figure 9 OSD color look-up table data path diagram

Auto-Adjustment

There are two main independent auto-adjustment functions supported by RTD2522, including auto-position & auto-tracking. The operation procedure is as following;

1.1.8 *Auto-Position*

1. Define the RGB color noise margin (7B,7C,7D): When the value of color channel R or G or B is greater than these noise margins, a valid pixel is found.
2. Define the threshold-pixel for vertical boundary search (7C[1:0]).
3. Define the boundary window of searching (75 ~ 7A) for horizontal boundary search.
4. Start auto-function (7F[0]) .
5. The result can be read from register (80 ~ 87).

1.1.9 *Auto-Tracking*

1. Setting the control-registers (7F) for the function (auto-phase, auto-balance) according to the Control-Table.
2. Define the Diff-Threshold (7E).
3. Define the boundary window of searching (75 ~ 7A) for tracking window.
4. Start auto-function (7F[0]) .
5. The result can be read from register (88 ~ 8B).

PLL System

Inside the RTD2522, there are three PLL systems for display clock and ADC sample clock.

1.1.10 *DCLK PLL*

PLL provides a wide range of user-programmable frequency synthesis options, and the formula as following; The frequency before VCO_Divide must be 50MHz~450MHz.

DCLK = Fin * DPM / DPN / VCO_Divide,

Meanwhile, Fin = 24.576MHz, the DPLL_M[7:0] & DPLL_N[5:0] are the 8-bit M & 6-bit N value of DCLK. DPM=DPLL_M[7:0]+2, DPN=DPLL_N[5:0]+2.

Of course, you can force this clock from external oscillators through pins REFCLK for your own applications.

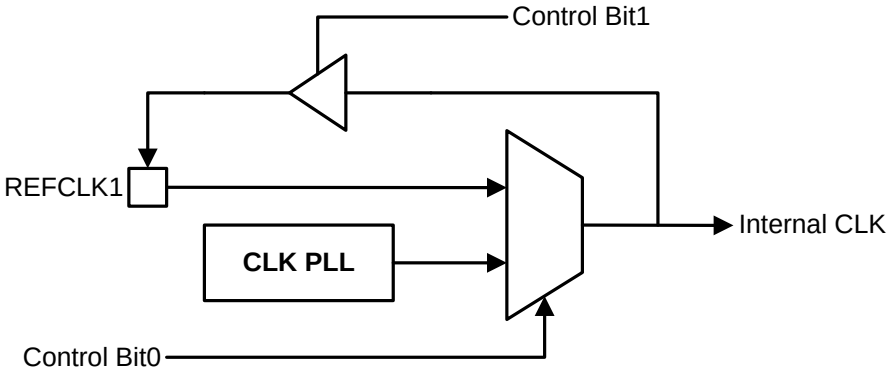
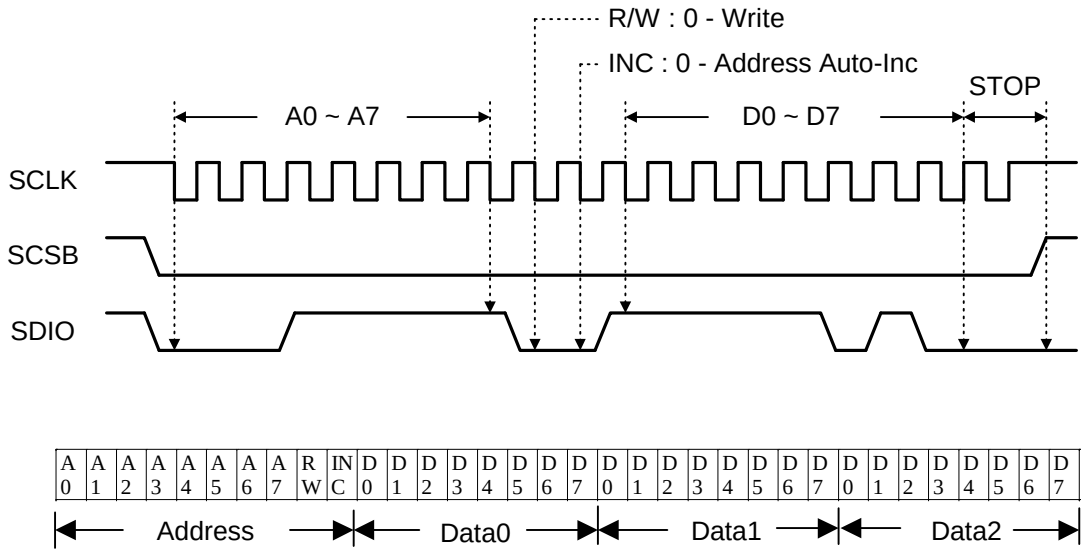


Figure 10 PLL System Control Diagram

Spread-Spectrum function is also build in DCLK to reduce EMI while using TCON. You can control the SSP_I, SSP_W, and FMDIV to fine-tune the EMI.

Host Interface

Any transaction should start from asserted the SCS# and stop after de-asserted the SCS#. Within this period, any data are driving by clock rising edge and latched by clock falling edge. The detailed timing diagrams are as following;



Address: A0~A7

R/W: Read/Write Mode for Data Phase, 0 -- Write, 1 -- Read

INC: Address Auto-Increasing Mode, 0 -- enable auto-increasing, 1 -- disable

Figure 11 Serial Port Write Timing & Data Format

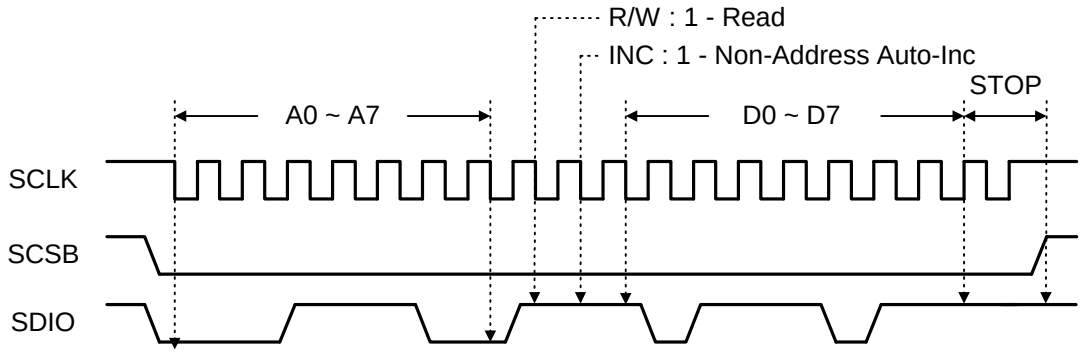


Figure 12 Serial Port Read Timing

Registers Description

Reading unimplemented registers will return 0.

Address: 00 ID_REG Default: 61h

Bit	Mode	Function
7:0	R	**MSB 4 bits: 0110** product code **LSB 4 bits: 0001** rev. code

Address: 01 STATUS (Status Register) Default: 00h

Bit	Mode	Function
7	R	**ADC_PLL Non-Lock:** If the ADC_PLL non-lock occurs, this bit is set to “1”.
6	R	**Input VSYNC Error** If the input vertical sync occurs within the programmed active period, this bit is set to “1”.
5	R	**Input HSYNC Error** If the input horizontal sync occurs within the programmed active period, this bit is set to “1”.
4	R	**Input ODD Toggle Occur** If the ODD signal(from SAV/EAV) toggle occurs, this bit is set to “1”.
3	R	**Video-8 Input Vertical Sync Occurs** If the YUV input vertical sync edge occurs, this bit is set to “1”.
2	R	**ADC Input Vertical Sync Occurs** If the RGB input vertical sync edge occurs, this bit is set to “1”.
1	R	**Input Overflow Status** (Frame Sync Mode) If an overflow in the input data capture buffer occurs, this bit is set to “1”.
0	R	**Line Buffer Underflow status** (Frame Sync Mode) If an underflow in the line-buffer occurs, this bit is set to “1”.

Write to clear status.

Address: 02 HOSTCTRL **Default: 00h**

Bit	Mode	Function
7	R	**Display Support** 0: XGA (RTD2512) 1: SXGA (RTD2522)
6:5	---	**Reserved**
4	R/W	**SOG_Mode** 0: DC-offset-circuit 1: Direct connect
3	---	**Reserved**
2	R/W	**Power Down Mode Enable** 0: Normal 1: Enable power down mode
1	R/W	**Power Saving Mode Enable** (except sync processor & serial port): 0: Normal 1: Enable power saving mode
0	R/W	**Reset Whole Chip** (Low pulse at least 8ms): 0: Normal 1: Enable reset

Address: 03 IRQ_CTRL0 (IRQ Control Register 0) **Default: 00h**

Bit	Mode	Function
7	R/W	**IRQ (ADC_PLL Non-Lock)** 0: Disable the ADC_PLL non-lock error event as an interrupt source 1: Enable the ADC_PLL non-lock error event as an interrupt source
6	R/W	**IRQ (Input VSYNC Error)** 0: Disable the Input VSYNC error event as an interrupt source 1: Enable the Input VSYNC error event as an interrupt source
5	R/W	**IRQ (Input HSYNC Error)** 0: Disable the Input HSYNC error event as an interrupt source 1: Enable the Input HSYNC error event as an interrupt source
4	R/W	**IRQ (Input ODD Toggle Occur)** 0: Disable the Input ODD toggle event as an interrupt source 1: Enable the Input ODD toggle event as an interrupt source
3	R/W	**IRQ (Video-8 Input Vertical Sync Occurs)** 0: Disable the B-port (VGB) Input VSync event as an interrupt source 1: Enable the B-port (VGB) Input VSync event as an interrupt source
2	R/W	**IRQ (ADC Input Vertical Sync Occurs)** 0: Disable the A-port (VGA) Input VSync event as an interrupt source 1: Enable the A-port (VGA) Input VSync event as an interrupt source
1	R/W	**IRQ (Input Overflow Status)** 0: Disable the Input Buffer overflow event as an interrupt source 1: Enable the Input Buffer overflow event as an interrupt source
0	R/W	**IRQ (Line Buffer Underflow status)** 0: Disable the Line Buffer underflow event as an interrupt source 1: Enable the Line Buffer underflow event as an interrupt source

Input Video Capture

a. Capture Format

Address: 04 VGIP_CTRL (Video Graphic Input Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**Vertical Scale-Down Compensation** 0: disable 1: enable
6	R/W	**Horizontal Scale-Down Compensation** 0: disable 1: enable
4:2	R/W	**Input Pixel Format** 000: From Embedded ADC 001: Reserved 010: Low Speed Input (<60MHz) from Embedded ADC 011: Video-8 from B port (8bits) 100: From Embedded TMDS 101: Reserved 110: Low Speed Input (<60MHz) from Embedded TMDS 111: Reserved
1	R/W	**Input graphic/video mode** 0: From analog input (input captured by 'Input Capture Window') 1: From digital input (captured start by 'enable signal', but sill stored in 'capture window size')
0	R/W	**Input Video Run Enable** 0: No data is transferred 1: Sampling input pixels

Address: 05 VGIP_SIGINV (Input Control Signal Inverted Register) Default: 00h

Bit	Mode	Function
7	R/W	**IVS Sync with IHS Control** 0: Enable 1: Disable
6	R/W	**Input HS Measured Source Select** 0: A/B/C port HS 1: HS_RAW/SOG
5	R/W	**Input CSYNC (HS_RAW or SOG) Inverted Enable** 0: Disable 1: Enable
4	R/W	**Input Video ODD signal invert enable(from EAV)** 0: Not inverted (ODD = positive polarity) 1: Inverted (ODD = negative polarity)
3	R/W	**Input VS Signal Polarity Inverted** 0: Not inverted (VS = positive polarity) 1: Inverted (VS = negative polarity)
2	R/W	**Input HS Signal Polarity Inverted** 0: Not inverted (HS = positive polarity) 1: Inverted (HS = negative polarity)
1	R/W	**Input ENA Signal Polarity Inverted** 0: Not inverted (input high active) 1: Inverted (while input low active)
0	R/W	**Input Clock Polarity** 0: Rising edge latched 1: Falling edge latched

b. Input Frame Window

Address: 06 IPH_ACT_STAL (Input Horizontal Active Start Low)

Bit	Mode	Function
7:0	R/W	Input Video Horizontal Active Start -- Low Byte [7:0]

Address: 07 IPH_ACT_STAH (Input Horizontal Active Start)

Bit	Mode	Function
2:0	R/W	Input Video Horizontal Active Start -- High Byte [10:8]

The number of pixel clocks from the leading edge of HS to the first pixel of the active line.
IPH_ACT_STA must bigger than 2.

Address: 08 IPH_ACT_WIDL (Input Horizontal Active Width Low)

Bit	Mode	Function
7:0	R/W	Input Video Horizontal Active Width -- Low Byte [7:0]

Address: 09 IPH_ACT_WIDH (Input Horizontal Active Width High)

Bit	Mode	Function
2:0	R/W	Input Video Horizontal Active Width – High Byte [10:8]

This register defines the number of active pixel clocks to be captured.
(Horizontal Active Start + Horizontal Active Width) < 2047
This capture width must be increments of four.

Address: 0A IPV_ACT_STAL (Input Vertical Active Start Low)

Bit	Mode	Function
7:0	R/W	Input Video Vertical Active Start – Low Byte [7:0]

Address: 0B IPV_ACT_STAH (Input Vertical Active Start High)

Bit	Mode	Function
2:0	R/W	Input Video Vertical Active Start – High Byte [10:8]

The number of lines from the leading edge of selected input video VSYNC to the first line of the active window.

Address: 0C IPV_ACT_LENL (Input Vertical Active Lines)

Bit	Mode	Function
7:0	R/W	Input Video Vertical Active Lines – Low Byte [7:0]

Address: 0D IPV_ACT_LENH (Input Vertical Active Lines)

Bit	Mode	Function
2:0	R/W	Input Video Vertical Active Lines – High Byte [10:8]

This register defines the number of active lines to be captured.

Address: 0E IRQ_CTRL1 (IRQ Control Register 1) Default: 00h

Bit	Mode	Function
7	R	This bit set to '1' indicates that the read before display SRAM is not ready
6:2	---	**Reserved.**
1	R/W	**Internal IRQ Enable:** 0: Disable these interrupt. 1: Enable these interrupt. The DDC & Status0 IRQ enable will be logically "ORed" together.
0	**---**	**Reserved**

Address: 14 INTERNAL FIELD DETECTION Default: x0h

Bit	Mode	Function
7:5	----	
4	R/W	**Video mode compensation:** 0: disable 1: enable
3	R/W	**Internal ODD-signal inverse for FS_Delay_Fine_Tuning** 0: No invert 1: Invert
2	R/W	**ODD to Control FS_Delay_Fine_Tuning** 0: Disable 1: Enable (FS_Delay_Fine_Tuning must set enable)
1	R/W	**Internal ODD-signal inverse for video-compensation** 0: No invert 1: invert
0	R/W	**Internal ODD signal selection** 0: ODD signal (from EAV) 1: Internal Field Detection ODD signal (Also support under DVI input)

Scaling Up Function

Address: 15 SCALE_CTRL (Scale Control Register) Default: 00h

Bit	Mode	Function
7:6	----	Reserved
5:4	R/W	**Vertical Filter Effect:** 00: Filter 1 01: Filter 2 10: Filter 3 11: Filter 4
3:2	R/W	**Horizontal Filter Effect:** 00: Filter 1 01: Filter 2 10: Filter 3 11: Filter 4
1	R/W	**Enable the Vertical Filter Function:** 0: By pass the vertical filter function block 1: Enable the vertical filter function block
0	R/W	**Enable the Horizontal Filter Function:** 0: By pass the horizontal filter function block 1: Enable the horizontal filter function block

Address: 16 HOR_SCA_M (Horizontal Scale Factor Medium)

Bit	Mode	Function
7:0	R/W	Bit [11:4] of horizontal scale factor

Address: 17 HOR_SCA_H (Horizontal Scale Factor High)

Bit	Mode	Function
7:0	R/W	Bit [19:12] of horizontal scale factor

This horizontal scale factor includes a 20-bit fraction part to present a horizontal scaled up size over the stream input. For example, for 800-pixel original picture scaled up to 1024-pixel, the factor should be filled in as follows:
(800/1024) x 2^20 = 0.78125 x 2^20 = 819200 = C8000h = C8h, 00h, 0h.

Address: 18 VER_SCA_M (Vertical Scale Factor Low)

Bit	Mode	Function
7:0	R/W	Bit [11:4] of vertical scale factor

Address: 19 VER_SCA_H (Vertical Scale Factor High)

Bit	Mode	Function
7:0	R/W	Bit [19:12] of vertical scale factor

This vertical scale factor includes a 20-bit fraction part to present a vertical scaled up size over the stream input. For example, for 600-line original picture scaled up to 768-line, the factor should be filled in as follows:
(600/768) x 2^20 = 0.78125 x 2^20 = 819200 = C8000h = C8h, 00h, 0h.

Address: 1A HV_SCA_L (Horizontal/Vertical Scale Factor Low)

Bit	Mode	Function
7:6	R/W	Bit [3:2] of horizontal scale factor
5:4	---	Reserved for Bit [1:0] of horizontal scale factor
3:2	R/W	Bit [3:2] of vertical scale factor
1:0	---	Reserved for Bit [1:0] of vertical scale factor

Address: 1B FILTER_CTRL0 (Filter Control Register 1) Default: C4h

Bit	Mode	Function
7:2	R/W	**Horizontal filter coefficient initial value**; default: 110001
1	R/W	**Enable user defined vertical filter coefficient table** 0: disable 1: enable
0	R/W	**Enable user defined horizontal filter coefficient table** 0: disable 1: enable

Address: 1C FILTER_CTRL1 (Filter Control Register 2) Default: C4h

Bit	Mode	Function
7:2	R/W	**Vertical filter coefficient initial value**; default: 110001
1	R/W	**Select User Defined Filter Coefficient Table for Access Channel** 0: Horizontal 1: Vertical
0	R/W	**Enable Filter Coefficient Access** 0: disable 1: enable the access channels

Address: 1D FILTER_PORT (User Defined Filter Access Port)

Bit	Mode	Function
7:0	W	Access port for user defined filter coefficient table

When enable filter coefficient accessing, the first write byte is stored into the LSB(bit[7:0]) of coefficient #1 and the second byte is into MSB (bit[8:11]). Therefore, the valid write sequence for this table is c0-LSB, c0-MSB, c1-LSB, c1-MSB, c2-LSB, c2-MSB … c63-LSB & c63-MSB, totally 64 * 2 cycles. Since the 128 taps is symmetric, we need to fill the 64-coefficient sequence into table only.

Address: 1E FS_DELAY_FINE_TUNING (Frame Sync Delay Fine Tuning) Default: 00h

Bit	Mode	Function
7:0	R/W	Frame Sync Mode Delay Fine Tune, “00” to disable

In Frame Sync Mode #1, this register [7:0] represents output VS delay fine-tuning. For example, it delays the number of (this register[7:0] * 16 + 16) input clocks.

Address: 1F STATUS1 (Status1 Register)

Bit	Mode	Function
7	R	**Line Buffer Overflow Status** 1: Line Buffer overflow has occurred since the last status read
6	R	**Line Buffer Underflow Status** 1: Line Buffer underflow has occurred since the last status read
5	R	**OENA Stop Event Status** 1: If the OENA stop event occurred since the last status read
4	R	**OENA Start Event Status** 1: If the OENA start event occurred since the last status read
3	R	**OVS Start Event Status** 1: If the OVS start event occurred since the last status read
2	R	**IENA Stop Event Status** 1: If the IENA stop event occurred since the last status read
1	R	**IENA Start Event Status** 1: If the IENA start event occurred since the last status read
0	R	**IVS Start Event Status** 1: If the IVS start event occurred since the last status read

Write to clear status.

Display Format

Address: 20 VDIS_CTRL (Video Display Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**DHS Output Format Select (only available in Frame Sync #1)** 0: The first DHS after DVS is active 1: The first DHS after DVS is inactive
6	R/W	**Display Data Output Inverse Enable** 0: Disable 1: Enable (only when data bus clamp to 0)
5	R/W	**Display Output Force to Background Color:** 0: Display output operates normally 1: Zoom Filter output is forced to the color as selected by background color
4	R/W	**Display 18 bit RGB Mode Enable:** 0: All individual output pixels are full 24-bit RGB 1: All individual output pixels are rounded to 18-bit RGB
3	R/W	**Frame Sync Mode Enable:** 0: Free running mode 1: Frame sync mode
2	R/W	**Display Video Output Pixel Double Width Enable:** 0: Single width pixels are output to the display with every DCLK cycle 1: Double width pixels are output to the display with every DCLK cycle
1	R/W	**Display Output Run Enable:** 0: DHS, DVS, DEN, DCLK & data bus are clamped to "0" 1: Display output normal operation.
0	R/W	**Display Video Timing Run Enable:** 0: Display Timing Generator is halted, Zoom Filter halted 1: Display Timing Generator and Zoom Filter enabled to run normally

Step to disable output: First set CR20_1=0, set CR20_6 & inverse control, then set CR20_0=0 to disable output.

Address: 21 VDIS_SIGINV (Display Control Signal Inverted) Default: 00h

Bit	Mode	Function
7:4	R/W	**Background color select [3:0]** Select one color from 16 look-up-table
3	R/W	**Display Vertical Sync (DVS) Output Invert Enable:** 0: Display Vertical Sync output normal active high logic 1: Display Vertical Sync output inverted logic
2	R/W	**Display Horizontal Sync (DHS) Output Invert Enable:** 0: Display Horizontal Sync output normal active high logic 1: Display Horizontal Sync output inverted logic
1	R/W	**Display Data Enable (DEN) Output Invert Enable:** 0: Display Data Enable output normal active high logic 1: Display Data Enable output inverted logic
0	R/W	**Reserved**

Address: 22 DH_TOTAL (Display Horizontal Total Pixels)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Total Pixel Clocks:** Low Byte[7:0]

Address: 23 DH_TOTAL (Display Horizontal Total Pixels)

Bit	Mode	Function
7:3	---	Reserved
2:0	R/W	**Display Horizontal Total Pixel Clocks**: High Byte[10:8]

Determines the number of DCLK cycles in each display line minus 2. (DHS leading edge to DHS leading edge)

Address: 24 DH_HS_END (Display Horizontal Sync End)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Sync End:** Determines the width of DHS pulse in DCLK cycles

Address: 25 DH_BKGD_STA (Display Horizontal Background Start)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background Start**: Low Byte [7:0]

Address: 26 DH_BKGD_STA (Display Horizontal Background Start)

Bit	Mode	Function
7:3	R	The Width Bit [4:0] of Last Line Before Sync in Frame Sync Mode 1
2:0	R/W	**Display Horizontal Background Start**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Background region.

Address: 27 DH_ACT_STA (Display Horizontal Active Start)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active Region Start**: Low Byte [7:0]

Address: 28 DH_ACT_STA (Display Horizontal Active Start)

Bit	Mode	Function
2:0	R/W	**Display Horizontal Active Region Start**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Active region.

Address: 29 DH_ACT_END (Display Horizontal Active End)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active Width**: Low Byte [7:0]

Address: 2A DH_ACT_END (Display Horizontal Active End)

Bit	Mode	Function
2:0	R/W	**Display Horizontal Active Width**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to the pixel of background region.

Address: 2B DH_BKGD_END (Display Horizontal Background End)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background end**: Low Byte [7:0]

Address: 2C DH_BKGD_END (Display Horizontal Background End)

Bit	Mode	Function
7:3	R	The Width Bit [9:5] of Last Line Before Sync in Frame Sync Mode 1
2:0	R/W	**Display Horizontal Background end**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to the start of horizontal blanking. REG_2C[7:3] &REG_26[7:3] indicates the width (counted by two pixel) of last line before VSYNC in frame sync mode 1.

Address: 2D DV_TOTAL (Display Vertical Total Lines)

Bit	Mode	Function
7:0	R/W	**Display Vertical Total:** Low Byte [7:0]

Address: 2E DV_TOTAL (Display Vertical Total Lines)

Bit	Mode	Function
7:3	R/W	**Frame Sync Mode Fine Tune:** Reference 0x31[4] setting
2:0	R/W	**Display Vertical Total**: High Byte [10:8]

In FreeRun mode, Display Vertical Total represents the number of DHS in a frame. In framesync mode, when the line number of Display HS is equal to Display Vertical Total, a status CR3D_7 is set.

Address: 2F DV_VS_END (Display Vertical Sync End)

Bit	Mode	Function
7:0	R/W	**Display Vertical Sync End:** Determines the duration of DVS pulse in lines

Address: 30 DV_BKGD_STA (Display Vertical Background Start)

Bit	Mode	Function
7:0	R/W	**Display Vertical Background Start:** Low Byte [7:0]

Address: 31 DV_BKGD_STA (Display Vertical Background Start) Default: 00h

Bit	Mode	Function
7	R/W	Auto switch when the line number of Display HS is equal to Display Vertical Total 0: Disable 1: Enable
6	R/W	Auto switch to (for timing) 0: Disable 1: Free Run
5	R/W	Auto switch to (for data) 0: Disable 1: Background
4	R/W	Fine Tune Delay Mode Select 0: 0/32 -- 2/32 -- 4/32 -- 6 /32 ~~~ 62/32 1: 0/32 -- 4/32 -- 8/32 --12/32 ~~~ 124/32
3	---	Reserved
2:0	R/W	**Display Vertical Background Start:** High Byte [10:8]

Determines the number of lines from leading edge of DVS to first line of background region.

Address: 32 DV_ACT_STA (Display Vertical Active Start)

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region Start:** Low Byte [7:0]

Address: 33 DV_ACT_STA (Display Vertical Active Start)

Bit	Mode	Function
2:0	R/W	**Display Vertical Active Region Start:** High Byte [10:8]

Determines the number of lines from leading edge of DVS to first line of active region.

Address: 34 DV_ACT_END (Display Vertical Active End)

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region End**: Low Byte [7:0]

Address: 35 DV_ACT_END (Display Vertical Active End)

Bit	Mode	Function
2:0	R/W	**Display Vertical Active Region End:** High Byte [10:8]

Determines the number of lines from leading edge of DVS to the line of follow background region.

Address: 36 DV_BKGD_END (Display Vertical Background End)

Bit	Mode	Function
7:0	R/W	**Display Vertical Background end:** Low Byte [7:0]

Address: 37 DV_BKGD_END (Display Vertical Background End)

Bit	Mode	Function
2:0	R/W	**Display Vertical Background end:** High Byte [10:8]

Determines the number of lines from leading edge of DVS to the line of start of vertical blanking.

Address: 38 IV_DV_LINES (IVS to DVS Lines)

Bit	Mode	Function
7:0	R/W	**IVS to DVS Lines:** (Only for FrameSync Mode) The number of input HS from input VS to output VS.

YUV-to-RGB Control

Address: 39 YUV2RGB (YUV to RGB Control Register) Default: 00h

Bit	Mode	Function
7	R/W	SRGB Enable
6	R/W	**YUV-to-RGB Conversion Mode Selection:** 0: YUV422 1: YUV444
5	R/W	**Enable YUV to RGB Conversion:** 0: Disable YVB-to-RGB conversion 1: Enable YUV-to-RGB conversion
4	R/W	SRGB SRAM Control
3:2	R/W	SRGB Coefficient Write Enable 00: Disable 01: R port 10: G port 11: B port

Address: 3A DIS_TIMING (Display Clock Fine Tuning Register) Default: 00h

Bit	Mode	Function
6	R/W	**Internal OSD Port Latch Clock Delay** 0: normal 1: 1ns delay
5	R/W	**Force Display Timing Generator Enable:** 0: wait for input VS trigger 1: force enable
4	---	Reserved
3	R/W	**Display Output Clock Coarse Tuning Control:** 0: Disable 1: 8ns delay
2:0	R/W	**Display Output Clock Fine Tuning Control:** 000: DCLK rising edge correspondents with output display data 001: 1ns delay 010: 2ns delay 011: 3ns delay 100: 4ns delay 101: 5ns delay 110: 6ns delay 111: 7ns delay

Address: 3B DIS_TIMING (Display Clock Fine Tuning Register) Default: 00h

Bit	Mode	Function
7	---	**Reserved**
5:4	R/W	**DPLL Output Select** 00: Select the internal PLL clock source as DPLL output (PWM1 output to REFCLK) 01: Select the external REFCLK1 clock source as DPLL output 10: Select the internal PLL clock source as DPLL & REFCLK1 output 11: Select the internal PLL clock source as DPLL output (Video odd/even from EAV output to REFCLK)
3	R/W	**DCLK Polarity Inverted** 0: Non-Inverted 1: Inverted
2	R/W	**DCLK Output Enable** 0: Disable 1: Enable

Address: 3C PE_CTRL Default: 00h

Bit	Mode	Function
7	R/W	**DDS Tracking Edge** 0: HS positive edge 1: HS negative edge
6	R/W	**PE Measure Enable** 0: Disable 1: Enable PE Measurement, clear after finish.
4:0	R	**PE Value**

Address: 3D Status **Default: 00h**

Bit	Mode	Function
7	R	The line number of Display HS is equal to Display Vertical Total, this bit is set to "1". Write to clear status.
6	W	**PE Max. Measure Clear** 0: clear after finish 1: write '1' to clear PE Max. Value
5	R/W	**PE Max. Measure Enable** 0: Disable 1: Enable PE Max. Measurement
4:0	R/W	**PE Max Value**

Address: 3E DUTY_FINE_TUNE

Bit	Mode	Function
7:4	R/W	**Internal Display Clock (IDCLK) Duty Fine-tune:** (3F_bit1 to enable) 1111 (min fine-tune) → 1110 → 1100 → 1000 → 0000 (max fine-tune)
3:0	R/W	**Color Processing Clock (CPCLK) Duty Fine-tune:** (3F_bit2 to enable) 1111 (min fine-tune) → 1110 → 1100 →1000 →0000 (max fine-tune)

Address: 3F DUTY_FINE_TUNE_CTRL

Bit	Mode	Function
3	R/W	**Internal Display Clock (IDCLK) Delay Enable:** 0: Disable. 1: Enable IDCLK delay.
2	R/W	**Color Processing Clock (CPCLK) Duty Fine-tune Enable:** 0: Disable. 1: Enable CPCLK duty fine-tune (setting in 3E_bit3:0)
1	R/W	**Internal Display Clock (IDCLK) Duty Fine-tune Enable:** 0: Disable. 1: Enable IDCLK duty fine-tuner (setting in 3E_bit7:4)
0	R/W	**Internal Display Clock (IDCLK) Invert.** 0: Disable 1: IDCLK invert enable.

FIFO Display Window

Address: 40 DRWL_BSU (Display Read Pixel Low Byte Before Scaling-Up)

Bit	Mode	Function
7:0	R/W	**Display window read width before scaling up:** Low Byte [7:0]

Address: 41 DRWH_BSU (Display Read Pixel High Byte Before Scaling-Up)

Bit	Mode	Function
2:0	R/W	**Display window read width before scaling up:** High Byte [10:8]

Address: 42 DRLL_BSU (Display Read Length Low Byte Before Scaling-Up)

Bit	Mode	Function
7:0	R/W	**Display window read length before scaling up:** Low Byte [7:0]

Address: 43 DRLH_BSU (Display Read Length High Byte Before Scaling-Up)

Bit	Mode	Function
2:0	R/W	**Display window read length before scaling up:** High Byte [10:8]

Address: 44 sRGB

Bit	Mode	Function
7:0	W	When R-port coefficient: RG0, RB0, RG1, RB1, …RG31, RB31, When G-port coefficient: GR0, GB0, GR1, GB1, …GR31, GB31, When B-port coefficient: BR0, BG0, BR1, BG1, …BR31, BG31 total 64 bytes (2's complement : -128~127)

Address: 45 sRGB R-Offset

Bit	Mode	Function
5:0	W	(2's complement : -32~31)

Address: 46 sRGB G-Offset

Bit	Mode	Function
5:0	W	(2's complement : -32~31)

Address: 47 sRGB B-Offset

Bit	Mode	Function
5:0	W	(2's complement : -32~31)

Address: 48 EVENT_STATUS_CONTROL Default: 00h

Bit	Mode	Function
7	R/W	Enable Vertical Line Comapre Function 0: Disable 1: Enable
6	R/W	Gating Vertical Line Compare Function to IRQ
5	R	Vertical Line Compare Status (for Polling)
4	R/W	Select Compare Source: 0: Input Side 1: Display Side
3	--	Reserved
2:0	R/W	Select Veritcal Line --Low Byte [2:0]

Write to clear

Address: 49 EVENT_LOCATION Default: 00h

Bit	Mode	Function
7:0	R/W	Select Veritcal Line --High Byte [11:3]

SYNC Processor

Address: 4A SYNC_CTRL (Only for RTD252x) Default: 00h

Bit	Mode	Function
7	R/W	**IRQ Enable** 0: Disable input sync signal edge occurs as an interrupt source 1: Enable input sync signal edge occurs as an interrupt source
6	R	**SOG Edge Occurs** If the SOG edge occurs, this bit is set to "1".
5	R	**ADC Input Horzonital Sync Occurs (HS_RAW)** If the ADC input horizontal sync edge occurs, this bit is set to "1".
4	R	**Video-8 Input Horzonital Sync Occurs** If the Video-8 input horizontal sync edge occurs, this bit is set to "1".
3:2	---	**Reserved**
1:0	R/W	**Measure Hsync/Vsync Source Select:** 00: RTD300x/RTD20xx Orignal Configuration 01: HS_RAW / AVS 10: Video-8 Hsync / Video-8 Vsync 11: TMDS Hsync / TMDS Vsync

Write to clear status.

Address: 4B SYNC_CTRL (SYNC Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**COAST Signal Invert Enable:** 0: not inverted 1: inverted
6	R/W	**COAST Signal Output Enable:** 0: disable; 1: enable;
5	R/W	**HS_OUT Signal Invert Enable:** 0: not inverted 1: inverted
4	R/W	**HS_OUT Signal Output Enable:** 0: disable; 1: enable;
3	R/W	**CLAMP Signal Invert Enable:** 0: not inverted 1: inverted
2	R/W	**CLAMP Signal Output Enable:** 0: Disable; 1: Enable
1	R/W	**Sync-On-Green Enable:** 0: Disable; 1: Enable (set "1" to Sync-Mode-Select at the same time)
0	R/W	**Sync Mode Select:** 0: Separate H & V; 1: Composite Sync from HSYNC or Green

Address: 4C SYNC_POR (H & V SYNC Polarity Measured Result) Default: 00h

Bit	Mode	Function
7	R/W	**Safe Mode** 0: Normal 1: Safe Mode Enable, mask 1 of 2 IVS.
5	R/W	**Select HS_OUT Source Signal** 0: Bypass HS_RAW 1: Select De-Composite HS out (In Composite mode)

3	R	**Input VSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
2	R	**Input HSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
1	R/W	**Start a HS & VS period / H & V resolution & polarity measurement** 0: disable to start a measurement 1: enable to start a measurement, cleared after finished
0	R/W	**HSYNC & VSYNC Measured Mode** 0: HS period counted by crystal clock & VS period counted by HS 1: H resolution counted by input clock & V resolution counted by ENA (Get the correct resolution which is triggered by enable signal, ENA)

Address: 4D MEAS_HS_PER (HSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	**Input HSYNC Period Measurement Result:** Low Byte[7:0]

Address: 4E MEAS_HS_PER (HSYNC Period Measured Result)

Bit	Mode	Function
7	R	**Input HSYNC Period Measurement Result:** Over-flow bit 1: Over-flow occurred
6	R/W	**ODD invert for ODD-Controlled-IVS_delay.** 0: Disable 1: Invert
5	R/W	**ODD-Controlled-IVS_delay Enable** 0: Disable 1: Enable
4	R/W	**Input HSYNC Synchronize Edge** 0: Input HSYNC is synchronized by the positive edge of the input clock 1: Input HSYNC is synchronized by the negative edge of the input clock
3:0	R	**Input HSYNC Period Measurement Result:** High Byte[11:8]

This result is expressed in terms of crystal clocks. When measured digitally, the result is expressed as the number of input clocks between 2 input HS signals divided by 2.

Address: 4F MEAS_VS_PER (VSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	**Input VSYNC Period Measurement Result:** Low Byte[7:0]

Address: 50 MEAS_VS_PER (VSYNC Period Measured Result)

Bit	Mode	Function
7	R	**Input VSYNC Period Measurement Result:** Over-flow bit 1: Over-flow occurred
6	R	**Internal Field Detection ODD toggle happen**
5:4	R	**The number of input HS between 2 input VS**. LSB bit [1:0]
3	---	Reserved
2:0	R	**Input VSYNC Period Measurement Result:** High Byte[10:8]

This result is expressed in terms of input HS pulses. When measured digitally, the result is expressed as the number of input enable signal within a frame.

Address: 51 MEAS_HS_HI (HSYNC High Period Measured Result)

Bit	Mode	Function
7:0	R	**Input HSYNC Period Measurement Result:** Low Byte[7:0]

Address: 52 MEAS_HS_HI (HSYNC High Period Measured Result) Default: 8'b00xx_xxxx

Bit	Mode	Function
7	R/W	**HS Recovery in Coast** 0: Disable 1: Enable (can turn on when CS or SOG)
6	R/W	**HSYNC Synchronize source** 0: Input HS 1: Feedback HS
3:0	R	**Input HSYNC Period Measurement Result:** High Byte[11:8]

This result is expressed in terms of crystal clocks. When measured digitally, the result is expressed as the number of input clocks inside the input enable signal divided by 2.

Address: 53 MEAS_VS_HI (VSYNC High Period Measured Result)

Bit	Mode	Function
7:0	R	**Input VSYNC Period Measurement Result:** Low Byte[7:0]

Address: 54 MEAS_VS_HI (VSYNC High Period Measured Result)

Bit	Mode	Function
7	R	6-iclk-delay HS level latched by VS rising edge

6	R	HS level latched by VS rising edge
5	R	HS level latched by 6-iclk-delay VS rising edge
4	R/W	**Feedback HSYNC Synchronize Edge** 0: Feedback HSYNC is synchronized by the positive edge of the input clock 1: Feedback HSYNC is synchronized by the negative edge of the input clock
3	R	**VSYNC Synchronize Edge** 0: latch VS by the positive edge of input HSYNC 1: latch VS by the negative edge of input HSYNC
2:0	R	**Input VSYNC Period Measurement Result:** High Byte[10:8]

This result is expressed in terms of input HS pulses

Clamping Signal Control

Address: 55 CLAMP_START (Clamp Signal Output Start)

Bit	Mode	Function
7:0	R/W	**Start of Output Clamp Signal Pulse:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.

Address: 56 CLAMP_END (Clamp Signal Output End)

Bit	Mode	Function
7:0	R/W	**End of Output Clamp Signal Pulse:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal.

Color Processor Control

Address: 5D COLOR_CTRL (Color Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**Dithering Frame Modulation New Function** 0: original dithering function setting When 0x5D[6]='1', dithering frame modulation with modulus=2 1: dithering frame modulation with modulus=4
6	R/W	**Dithering Frame Modulation Function:** 0: disable 1: enable dithering frame modulation
5	R/W	**Enable Access Channel for Dithering Table:** 0: disable this channel 1: enable this channel (address should not auto increase)
4	R/W	**Enable Access Channels for Gamma Correction Coefficient:** 0: disable these channels 1: enable these channels (address should not auto increase)
3	R/W	**Enable Dithering Function:** 0: disable the dithering function 1: enable the dithering function
2	R/W	**Enable Look-Up Table for Gamma Correction Coefficient:** 0: disable the look-up table 1: enable the look-up table coefficient
1	R/W	**Enable Contrast Control Coefficient:** 0: disable the coefficient 1: enable the coefficient
0	R/W	**Enable Brightness Control Coefficient:** 0: disable the coefficient 1: enable the coefficient

Brightness Coefficient:

Address: 5E BRI_R_COE (Brightness Red Coefficient)

Bit	Mode	Function
7:0	W	**Brightness Red Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 5F BRI_G_COE (Brightness Green Coefficient)

Bit	Mode	Function
7:0	W	**Brightness Green Coefficient: Valid range:** -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 60 BRI_B_COE (Brightness Blue Coefficient)

Bit	Mode	Function
7:0	W	**Brightness Blue Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Contrast Coefficient:

Address: 61 CTS_R_COE (Contrast Red Coefficient)

Bit	Mode	Function
7:0	W	**Contrast Red Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 62 CTS_G_COE (Contrast Green Coefficient)

Bit	Mode	Function
7:0	W	**Contrast Green Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 63 CTS_B_COE (Contrast Blue Coefficient)

Bit	Mode	Function
7:0	W	**Contrast Blue Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Gamma Correction :

Address: 64 RED_GAMMA_PORT (Red Gamma Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for red gamma correction table**

Address: 65 GRN_GAMMA_PORT (Green Gamma Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for green gamma correction table**

Address: 66 BLU_GAMMA_PORT (Blue Gamma Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for blue gamma correction table**

When enable gamma correction table accessing, total size of coefficient table is 256 bytes for each color respectively. And the input data sequence is c0, c1, c2, … c255.

Dithering Coefficient:

Address: 67 DITHER_PORT (Dithering Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for dithering table**

When enable dithering table accessing, total size of coefficient table is 16 * 4 bits for RGB color. And the input data sequence is {c1, c0}, {c3, c2}, … {c15, c14}. Default table: { (2,3,1,0), (1,0,2,3), (3,2,0,1), (0,1,3,2) }

Cyclic-Redundant-Check

Address: 68 OP_CRC_CTRL (Output CRC Control Register) Default: FCh

Bit	Mode	Function
7:2	R/W	**SRAM Control //111111 (F, I, A, M, G, C)** F (bit 7): four-line sram I (bit 6): input sram A (bit 5): OSD attribute sram M (bit 4): OSD font map sram G (bit 3): Gamma, Dithering table sram C (bit 2): filter coefficient sram
1	R/W	**Enable Full Line buffer:** 0: Disable 1: Enable
0	R/W	**Output CRC Control:** 0: Stop or finish (Auto-stop after checked a completed display frame) 1: Start

CRC function = X^24 + X^7 + X^2 + X + 1.

Address: 69 OP_CRC_BYTE_0 (Output CRC Checksum Byte 0)

Bit	Mode	Function
7:0	R	Output CRC-24 bit 7~0

Address: 6A OP _CRC_BYTE_1 (Output CRC Checksum Byte 1)

Bit	Mode	Function
7:0	R	Output CRC-24 bit 15~8

Address: 6B OP _CRC_BYTE_2 (Output CRC Checksum Byte 2)

Bit	Mode	Function
7:0	R	Output CRC-24 bit 23~16

Display Pattern Generator

Address: 6C Pattern Generator **Default: 00h**

Bit	Mode	Function
7:6	R/W	**Chess Board Period** 00: 1-line toggle 01: 2-line toggle 10: 4-line toggle 11: no define
5	R/W	**Chess Board Enable** 0: Disable 1: Enable (BGCS[2:0] will toggle every Chess-Board-Period line, combining with Horizontal-Periodic-Line or Grid can produce Chess-Board)
4	R/W	**Flag Enable** 0: Disable 1: Enable (Vertical-Background-Start from 0x80, the 1st 256 lines will display only Red-color, the 2nd 256 lines will display only Green-color, the 3rd 256 lines will only display Blue-color, the 4th 256 lines will display Whole color)
3:1	R/W	**Mode Selection** **000: Horizontal-Gray-Bar** Horizontal-Background-Start from 0x40, BGCS[3:0] increases every 64-pixels. **001: Vertical-Gray-Bar** Vertical-Background-Start from 0x40, BGCS[3:0] increases every 64-lines. **010: Horizontal-Periodic-Line** The Nth-pixel will show the color BGCS[3:0]=(N mod 16). **011: Vertical-Period-Line** The Nth-line will show the color BGCS[3:0]=(N mod 16). **1xx: Grid** Background-Start from times of 16/32/64/128 pixels/lines, if BGCS[1xxx] is border-color, 16-Grid pattern is generated; if BGCS[1xx1] is border-color, 32-Grid pattern is generated; (vertical broken-line) if BGCS[1x11] is border-color, 64-Grid pattern is generated; (vertical broken-line) if BGCS[1111] is border-color, 128-Grid pattern is generated. (vertical broken-line) BGCS[0xxx] is same with Horizontal-Period_Line but only 3-bit (N mod 8).
0	R/W	**Test Pattern Enable:** 0: Disable 1: Enable

BackGround-Color-Select: BGCS[3:0] is the “bit-inverse” index of color from Overlay Color LUT.

Setting Guide:

1. Display can set “Force-to-background” or not, if not
2. Display background window sets to panel display size.
3. Display active window setting must be outside of DH_TOTAL, DV_TOTAL.
4. Set color-LUT of BGCS[3:0] and Test-Pattern-Generator register.

Overlay Control

Address: 6D OVL_CTRL (Overlay Display Control Register) Default: 00h

Bit	Mode	Function
7:6	R/W	**Alpha-blending(for OSD):** 00: Disable 01: 1/4 10: 1/8 11: 1/16
5	R/W	**Display Even/Odd Data Swap:** 0: Disable 1: Enable
4	R/W	**Display Red/Blue Data Swap** 0: Disable 1: Enable
3	R/W	**Display MSB/LSB Data Swap** 0: Disable 1: Enable
2	R/W	**Skew Data Output** 0: Non-skew data output 1: Skew data output
1	R/W	**Overlay Sampling Mode Select:** 0: dual pixels per clock 1: single pixel per clock
0	R/W	**Overlay Port Enable:** 0: Disable 1: Enable

Note: While you turn on the alpha-blending function, should also modify the window color & window shadow color inside look-up-table.

Address: 6E OVL_LUT_ADDR (Overlay LUT Address) Default: 00h

Bit	Mode	Function
7	R/W	**Enable Overlay Color Plate Access:** 0: Disable 1: Enable
6	---	Reserved
5:0	R/W	**Overlay 16x24 Look-Up-Table Write Address [5:0]**

Auto-increment while every accessing “Overlay LUT Access Port”.

Address: 6F OVL_LUT_PORT (Overlay LUT Access Port)

Bit	Mode	Function
7:0	W	**Overlay 16x24 Look-Up-Table access port [7:0]**

Using this port to access overlay color plate which addressing by the above register.
The writing sequence into LUT is {R0, G0, B0, R1, G1, B1,… R15, G15, B15} and the address counter will be automatic increment and circular from 0 to 47.

Scale Down Control

Address: 70 SCALE_DOWN_CTRL (Scale Down Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**Video 8 Port Input Latch Bus MSB to LSB Swap Control:** 0: normal 1: Switched Video8 port MSB to LSB sequence into LSB to MSB
6	R/W	Default='0'. When set to '1', vertical scale down is disable in scale down mode
5	R/W	**Internal ENA (I_ENA) Delay Control:** 0: normal; 1: 2ns delay;
4	R/W	**Internal VS (I_VS) Delay Control:** 0: normal; 1: 2ns delay;
3	R/W	**Internal HS (I_HS) Delay Control:** 0: normal; 1: 2ns delay;
2:1	R/W	**Input Clock Delay Control:** 00: Normal 01: 1ns delay 10: 2ns delay 11: 3ns delay
0	R/W	**Scale down function enable:** 0: disable scale down function 1: enable scale down function

Address: 71 H_SCALE_DL (Horizontal scale down factor register)

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor:** Low Byte [7:0]

Address: 72 H_SCALE_DH (Horizontal scale down factor register)

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor:** High Byte [15:8]

Registers { H_SCALE_DH, H_SCALE_DL} = (Xi / Xm) x (2^12) truncate. If not truncate, fill minus 1.
Meanwhile, Xi = horizontal input width; Xm = horizontal memory write width

Address: 73 V_SCALE_DL (Vertical scale down factor register)

Bit	Mode	Function
7:0	R/W	**Vertical Scale Down Factor:** Low Byte [7:0]

Address: 74 V_SCALE_DH (Vertical scale down factor register)

Bit	Mode	Function
7:0	R/W	**Vertical Scale Down Factor:** High Byte [15:8]

Registers { V_SCALE_DH, V_SCALE_DL} = (Yi / Ym) x (2^12) truncate. If not truncate, fill minus 1
Meanwhile, Yi = vertical input width; Ym = vertical memory write width

Image Auto Function

Address: 75 H_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary Start:** Low Byte [7:0]

Address: 76 H_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary End:** Low Byte [7:0]

Address: 77 H_BOUNDARY_HIGH Default: 8'b0xxx_xxxx

Bit	Mode	Function
7	R/W	**Field_Select_Enable:** Auto-Function only active when Even or Odd field. 0: Disable 1: Enable
6:4	R/W	**Horizontal Boundary Start:** High Byte [10:8] //11-bit=2048
3:0	R/W	**Horizontal Boundary End:** High Byte [11:8] //12-bit=4096

Address: 78 V_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	**Vertical Boundary Start:** Low Byte [7:0] //(Invalid when Vertical Auto-Boundary)

Address: 79 V_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	**Vertical Boundary End:** Low Byte [7:0] //(Invalid when Vertical Auto-Boundary)

Address: 7A V_BOUNDARY_HIGH Default: 8'b0xxx_xxxx

Bit	Mode	Function
7	R/W	**Field_Select:** Select Even or Odd field. Active when **Field_Select_Enable**. 0: Active when ODD signal is "0" 1: Active when ODD signal is "1"
6:4	R/W	**Vertical Boundary Start:** High Byte [10:8] //11-bit //(Invalid when Vertical Auto-Boundary)
3:0	R/W	**Vertical Boundary End:** High Byte [11:8] //12-bit //(Invalid when Vertical Auto-Boundary)

Address: 7B RED_NOISE_MARGIN (Red Noise Margin Register) Default: 8'bxxxxxx00

Bit	Mode	Function
7:2	R/W	**Red pixel noise margin setting register**
1	R/W	Even or Odd pixel be measured 0: Even 1: Odd
0	R/W	Measure only Even or Odd pixel enable 0: Disable 1: Enable

Address: 7C GRN_NOISE_MARGIN (Green Noise Margin Register) Default: 8'bxxxxxx00

Bit	Mode	Function
7:2	R/W	**Green pixel noise margin setting register**
1:0	R/W	**Vertical boundary search:** 00: 1 pixel over threshold; 01: 2 pixel over threshold 10: 4 pixel over threshold; 11: 8 pixel over threshold

Address: 7D BLU_NOISE_MARGIN (Blue Noise Margin Register) Default: 8'bxxxxxx00

Bit	Mode	Function
7:2	R/W	**Blue pixel noise margin setting register**
1:0	R/W	**Color Source Select for Detection:** 00: B color 01: G color 10: R color

Address: 7E DIFF_THRESHOLD

Bit	Mode	Function
7:0	R/W	**Difference Threshold**

Address: 7F AUTO_ADJ_CTRL (Auto adjustment control register) Default: 00h

Bit	Mode	Function
7	R/W	Measure Digital Enable Info when boundary search active 0: Normal Boundary Search 1: Digital Enable Info Boundary Search. (The vertical & horizontal, start & end information of external digital signal can be obtained from CR80~87).
6	R/W	**Accumulation Type** 0: Type1 1: Type2
5	R/W	**Color Max or Min Measured Select:** 0: MIN color measured (Only when Balance-Mode, result must be complemented) 1: MAX color measured
4	R/W	**Accumulation or Compare Mode** 0: Compare Mode 1: Accumulation Mode
3:2	R/W	Mode Selection (00 is forbidden) 01: Mode1 10: Mode2 11: Mode3
1	R/W	**Function (Phase/Balance) Selection** 0: Auto-Balance 1: Auto-Phase
0	R/W	**Start Auto-Function Tracking Function:** 0: stop or finished 1: start

Control Table/ Function	Sub-Function	7F.6	7F.5	7F.4	7F.3	7F.2	7F.1	7E
Auto-Balance	**Max pixel**	X	1	0	0	X	0	X
	Min pixel	X	0	0	0	X	0	X
Auto-Phase Type1	**Mode1**	0	1	1	0	1	1	Th
	Mode2	0	1	1	1	0	1	Th
	Mode3	0	1	1	1	1	1	Th
Auto-Phase Type2	**Mode1**	1	1	1	0	1	1	Th
	Mode2	1	1	1	1	0	1	Th
	Mode3	1	1	1	1	1	1	Th
Accumulation	**All pixel**	1	1	1	0	1	0	0

Table 1 Auto-Tracking Control Table

Address: 80 VER_START_L (Active region vertical start Register)

Bit	Mode	Function
7:0	R	**Active region vertical start measurement result:** bit[7:0]

Address: 81 VER_START_H (Active region vertical start Register)

Bit	Mode	Function
3:0	R	**Active region vertical start measurement result:** bit[11:8]

Address: 82 VER_END_L (Active region vertical end Register)

Bit	Mode	Function
7:0	R	**Active region vertical end measurement result:** bit[7:0]

Address: 83 VER_END_H (Active region vertical end Register)

Bit	Mode	Function
3:0	R	**Active region vertical end measurement result:** bit[11:8]

Address: 84 HOR_START_L (Active region horizontal start Register)

Bit	Mode	Function

7:0	R	**Active region horizontal start measurement result:** bit[7:0]

Address: 85 HOR_START_H (Active region horizontal start Register)

Bit	Mode	Function
3:0	R	**Active region horizontal start measurement result:** bit[11:8]

Address: 86 HOR_END_L (Active region horizontal end Register)

Bit	Mode	Function
7:0	R	**Active region horizontal end measurement result:** bit[7:0]

Address: 87 HOR_END_H (Active region horizontal end Register)

Bit	Mode	Function
3:0	R	**Active region horizontal end measurement result:** bit[11:8]

Address: 88 AUTO_PHASE_0 (Auto phase result byte0 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[7:0] / The measured value of R or G or B color max or min. (Auto-Balance)

Address: 89 AUTO_PHASE_1 (Auto phase result byte1 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[15:8]

Address: 8A AUTO_PHASE_2 (Auto phase result byte2 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[23:16]

Address: 8B AUTO_PHASE_3 (Auto phase result byte3 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[31:24]

Address: 8C IVS_DELAY (Internal Input-VS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W	Input VS delay count by Input HS to reset input data

Address: 8D IHS_DELAY (Internal Input-HS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W	Input HS delay count by Input clock

Address: 8E ODD_CTRL (ODD Source Control Register) Default: 00h

Bit	Mode	Function
7	R	**SAV/EAV two-bit error**
6	R	**SAV/EAV one-bit error**
5	R/W	**Auto switch when ADC-PLL non-lock** 0: Disable 1: Enable
4	R/W	**Auto switch when overflow or underflow** 0: Disable 1: Enable
3	R/W	**Decode Video-8 when ADC or TMDS active** 0: Disable 1: Enable
1	R/W	**EAV Error Correction Enable in video8** 0: Disable 1: Enable
0	R/W	**8-bit Random Generator** 0: Disable 1: Enable

Address: 8F FCLK (Scale Down Clcok) Fine Tune Default: 00h

Bit	Mode	Function
7:2	--	**Reserved**
1	R/W	**0x8F[3] & 0x8F[1] FCLK fine tune** 01: slowest 00: typical 1x: fastest
0	R/W	**Select source of FCLK** 0: original setting (default) 1: select ADC_CLK without combinational logic delay

Embedded OSD

Address: 90 OSD_ROW_ADDR (OSD Row Address)

Bit	Mode	Function
7:0	R/W	Row Address for embedded OSD access

Address: 91 OSD_COL_ADDR (OSD Column Address)

Bit	Mode	Function
7:0	R/W	Column Address for embedded OSD access

Address: 92 OSD_DATA_PORT (OSD Data Port)

Bit	Mode	Function
7:0	W	Data port for embedded OSD access

Refer to the embedded OSD application note for the detailed.

Embedded Timing Controller

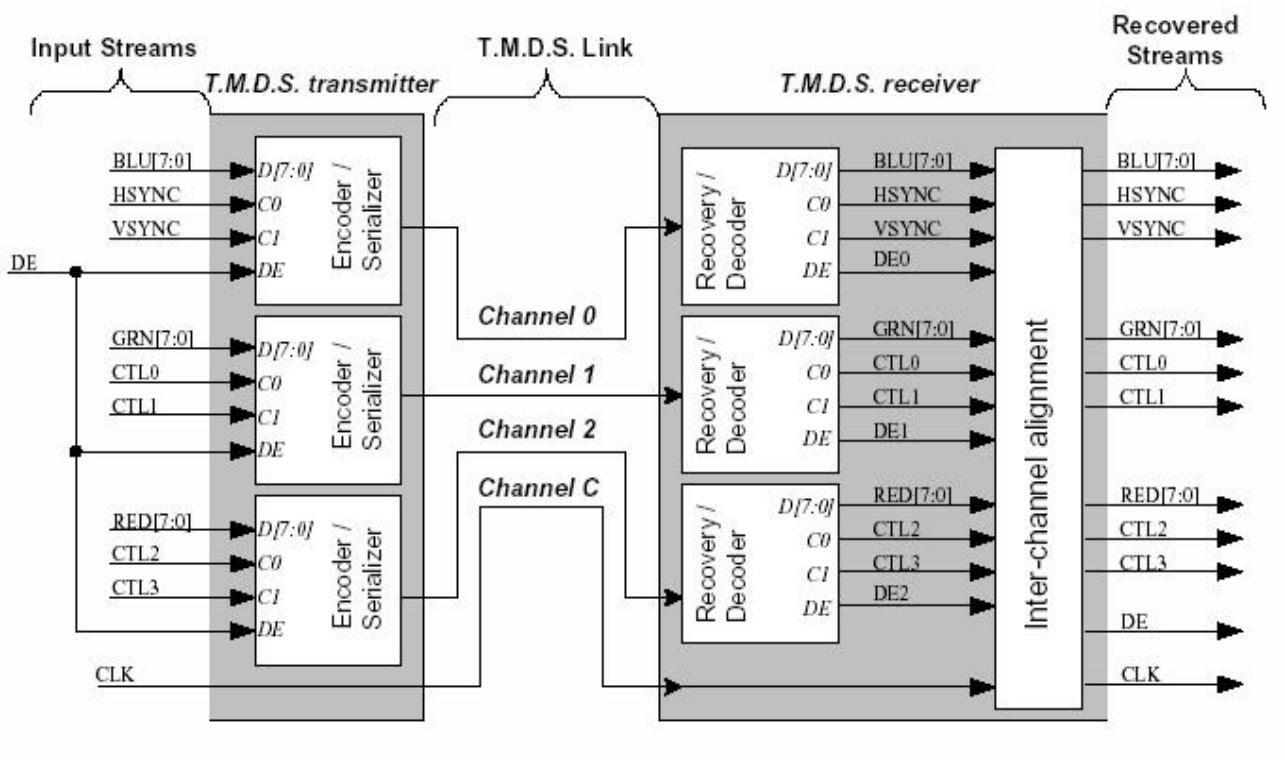
Address: 95 TCON_ADDR _PORT **Default: 00h**

Bit	Mode	Function
7:0	**R/W**	Address port for embedded TCON access

Address: 96 TCON_DATA _PORT

Bit	Mode	Function
7:0	**R/W**	Data port for embedded TCON access

Embedded TMDS with HDCP



Address A0: Output Port Enable **Default: 0Fh**

Bit	Mode	Function
7	R/W	Power down TMDS/HDCP whole function High: Normal Run Low: Power Down
6:4	R/W	Read as '0'
3	R/W	Output control by auto function High: Auto output, Low: Manual.
2:0	R/W	Bit 0: Enable Blue output port. Bit 1: Enable Green output port Bit 2: Enable Red output port

Address A1: Input Port Enable **Default: EFh**

Bit	Mode	Function
7	R/W	Mcufirst High: disable DDC channel and MCU access only Low: enable DDC channel and MCU access only when DDC is not busy
6:5	R/W	Reserved
4	R	Chbok: Detect Blue Channel DE low last 128 dclk High: Active, Low: Non-Active
3	R/W	Input control by auto function High: Auto enable, Low: Manual
2:0	R/W	Bit 0: Enable Blue input port. Bit 1: Enable Green input port Bit 2: Enable Red input port

Address A2: Analog Performance#1 **Default: 8Bh**

Bit	Mode	Function
7	R/W	WDmode: Select Watch Dog mode, Low: Analog, High: Digital.

6:5	R/W	00: Auto 10: Watch Dog Pin='1' x1: Watch Dog Pin='0'
4:3	R/W	sr[1:0]: The resistor of LPF in PLL.
2:0	R/W	si[2:0]: Charge pump current in PLL, Icp=si[2:0]*5u+5u.

Address A3: Analog Performance#2 **Default: 26h**

Bit	Mode	Function
7	R/W	anaWDen: Analog watch dog when ckonctrl =1, control pllckon High: Analog & Digital Low: Digital
6	R/W	ckon_manual: control pllckon when ckon_ctrl =0, Low: off, High: on.
5	R/W	ckonctrl: Low: Manual, High: Auto
4	R/W	z0pow: MCU must pull it up after power stable
3	R/W	down: When down=0, Z0 is auto set 50 ohm.
2:1	R/W	selTST[1:0]: Select the TSTout function of clock port & RD port.
0	R/W	ENTST: Enable clock port TSTout pin. 0:Analog to TSTPAD (20k ohm to GND) 1:Digital to TSTPAD (50 ohm to VDD)

Address A4: Analog Performance#3 **Default: 35h**

Bit	Mode	Function
7:6		Read as "00"
5:4	R/W	selTST[1:0]: Select the TSTout pin of Z0_control.
3:0	R/W	When down=1, Z0 can be controlled by [3:0]

Address A5: Analog_Test_Output_Selection & Digital WD **Default: 2f h**

Bit	Mode	Function
7:6	R/W	Reserved
5:4	R/W	selperd: Choose the freq stable time to turn on pllckon Perd Stable Time 00: 16us 32~48us 01: 64us 128~192us 10:256us 512~768us 11: 1ms 2~3ms
3	R/W	HZTST: Enable TMDS TSTout pin. 0:Enable TSTOUTPAD 1:High impedance
2:0	R/W	selTST[2:0]: Select the TSTout pin to PAD.

Address A6: Control Register **Default: 08h**

Bit	Mode	Function
7	R/W	High: CRC check during the next full frame and clear reg. 0xA7~0xA9. Low: After start CRC
6	R	CRCdone High: When CRC done Low: When set 0xA6[7]
5	R/W	Indicate VSYNC Polarity Mode: High: manual, decided by 0xA6[0] Low: auto, indicate by 0xA6[4]
4	R	Indicate VSYNC Polarity High: Negative Low: Positive
3	R/W	HDCP Enable High: Auto Enable HDCP function, when Tx I2C write Aksv,

		Low: Disable HDCP
2	R/W	Reserved
1	R/W	Always PRE-charge: High: Enable, Low: Disable
0	R/W	Invert VSYNC for HDCP High: Inverted Low: Not Inverted

Address A7: CRC Output Byte_0 **Default: XX**

Bit	Mode	Function
7:0	R	CRC output bit 7~0 Cleared when 0x04[2] is set.

Address A8: CRC Output Byte_1 **Default: XX**

Bit	Mode	Function
7:0	R	CRC output bit 15~8

Address A9: CRC Output Byte_2 **Default: XX**

Bit	Mode	Function
7:0	R	CRC output bit 23~16

Address:AA: RESERVED to 0

Address AB: DVI_REG_TEST **Default: 00h**

Bit	Mode	Function
7	R/W	tck_mode: High: TCK2 mode Low: Original
6:4	R/W	f25sel: Decision latched data of F2x5FIFOT: check 12bit 30bit 000 [11:0] lat0 29:0 001 [23:12] lat1 29:0 010 [47:36] lat3 59:30 011 [59:48] lat4 59:30 10x [29:24] lat2 29:0 11x [35:30] lat2 59:30
3	R/W	Reserved
2:1	R/W	wpsel: Display selection of write pointer of TMDS, 00: wp=6'h00, 01: wp of blue channel 10: wp of green channel 11: wp of red channel
0	R/W	dclkdiv: Low: out dclk when shwp=0,shck=1 to VIDEO8[0] High: dclk/2

Address AC: Pattern Comparator **Default: 90h**

Bit	Mode	Function
7	R/W	Calibration of FIFO write pointer after Vsync High: Enable calibration, Low: Disable
6	R/W	Calibration write pointer Vsync edge select High: Falling, Low: Rising
5	R/W	Hsync edge select after Vsync calibrate write pointer High: Falling, Low: Rising
4	R/W	Clock delay select after Hsync calibrate write pointer High: Enable delay 5 clock Low: Disable
3	R/W	Calibration of FIFO write pointer and boundary detection after falling DE

		High: Enable calibration, Low: Disable
2	R/W	pertst: High: start to do pixel error rate test wait for matched pattern Low: stop PERT and clear numerr and perten
1	R/W	pertmode: High: PN code PERT Low: Half clock PERT
0	R	perten: High: matched pattern found PERT(Pixel Error Rate Test) enable Low: clear by pertst reset

Address AD: Pixel Error Rate Low Byte **Default: 00h**

Bit	Mode	Function
7:0	R	Numerr low byte: Total count of pixel error

Address AE: Pixel Error Rate High Byte **Default: 00h**

Bit	Mode	Function
7:0	R	Numerr high byte: Total count of pixel error

Address AF: DVI_CTRL1 **Default: 00h**

Bit	Mode	Function
7	R/W	Device Key Access Port download enable High: enable Low: disable
6:4	R	If Red/Green/Blue FIFO overflow or underflow, These will set '1', clear '0' after read.
3	R/W	Reserved
2	R/W	OCLK divide 2: High: Enable Low: Disable
1:0	R/W	Reserved

Address B0: TMDS CTL0~3 Signal Status **Default:30h**

Bit	Mode	Function
7:4	R/W	Reserved
3	R	TMDS internal CTL3 signal status
2	R	TMDS internal CTL2 signal status
1	R	TMDS internal CTL1 signal status
0	R	TMDS internal CTL0 signal status

Address B1: Device Key Access Port **Default: 00h**

Bit	Mode	Function
7:0	R/W	When enable device key accessing 40x56 table, When enable device key accessing 40x56 table, the 56-bit key table will be transferred to 64-bit pseudo data with 7^{th}, 15^{th}, 23rd, 31st, 39^{th}, 47^{th}, 55^{th} bits inserted. The inserted data are '0'.And the write sequence is: {D0-Byte0, D0-Byte1, D0-Byte2, D0-Byte3,D0-Byte4, D0-Byte5, D0-Byte6, D0-Byte7}, {D1-Byte0, D1-Byte1, 1-Byte2,D1-Byte3, D1-Byte4, D1-Byte5, D1-Byte6, D1-Byte7}, ……

Address B2: Device Key BIST Pattern

Bit	Mode	Function
7	R/W	Reserved
6:0	W	BIST Pattern Input

Address B3~B5 Reserved

Address B6: HDCP_ADDR_PORT **Default: 00h**

Bit	Mode	Function

7:0	R/W	Address port for embedded HDCPaccess

Address B7: HDCP_DATA_PORT

Bit	Mode	Function
7:0	R/W	Data port for embedded HDCP access

HDCP Control Register Map

Hex Address	*Write/ Read*	*Size in Bytes*	*Register Name*	*Function*
0x00	R/W	5	BKSV	Video receiver KSV. This value must always be available for reading, and may be used to determine that the video receiver is HDCP capable. Valid KSVs contain 20 ones and 20 zeros, a characteristic that must be verified by video transmitter hardware before encryption is enable.
0x05	R	3		Read as 0x00
0x08	R	2	Ri'	Link verification response. Updated every 128th frame. It is recommended that graphics systems protect against errors in the I2C transmission by reading this value when unexpected values are received. This value must be available at all times between updates. R0' must be available a maximum of 100ms after AKSV is received. Subsequent Ri' values must be available a maximum of 128 pixel clocks following the assertion of CTL3
0x0A	R	6		Read as 0x00
0x10	R	5	AKSV	Video transmitter KSV. Writes to this multi-byte value are written least significant byte first. The final write to 0x14 triggers the authentication sequence in the display device.
0x15	R	3		Read as 0x00
0x18	R	8	An	Session random number. This multi-byte value must be written by the graphics system before the KSV is written.
0x20	R	20		Read as 0x00
0x34	R	12		Read as 0x00
0x40	R	1	Bcaps	Bit 6: REPEATER. Video repeater capability. This device is not a repeater. Read as ZERO. Bit 5: READY, KSV FIFO ready. This device does not support repeater capability. Read as ZERO. Bit 4: FAST. This device supports 400Khz transfers. Read as ONE.
0x41	R	2	Bstatus	This device does not support repeater capability. All byte read as 0x00.
0x43	R	1	KSV/FIFO	Read as 0x00
0x44	R	124		Read as 0x00

Address B8~BB Reserved

DVI DDC Channel

(Refers to the VESA "Display Data Channel Standard" for detailed, DVI channel only support DDC2B)

Address: BC DDC_ENABLE (DDC Channel Enable Register) Default: 00h

Bit	Mode	Function
7:5	R/W	DDC Channel Address Least Significant 3 Bits (The default DDC channel address MSB 4 Bits is "A")
4	R/W	DDC Write Status (for external DDC access only) It is cleared after write.
3	R/W	DDC SRAM Write Enable (for external DDC access only) 0: Disable 1: Enable
2	R/W	DDC Debounce Enable 0: Disable 1: Enable (with crystal / 4)
1	R/W	DDC Channel RAM Size

		0: 128 bytes 1: 256 bytes
0	R/W	DDC Channel Enable Bit 0: MCU access Enable 1: DDC channel Enable

Address: BD DDC_INDEX (DDC SRAM R/W Index Register)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Index Register[7:0]

The DDC channel index register will be auto increased one by one after each read or write cycle.

Address: BE DDC_ACCESS_PORT (DDC Channel ACCESS Port)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Port

** The DDC function can still work when Power_Down & Power_Save.

** After reset , the register will be set to default value, but ths SRAM will keep original data.

I2C Control Register Map (DVI DDC side): 0x74/0x75

Hex Address	*Write/ Read*	*Size in Bytes*	*Register Name*	*Function*
0x00	R	5	BKSV	Video receiver KSV. This value must always be available for reading, and may be used to determine that the video receiver is HDCP capable. Valid KSVs contain 20 ones and 20 zeros, a characteristic that must be verified by video transmitter hardware before encryption is enable.
0x05	R	3	Reserved	All bytes read as 0x00
0x08	R	2	Ri’	Link verification response. Updated every 128th frame. It is recommended that graphics systems protect against errors in the I2C transmission by reading this value when unexpected values are received. This value must be available at all times between updates. R0’ must be available a maximum of 100ms after AKSV is received. Subsequent Ri’ values must be available a maximum of 128 pixel clocks following the assertion of CTL3
0x0A	R	6	Reserved	All bytes read as 0x00
0x10	R/W	5	AKSV	Video transmitter KSV. Writes to this multi-byte value are written least significant byte first. The final write to 0x14 triggers the authentication sequence in the display device.
0x15	R	3	Reserved	All bytes read as 0x00
0x18	R/W	8	An	Session random number. This multi-byte value must be written by the graphics system before the KSV is written.
0x20	R	20	Reserved	Only necessary for transmitters.
0x34	R	12	Reserved	All bytes read as 0x00
0x40	R	1	Bcaps	Bit 6: REPEATER. Video repeater capability. This device is not a repeater. Read as ZERO. Bit 5: READY, KSV FIFO ready. This device does not support repeater capability. Read as ZERO. Bit 4: FAST. This device supports 400Khz transfers. Read as ONE.
0x41	R	2	Bstatus	This device does not support repeater capability. All byte read as 0x00.
0x43	R	1	KSV FIFO	Key selection vector FIFO. This device is not a repeater. All byte read as 0x00
0x44	R	124	Reserved	All bytes read as 0x00

Control for LVDS

Address: C0 LVDS_CTRL0 **Default: 00h**

Bit	Mode	Function
7	**R/W**	Power down PLL High: Normal Low: Power down
6	**R/W**	Power down even-port High: Normal Low: Power down
5	**R/W**	Power down odd-port High: Normal Low: Power down
4	**R/W**	Reserved
3	**R/W**	Select PLLtest-pin High: Fin Low: Fbak
2	**R/W**	WDRSTL: WD reset High: reset WD Low: WD on
1	**R/W**	WDSETL: WD set High: set WD Low: WD on
0	**R**	WD_Status (write to clear status)

Address: C1 LVDS_CTRL1 **Default: A3h**

Bit	Mode	Function
7:6	**R/W**	SCAPL [1:0]: Select Cload=1.2p*code (+1p)
5:3	**R/W**	SVOCML [2:0]: LVDS common mode voltage
2:0	**R/W**	SVOSWL [2:0]: LVDS output swing (max+/-30%)

Address: C2 LVDS_CTRL2 **Default: 22h**

Bit	Mode	Function
7:6	**R/W**	SBGL [1:0]: Bandgap Voltage (~1.2V)
5:3	**R/W**	SIL [2:0]: PLL charge pump current (I=5uA+5uA*code)
2:1	**R/W**	SRL [1:0]: PLL resistor
0	**R/W**	BMTS: Bit-Mapping Table Select High: Table 2 Low: Table 1

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
Even A	**ER1**	**ER0**	**EG0**	**ER5**	**ER4**	**ER3**	**ER2**	**ER1**	**ER0**	**EG0**	**ER5**
Even B	**EG2**	**EG1**	**EB1**	**EB0**	**EG5**	**EG4**	**EG3**	**EG2**	**EG1**	**EB1**	**EB0**
Even C	**EB3**	**EB2**	**DEN*6**	**VS*5**	**HS*5**	**EB5**	**EB4**	**EB3**	**EB2**	**DEN*6**	**VS*5**
Even D	**ER7**	**ER6**	**RSV*7**	**EB7**	**EB6**	**EG7**	**EG6**	**ER7**	**ER6**	**RSV*7**	**EB7**
Odd A	**OR1**	**OR0**	**OG0**	**OR5**	**OR4**	**OR3**	**OR2**	**OR1**	**OR0**	**OG0**	**OR5**
Odd B	**OG2**	**OG1**	**OB1**	**OB0**	**OG5**	**OG4**	**OG3**	**OG2**	**OG1**	**OB1**	**OB0**
Odd C	**OB3**	**OB2**	**DEN*2**	**VS*1**	**HS*0**	**OB5**	**OB4**	**OB3**	**OB2**	**DEN*2**	**VS*1**
Odd E	**OR7**	**OR6**	**RSV*3**	**OB7**	**OB6**	**OG7**	**OG6**	**OR7**	**OR6**	**RSV*3**	**OB7**

TABLE 1 Bit-Mapping 6bit(5~0)+2bit(7~6)

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
Even A	ER3	ER2	EG2	ER7	ER6	ER5	ER4	ER3	ER2	EG2	ER7
Even B	EG4	EG3	EB3	EB2	EG7	EG6	EG5	EG4	EG3	EB3	EB2
Even C	EB5	EB4	DEN*6	VS*5	HS*5	EB7	EB6	EB5	EB4	DEN*6	VS*5
Even D	ER1	ER0	RSV*7	EB1	EB0	EG1	EG0	ER1	ER0	RSV*7	EB1
Odd A	OR3	OR2	OG2	OR7	OR6	OR5	OR4	OR3	OR2	OG2	OR7
Odd B	OG4	OG3	OB3	OB2	OG7	OG6	OG5	OG4	OG3	OB3	OB2
Odd C	OB5	OB4	DEN*2	VS*1	HS*0	OB7	OB6	OB5	OB4	DEN*2	VS*1
Odd E	OR1	OR0	RSV*3	OB1	OB0	OG1	OG0	OR1	OR0	RSV*3	OB1

TABLE 2 Bit-Mapping 6bit(7~2)+2bit(1~0)

Address: C3 LVDS_CTRL3 **Default: 80h**

Bit	Mode	Function
7:6	R/W	E_RSV_s: even port reserve signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [3] 00: PWM_0
5:4	R/W	E_DEN_s: even port data enable signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [2] 00: E_DEN (DENA)
3:2	R/W	E_VS_s: even port VS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [1] 00: E_VS (DVS)
1:0	R/W	E_HS_s: even port HS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [0] 00: E_HS (DHS)

Address: C4 LVDS_CTRL4 **Default: 80h**

Bit	Mode	Function
7:6	R/W	O_RSV_s: odd port reserve signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [4] 00: PWM_1
5:4	R/W	O_DEN_s: odd port data enable signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [2] 00: O_DEN (DENA)
3:2	R/W	O_VS_s: odd port VS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [1] 00: O_VS (DVS)
1:0	R/W	O_HS_s: odd port HS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [0] 00: O_HS (DHS)

Address: C5 LVDS_CTRL5 **Default: 00h**

Bit	Mode	Function

7:3	**R/W**	Reserved
2:0	**R/W**	STSTL [2:0]: select test attribute 000: High Impedance 001: VOCME 010: VBG 011: 60uA (20K ohm to GND) 1xx: TSTPLL (50 ohm to VDD)

Phase Lock Loop

Address: D0 DPLL_CTRL (Display PLL Control Register) Default: 10h

Bit	Mode	Function
7:3	R/W	**Charge Pump Current** (0.5uA ~ 16uA)//(00010)
2	R	**DPLL Status** 0: Normal 1: Abnormal
1	---	Reserved
0	R/W	**DPLL output enable**//(0) 0: Inhibit DPLL output 1: Enable DPLL output

Address: D1 DPLL_M (M Parameter Register) Default: (7Dh)

Bit	Mode	Function
7:0	R/W	**DPM** value – 2

Address: D2 DPLL_N (N Parameter Register) Default: 0Ah

Bit	Mode	Function
6	R/W	**VCO Frequency Divider** (original 50MHz ~ 400MHz, 350~450 is better)//(0) 0: 1/4 1: 1/2
5:0	R/W	**DPN** value – 2

Assume **DPLL_M**=0x7D, **DPM**=0x7D+2=127; **DPLL_N**=0x0A, **DPN**=0x0A+2=12; **VCO**=1/4, **F_IN** = 24.576MHz.
F_DPLL = **F_IN** x **DPM** / **DPN** x **VCO / 4(2)** = 24.576 x 127 / 12 / 4 = 65.024MHz.

Address: D3 DPLL_FILTER (Loop Filter Control Register) Default: 2Fh

Bit	Mode	Function
7:6	R/W	Reserved
5:3	R/W	**Loop Filter Resistance Control** (1Kohm ~ 8Kohm). 6Kohm is preferred. //(101)
2:0	R/W	**Loop Filter Capacitance Control** (25pF ~ 200pF). 200pF is preferred. //(111)

Address: D4 DPLL_SSP (Spread Spectrum Control Register) Default: 06h

Bit	Mode	Function
7:6	R/W	**Spread Spectrum Current** (SSP_I) (0.5uA~2uA)//(00)
5:4	R/W	**Spread Spectrum Width** (SSP_W) (0.5ns~2ns)//(00)
3	R/W	**Spread Spectrum FMDIV** (SSP_FMDIV)//(0) 0: 33K 1: 66K
2	R/W	**Test-Pin 2 Input/Output Switch** 0: Input 1: Output
1	R/W	**Test-Pin 1 Input/Output Switch** 0: Input 1: Output
0	R/W	**Spread Spectrum Enable** (SSP_EN)//(0) 0: Disable 1: Enable

Address: D5 Reserved

Address: D6 PLL1_CTRL (PLL1 Control Register) Default: 12h

Bit	Mode	Function
7:4	R/W	**Charge Pump Current** (5uA ~ 80uA)//(0001)
3	R	**PLL1 Status**

		0: Normal 1: Abnormal
2	----	Reserved
1	R/W	**Phase Trigger Clock Stop**//(1) 0: Stop (for Test) 1: Normal Run
0	R/W	**PLL1 Power Down**//(0) 0: Power Down 1: Normal Run

Address: D7 PLL1_M (M Parameter Register) Default: (0Bh)

Bit	Mode	Function
7:0	R/W	**P1M** value – 2

Address: D8 PLL1_N (N Parameter Register) Default: 03h

Bit	Mode	Function
5:0	R/W	**P1N** value – 2

Assume **PLL1_M**=0x0B, **P1M**=0x0B+2=13; **PLL1_N**=0x03, **P1N**=0x03+2=5; **F_IN** = 24.576MHz.
F_PLL1 = **F_IN** x **P1M** / **P1N** = 24.576 x 13 / 5 = 63.8976MHz
If the target frequency is **F_ADC**, the constraint of **F_PLL1** is ***(15/16)*F_ADC < F_PLL1 < F_ADC***

Address: D9 PLL1_FILTER (Loop Filter Control Register) Default: 6Fh

Bit	Mode	Function
7:6	R/W	**BandGap Voltage Select** (Default = 01).
5:3	R/W	**Loop Filter Resistance Control** (1Kohm ~ 8Kohm). 6Kohm is preferred.(101)
2:0	R/W	**Loop Filter Capacitance Control** (20pF ~ 160pF). 160pF is preferred.(111)

Address: DA PLL2_CTRL (PLL2 Control Register) Default: 10h

Bit	Mode	Function
7:4	R/W	**Charge Pump Current** (5uA ~ 80uA)//(0001)
3:1	R/W	**Select 1 pair of 8 pairs signal to testpin** (default = 000).
0	R/W	**PLL2 Power Down** //(0) 0: Power Down (default) 1: Normal Run

Address: DB PLL2_M (M Parameter Register) Default: 0Ah

Bit	Mode	Function
7:0	R/W	**P2M** value – 2

Address: DC PLL2_N (N Parameter Register) Default: 04h

Bit	Mode	Function
7	R	**PLL2 Status** 0: Normal 1: Abnormal
5:0	R/W	**P2N** value – 2

Assume **PLL2_M**=0x0A, **P2M**=0x0A+2=12; **PLL2_N**=0x04, **P2N**=0x04+2=6; **F_IN** =65 MHz .
F_PLL2 = F_IN x P2M / P2N /2 = 65 x 12 / 6 / 2 = 65 MHz
the constraint of **F_PLL2** is that ***P2N =(int)(F_IN / 10)***

Address: DD PLL2_FILTER (Loop Filter Control Register) Default: EFh

Bit	Mode	Function
7:6	R/W	**Select CLK to A/D from** 00: internal PLL (PLL2 phase-select output) 01: internal clock (Fav) 10: test-pad clock (PLL_TEST1 input) 11: inverse internal PLL (PLL2 phase-select output)

5:3	R/W	**Loop Filter Resistance Control** (1Kohm ~ 8Kohm). 6Kohm is preferred.(101)
2:0	R/W	**Loop Filter Capacitance Control** (20pF ~ 160pF). 160pF is preferred.(111)

Address: DF PLLPHASE (Select Phase to A/D) **Default: 80h**

Bit	Mode	Function
7	R/W	X control
6:3	R/W	16 phases pre-select
0	R/W	Y control

Phase	[X ^^^^ Y]	Phase	[X ^^^^ Y]	Phase	[X ^^^^ Y]	Phase	[X ^^^^ Y]
0	[1 0000 1]	**8**	[0 1000 1]	**16**	[1 0000 0]	**24**	[0 1000 0]
1	[1 0001 1]	**9**	[01001 1]	**17**	[1 0001 0]	**25**	[0 1001 0]
2	[1 0010 1]	**10**	[0 1010 1]	**18**	[1 0010 0]	**26**	[0 1010 0]
3	[1 0011 1]	**11**	[0 1011 1]	**19**	[1 0011 0]	**27**	[0 1011 0]
4	[1 0100 1]	**12**	[0 1100 1]	**20**	[1 0100 0]	**28**	[0 1100 0]
5	[0 0101 1]	**13**	[1 1101 0]	**21**	[1 0101 0]	**29**	[1 1101 1]
6	[0 0110 1]	**14**	[1 1110 0]	**22**	[0 0110 0]	**30**	[1 1110 1]
7	[0 0111 1]	**15**	[1 1111 0]	**23**	[0 0111 0]	**31**	[1 1111 1]

Embedded ADC

Address: E0 REDGAIN

Bit	Mode	Function
7:0	R/W	RED Channel Gain Adjust

Address: E1 GRNGAIN

Bit	Mode	Function
7:0	R/W	Green Channel Gain Adjust

Address: E2 BLUGAIN

Bit	Mode	Function
7:0	R/W	Blue Channel Gain Adjust

Adjust the full-scale input range that corresponds to the maximum digital 8-bit binary output. Setting REDGAIN to 0 corresponds to an input full-scale range of 0.5V, and 255 adjust the input full-scale range to 1.0 V. That means the GAIN setting will change the LSB resolution. Increasing the gain results in larger input range, and less contrast effect is visible.

Address: E3 REDOFST

Bit	Mode	Function
7:0	R/W	**Red Channel Clamp Offset** FFh : clamp Vin+128*(Vfs/256) in back porch period as code 00h. 80h : clamp Vin in back porch period as code 00h. 00h : clamp Vin-128*(Vfs/256) in back porch as code 00h.

Address: E4 GRNOFST

Bit	Mode	Function
7:0	R/W	**Green Channel Clamp Offset** FFh : clamp Vin+128*(Vfs/256) in back porch period as code 00h. 80h : clamp Vin in back porch period as code 00h. 00h : clamp Vin-128*(Vfs/256) in back porch as code 00h.

Address: E5 BLUOFST

Bit	Mode	Function
7:0	R/W	**Blue Channel Clamp Offset** FFh : clamp Vin+128*(Vfs/256) in back porch period as code 00h. 80h : clamp Vin in back porch period as code 00h. 00h : clamp Vin-128*(Vfs/256) in back porch as code 00h.

Vfs: Input full-scale voltage *depends on REDGAIN setting*, **Vin**: Input channel signal, **Vbp**: Vin in back porch period
This register is used to adjust the input clamp level. One LSB offset (=Vfs/256) equals one LSB change in ADC output. Increasing the offset setting results in less brightness. Be careful that input full-scale voltage depends on GAIN setting, so the LSB offset step will be increased when increasing the GAIN setting.

Address: E6 ADC_CTRL **Default: 80h**

Bit	Mode	Function
7:3	R/W	**SOG Reference Control** //(10000)
2	R/W	**ADC R-Channel Power Down** (SOG Circuit always enable) //(0) 0: ADC Power Down 1: Normal
1	R/W	**ADC G-Channel Power Down** (SOG Circuit always enable) //(0) 0: ADC Power Down 1: Normal
0	R/W	**ADC B-Channel Power Down** (SOG Circuit always enable) //(0) 0: ADC Power Down 1: Normal

DDC Special Function Access

The following DDC special function registers are only valid when EXT# =0.

Address: F0 DDC_SET_SLAVE **Default: 6E**

Bit	Mode	Function
7:1	R/W	**DDC Slave Address** to decode
0	R/W	Channel Select 0: from ADC 1: from DVI

Address: F1 DDC_SUB_IN

Bit	Mode	Function
7:0	R	**DDC Sub-Address Received**

Address: F2 DDC_DATA_IN

Bit	Mode	Function
7:0	R	**DDC Data Received**

Address: F3 DDC_DATA_OUT

Bit	Mode	Function
7:0	W	**DDC Data Output**

Address: F4 DDC_STATUS

Bit	Mode	Function
7:5	----	Reserved
4	R	If **DDC_STOP** signal occurs, this bit is set to “1”
3	R	If **DDC_DATA_OUT** loaded to serial-out-byte, this bit is set to “1”
2	R	If **DDC_DATA_IN** latched, this bit is set to “1”
1	R	If **DDC_SUB** latched, this bit is set to “1”
0	R	If **DDC_SLAVE** latched, this bit is set to “1”

Write to clear status.

Address: F5 DDC_IRQ_CTRL **Default: 00h**

Bit	Mode	Function
7:5	----	Reserved
4	R/W	0: Disable the **DDC_STOP** signal as an interrupt source 1: Enable the **DDC_STOP** signal as an interrupt source
3	R/W	0: Disable the **DDC_DATA_OUT** loaded to serial-out-byte as an interrupt source 1: Enable the **DDC_DATA_OUT** loaded to serial-out-byte as an interrupt source
2	R/W	0: Disable the **DDC_DATA_IN** latched as an interrupt source 1: Enable the **DDC_DATA_IN** latched as an interrupt source
1	R/W	0: Disable the **DDC_SUB** latched as an interrupt source 1: Enable the **DDC_SUB** latched as an interrupt source
0	R/W	0: Disable the **DDC_SLAVE** latched as an interrupt source 1: Enable the **DDC_SLAVE** latched as an interrupt source

DDC Channel

(Refers to the VESA "Display Data Channel Standard" for detailed)

Address: FC DDC_ENABLE (DDC Channel Enable Register) Default: 00h

Bit	Mode	Function
7:5	R/W	**DDC Channel Address Least Significant 3 Bits** (The default DDC channel address MSB 4 Bits is "A")
4	R/W	**DDC Write Status (for external DDC access only)** It is cleared after write.
3	R/W	**DDC SRAM Write Enable (for external DDC access only)** 0: Disable 1: Enable
2	R/W	**DDC Debounce Enable** 0: Disable 1: Enable (with crystal/4)
1	R/W	**DDC Channel RAM Size** 0: 128 bytes 1: 256 bytes
0	R/W	**DDC Channel Enable Bit** 0: MCU access Enable 1: DDC channel Enable

Address: FD DDC_INDEX (DDC SRAM R/W Index Register)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Index Register[7:0]

The DDC channel index register will be auto increased one by one after each read or write cycle.

Address: FE DDC_ACCESS_PORT (DDC Channel ACCESS Port)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Port

** The DDC function can still work when Power_Down & Power_Save.

** After reset , the register will be set to default value, but ths SRAM will keep original data.

Address: FF Digital Test Reserved

Bit	Mode	Function
7:5	---	Reserved
4	R/W	PWM2/ TCON[1] Attribute: (under 0xFF[3]='0') 1: TCON [1] 0: PWM2
3	R/W	CP test signals for LVDS bit[6:0] go through by {PWM0, DDCSDA, DDCSCL, DDC2SCL, DDC2SDA, PWM1, DTST1} 1: Enable 0: Disable (if 0xFF[3]='0', DTST1=TCON[0])
2:0	R/W	000 Even data to LVDS A [6:0] 001 Even data to LVDS B [6:0] 010 Even data to LVDS C [6:0] 011 Even data to LVDS D [6:0] 100 Odd data to LVDS A [6:0] 101 Odd data to LVDS B [6:0] 110 Odd data to LVDS C [6:0] 111 Odd data to LVDS D [6:0]

Timing Controller

RTD2522 Register Description for Embedded Timing Controller:

Address: 95 TCON_ADDR _PORT Default: 00h

Bit	Mode	Function
7:0	**R/W**	Address port for embedded TCON access

Address: 96 TCON_DATA _PORT

Bit	Mode	Function
7:0	**R/W**	Data port for embedded TCON access

Register Description

Timing Controller Programmable Registers:

Address: 00 TC_CTRL1 (Timing Controller control register1) Default: 00h

Bit	Mode	Function
7	R/W	**Enable Timing Controller Function (Global)** 0: Disable 1: Enable
6	R/W	Reserved
5	R/W	**TCON[n] Toggle Function Reset** 0: not reset 1: reset by DVS
4	R/W	Reserved
3	R/W	**Inactive Period Data Controlled by internal TCON [4]** 0: DEN 1: TCON [4]
2:0	R/W	Reserved

Address: 01~07 Reserved for future

Address: 08 TCON[0]_VS_LSB (TCON [0] Vertical Start LSB Register)

Bit	Mode	Function
7:0	W	Line number[7:0] at which TCON control generation begins

Address: 09 TCON [0]_VS_MSB (TCON [0] Vertical Start/End MSB Register)

Bit	Mode	Function
7		Reserved
6:4	W	Line number[10:8] at which TCON control generation ends
3		Reserved
2:0	W	Line number[10:8] at which TCON control generation begins

Address: 0A TCON [0]_VE_LSB (TCON [0] Vertical End LSB Register)

Bit	Mode	Function
7:0	W	Line number[7:0] at which TCON control generation ends

Address: 0B TCON [0]_HS_LSB (TCON [0] Horizontal Start LSB Register)

Bit	Mode	Function
7:0	W	Pixel count[7:0] at which TCON goes active

Address: 0C TCON [0]_HS_MSB (TCON [0] Horizontal Start/End MSB Register)

Bit	Mode	Function
7		Reserved
6:4	W	Pixel count[10:8] at which TCON goes inactive
3		Reserved
2:0	W	Pixel count[10:8] at which TCON goes active

Notes: To be triggered on rising edge of the DCLK

Address: 0D TCON [0]_HE_LSB (TCON [0] Horizontal End LSB Register)

Bit	Mode	Function
7:0	W	Pixel count[7:0] at which TCON goes inactive

Notes: If the register number is large than display format, the horizontal component is always on.

Address: 0E TCON [0]_CTRL (GPO[0] Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**TCON [n] Enabl**e (Local) 0: Disable (TCON [n] output clamp to '0') 1: Enable
6:0	R/W	Reserved

TCON [0] ~ TCON [4] Control Registers Address Map

Address	Data(# bits)	Default
0A,09,08	TCON [0]_VS_REG (11)	
0D,0C,0B	TCON [0]_HS_REG (11)	
0E	TCON [0]_CTRL_REG	00
0F	Reserved	
12,11,10	TCON [1]_VS_REG (11)	
15,14,13	TCON [1]_HS_REG (11)	
16	TCON [1]_CTRL_REG	00
17	Reserved	
1A,19,18	TCON [2]_VS_REG (11)	
1D,1C,1B	TCON [2]_HS_REG (11)	
1E	TCON [2]_CTRL_REG	00
1F	Reserved	
22,21,20	TCON [3]_VS_REG (11)	
25,24,23	TCON [3]_HS_REG (11)	
26	TCON [3]_CTRL_REG	00
27	Reserved	
2A,29,28	TCON [4]_VS_REG (11)	
2D,2C,2B	TCON [4]_HS_REG (11)	
2E	TCON [4]_CTRL_REG	00
2F	Reserved	

Embedded OSD

Block Diagram

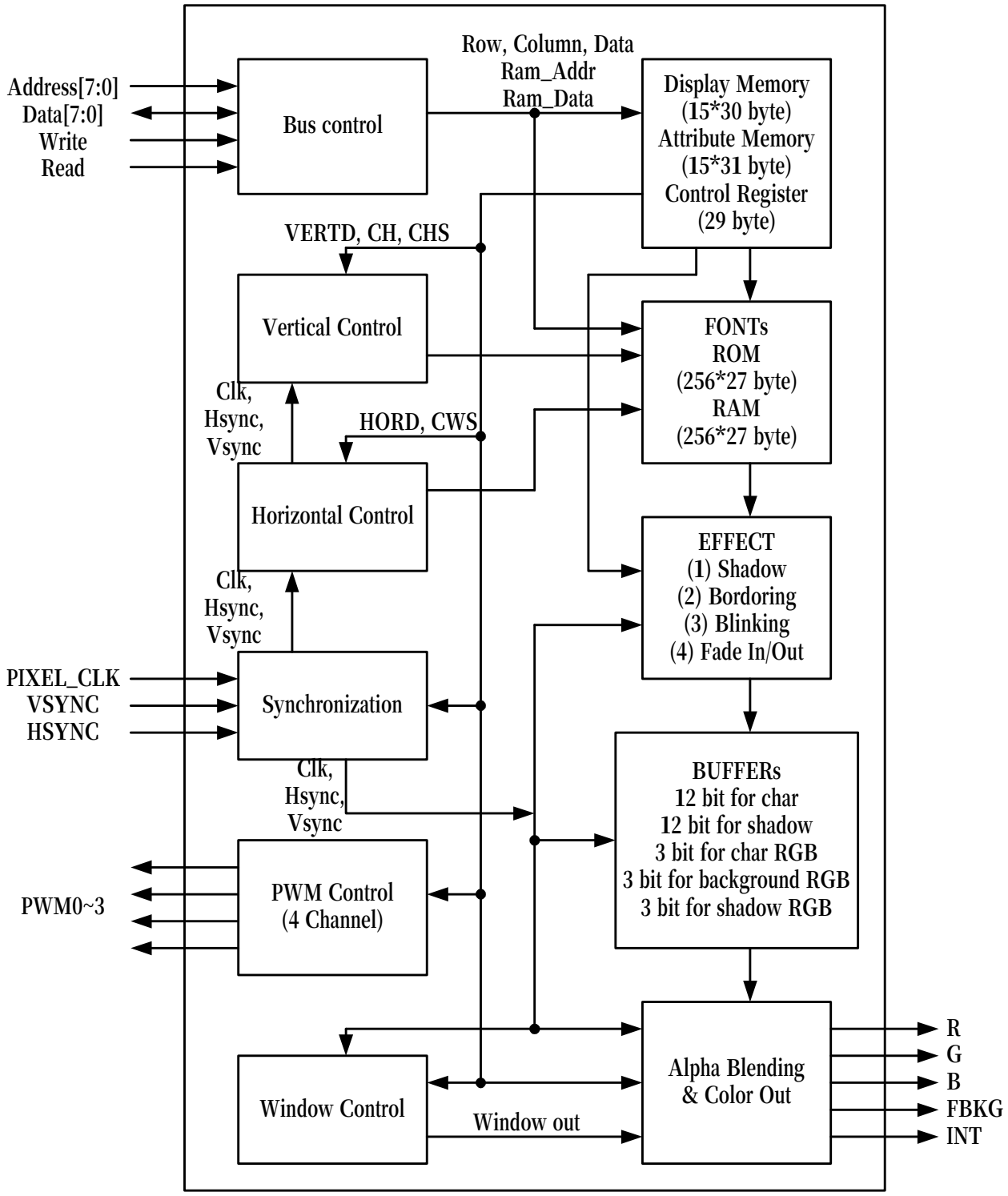


Figure 13 OSD Block Diagram

Addressing

Row port : A7~A0 = 90h (corresponds to register 90h in RTD2522)
Column port : A7~A0 = 91h (corresponds to register 91h in RTD2522)
Data port : A7~A0 = 92h (corresponds to register 92h in RTD2522)

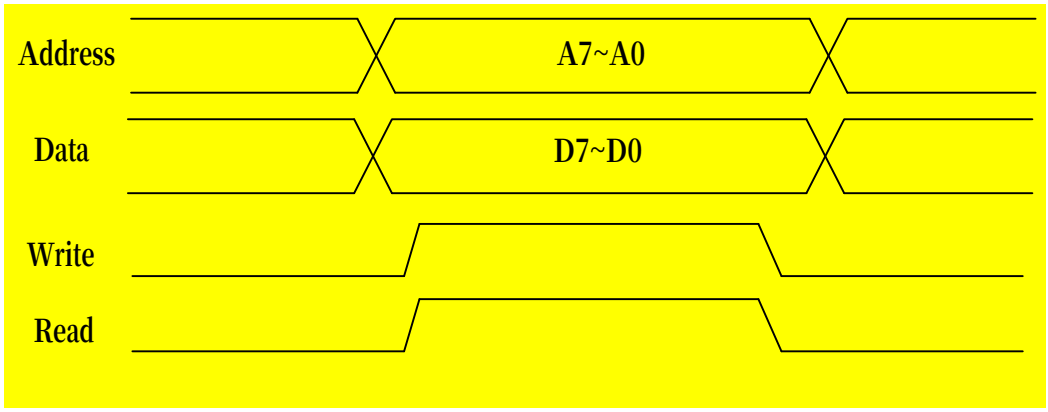


Figure 14 OSD Access Timing

1.1.11 *Programming Sequence*

a : assign ROW assign COLUMN assign DATA.
b : assign COLUMN assign DATA. (ROW is keep as previous content)
c : assign DATA. (ROW and COLUMN is keep as previous content.
And COLUMN is auto incremented by 1)

1.1.12 *The Allowable Programming Sequence*

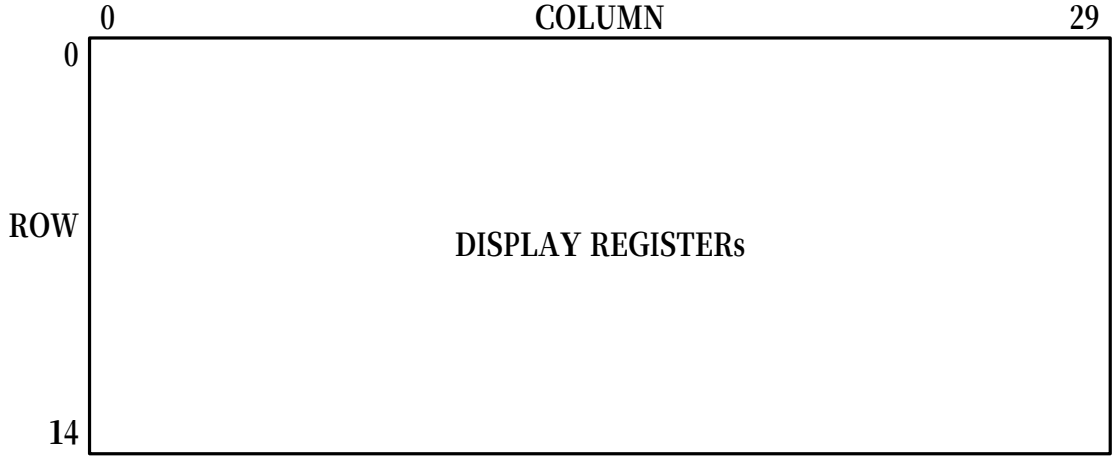
For display registers and attribute registers:
(1) a b c a b c a b c …
(2) a b c b c b c b c …
(3) a b c c .. b c c …
(4) a b c c c c c …

For user's ram:
(1) a b c0 c1 c2 … c35 (36 c for a complete character font)
a b c0 c1 …

Register Access

ROW address bit [A7:A5] = 3'b**100** : Display Registers
= 3'b**101** : Attribute Registers
= 3'b**110** : User's Font RAM

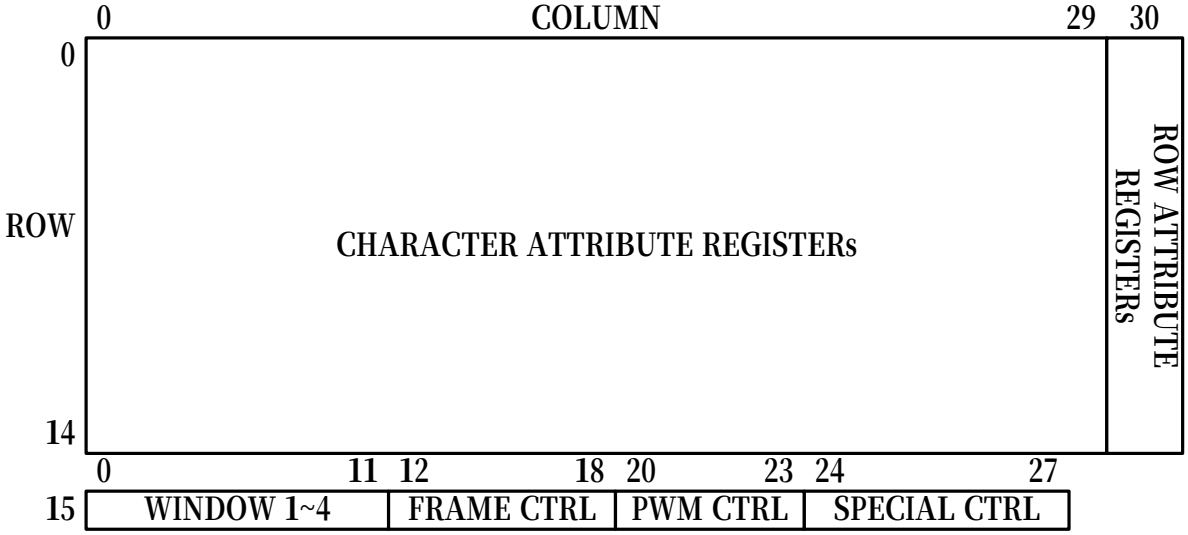
1.1.13 *Display Register*



ADDRESS	BIT								Transmission
	7	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*FORMAT*
ROW	1	0	0	X	D3	D2	D1	D0	a, b, c
COLUMN	X	X	X	D4	D3	D2	D1	D0	a, b
DATA	D7	D6	D5	D4	D3	D2	D1	D0	c
X: don't care D: valid data									

Figure 15 Display Registers

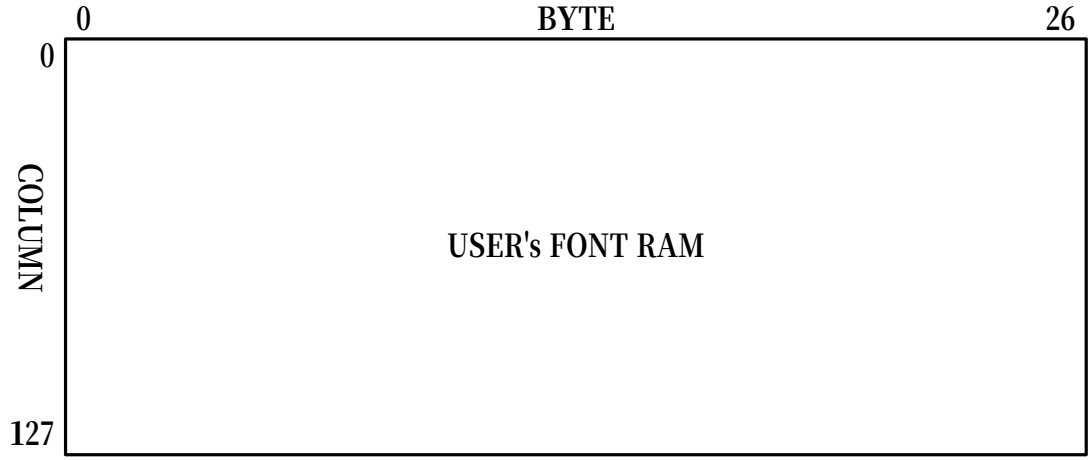
1.1.14 *Attribute Register*



ADDRESS	BIT								Transmission
	7	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*FORMAT*
ROW	1	0	1	X	D3	D2	D1	D0	a, b, c
COLUMN	X	X	X	D4	D3	D2	D1	D0	a, b
DATA	D7	D6	D5	D4	D3	D2	D1	D0	c
X: don't care D: valid data									

Figure 16 Character Attribute Registers

1.1.15 *User Font RAM*



ADDRESS	BIT								Transmission
	7	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*FORMAT*
ROW	1	1	0	X	X	X	X	X	a, b, c
COLUMN	D7	D6	D5	D4	D3	D2	D1	D0	a, b
DATA	D7	D6	D5	D4	D3	D2	D1	D0	c
X: don't care D: valid data									

Figure 17 User Font RAM

Registers

(I)Display Registers (Row0~14, Coln 0~29)

7	6	5	4	3	2	1	0
CHARACTER							

MSB LSB

Address: Row 0~14, Column 0~29 default: 00h

Bit	Mode	Function
7:0	W	ROM character address. These eight bits address one of the 256 character or symbols in the embedded ROM and RAM.

(II) Attribute Registers (Row0~14, Coln 0~29)

7	6	5	4	3	2	1	0
FONT_SEL	BGR	BGG	BGB	BLINK	R	G	B

Address: Row 0~14, Column 0~29 default: 00h

Bit	Mode	Function
7	W	**Font Select from ROM or RAM** (user-font) 0: ROM 1: RAM(only bit 6~0 valid)
6:4	W	**Background color selection**. These three bits define the color of the background for the correspondent characters. If all three bits are clear, no background will be shown (transparent). The color selection is shown in table 2.
3	W	**Blinking effect enable**. If this bit is set to '1', blinking effect will be active on corresponding character. The blinking frequency is one time per second(1Hz) with 50%-50% duty cycle at 80Hz vertical scan frequency.
2:0	W	**Character/Symbol color selection**. These three bits are the color attributes to define the color of the corresponding character or symbol. In color user font, these three bits define which color to be transparent.

Table 2 The character/window/shadow color selection

Window/Character	Background	R	G	B
Black	Transparent/Blending	0	0	0
Blue	Blue	0	0	1
Green	Green	0	1	0
Cyan	Cyan	0	1	1
Red	Red	1	0	0
Magenta	Magenta	1	0	1
Yellow	Yellow	1	1	0
White	White	1	1	1

(III) Row Attribute Registers (Row 0~14, Coln 30)

7	6	5	4	3	2	1	0
	R_BSEN	RS Enable	RS Color		R_INT	CHS	CWS

Address: Row 0~14, Column 30 default:00h

Bit	Mode	Function
7	---	Reserved.
6	W	**Row Bordering/Shadowing function enable**. (R_BSEN) 0 : disable bordering/shadowing effect of a single row. 1 : enable bordering/shadowing effect of a single row. *Row bordering and shadowing are controlled by 'BSEN' bit in Frame Control register –Row 15, Column 15. If this bit is set to '1', this function is enabled even though the 'BSEN' bit is '0'. Row bordering and shadowing is selected by 'SHADOW' bit in Frame Control register –Row 15, Column 15.
5	W	**Row Space (between current and next row)** 0: Disable 1: Enable
4	W	Row Space Color **(between current and next row)** 0: background color of next row 1: window color
3	---	Reserved.
2	W	**Intensity control for this row**.(R_INT) 0 : Normal intensity in corresponding ROW. INT output '0'. 1 : High intensity in corresponding ROW. INT output '1'. *When displaying shadow, border and background, INT output '0'. (shadow, border, background are dark color)
1	W	**Height of display character/symbol**.(CHS) 0: normal height. 1: double height.
0	W	**Width of display character/symbol**.(CWS) 0: normal width. 1: double width. *****When **double character width** is selected for a row, only the even-numbered character will be displayed. That is, characters of column 0,2,4,… 28 will be displayed.

R_INT **is not effective** when displaying character's shadow, border and background.

(IV) Window Registers

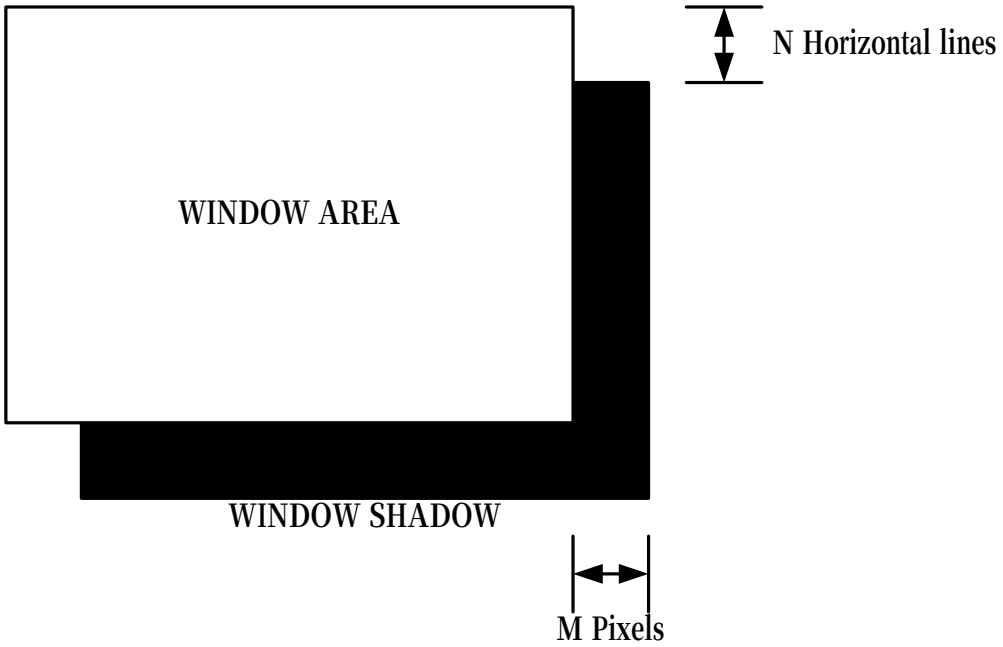


Figure 18 Window area and shadow

- **Window 1 Row Address Register (Row 15, Coln 0)**

7	6	5	4	3	2	1	0
ROW START ADDR				ROW END ADDR			
MSB			LSB	MSB			LSB

Address: Row 15, Column 0 default:XXh

Bit	Mode	Function
7:4	W	**Window 1 ROW start address**.
3:0	W	**Window 1 ROW end address**.

- **Window 1 Column Start Address Register (Row 15, Coln 1)**

7	6	5	4	3	2	1	0
COLUMN START ADDR					R	G	B
MSB				LSB			

Address: Row 15, Column 1 default:X0h

Bit	Mode	Function
7:3	W	**Window 1 COLUMN start address**.
2:0	W	**R,G,B Color of Window 1**.

- **Window 1 Column End Address Register (Row 15, Coln 2)**

7	6	5	4	3	2	1	0
COLUMN END ADDR					WEN	W_INT	W_SHD

MSB LSB

Address: Row 15, Column 2 default:00h

Bit	Mode	Function
7:3	W	**Window 1 COLUMN end address**.
2	W	**Enable Window 1**. 0:disable 1:enable Window 1.
1	W	**Color Intensity Selection for Window 1**. 0: normal intensity in this window. 1: high intensity in this window.
0	W	**Shadowing Window 1**. 0: disable shadowing. 1: enable shadowing.

- **Window 2 Row Address Register (Row 15, Coln 3)**

Address: Row 15, Column 3 default:XXh

Bit	Mode	Function
7:4	W	**Window 2 ROW start address**.
3:0	W	**Window 2 ROW end address**.

- **Window 2 Column Start Address Register (Row 15, Coln 4)**

Address: Row 15, Column 4 default:X0h

Bit	Mode	Function
7:3	W	**Window 2 COLUMN start address**.
2:0	W	**R,G,B Color of Window 2**.

- **Window 2 Column End Address Register (Row 15, Coln 5)**

Address: Row 15, Column 5 default:X0h

Bit	Mode	Function
7:3	W	**Window 2 COLUMN end address**.
2	W	**Enable Window 2**. 0:disable 1:enable Window 2.
1	W	**Color Intensity Selection for Window 2**. 0: normal intensity in this window. . 1: high intensity in this window.
0	W	**Shadowing Window 2**.

		0: disable shadowing. 1: enable shadowing.

- **Window 3 Row Address Register (Row 15, Coln 6)**

Address: Row 15, Column 6 default:XXh

Bit	Mode	Function
7:4	W	**Window 3 ROW start address**.
3:0	W	**Window 3 ROW end address**.

- **Window 3 Column Start Address Register (Row 15, Coln 7)**

Address: Row 15, Column 7 default:X0h

Bit	Mode	Function
7:3	W	**Window 3 COLUMN start address**.
2:0	W	**R,G,B Color of Window 3**.

- **Window 3 Column End Address Register (Row 15, Coln 8)**

Address: Row 15, Column 8 default:X0h

Bit	Mode	Function
7:3	W	**Window 3 COLUMN end address**.
2	W	**Enable Window 3**. 0:disable 1:enable Window 3.
1	W	**Color Intensity Selection for Window 3**. 0: normal intensity in this window. 1: high intensity in this window.
0	W	**Shadowing Window 3**. 0: disable shadowing. 1: enable shadowing.

- **Window 4 Row Address Register (Row 15, Coln 9)**

Address: Row 15, Column 9 default:XXh

Bit	Mode	Function
7:4	W	**Window 4 ROW start address**.
3:0	W	**Window 4 ROW end address**.

- **Window 4 Column Start Address Register (Row 15, Coln 10)**

Address: Row 15, Column 10 default:X0h

Bit	Mode	Function
7:3	W	**Window 4 COLUMN start address**.
2:0	W	**R,G,B Color of Window 4**.

• **Window 4 Column End Address Register (Row 15, Coln 11)**

Address: Row 15, Column 11 default:X0h

Bit	Mode	Function
7:3	W	**Window 4 COLUMN end address**.
2	W	**Enable Window 4**. 0:disable 1:enable Window 4.
1	W	**Color Intensity Selection for Window 4**. 0: normal intensity in this window. 1: high intensity in this window.
0	W	**Shadowing Window 4**. 0: disable shadowing. 1: enable shadowing.

(V) Frame Control Registers

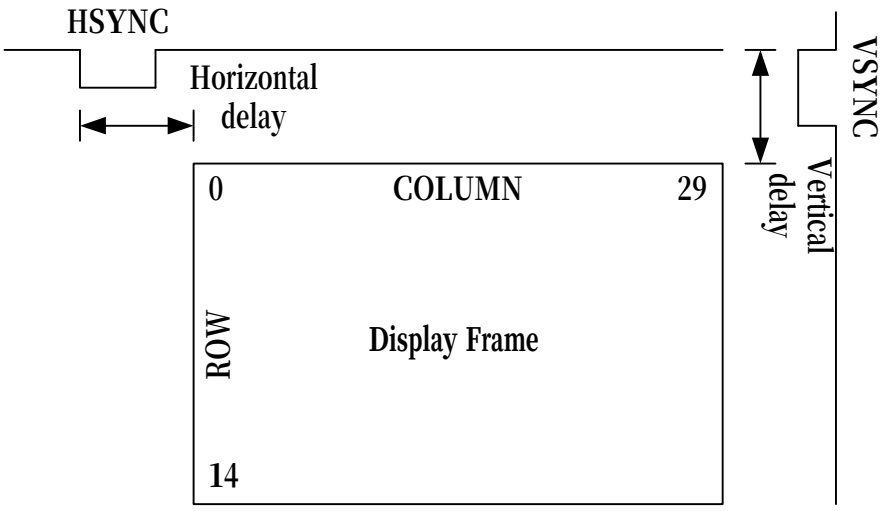


Figure 19 Window area and shadow

- **Vertical Delay Control Register (Row 15, Coln 12)**

7	6	5	4	3	2	1	0
VERTD							

MSB LSB

Address: Row 15, Column 12 default:04h

Bit	Mode	Function
7:0	W	**Vertical Delay** (VERTD). These bits define the vertical starting address. Totally 256 steps, with an increment of 4 horizontal lines per step. It can't be zero any time. ***Vertical Delay = (VERTD+1)*4 horizontal scan lines** The default value is 04h.

- **Horizontal Delay Control Register (Row 15, Coln 13)**

7	6	5	4	3	2	1	0
HORD							

MSB LSB

Address: Row 15, Column 13 default:0Fh

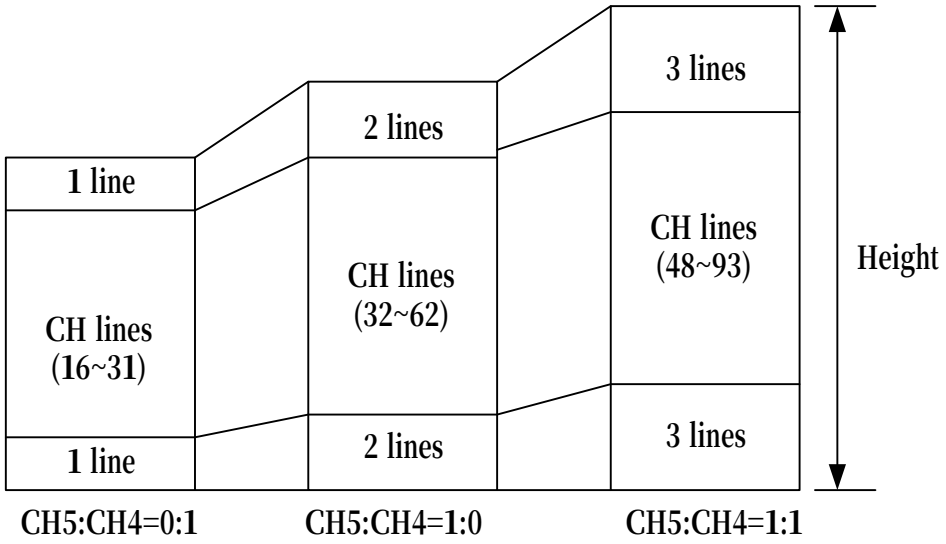
Bit	Mode	Function
7:0	W	**Horizontal Delay** (HORD). These bits define the horizontal starting address. Totally 256 steps, each step increment represents of 6 dots (12*18 font) shift to the right on the screen. ***Horizontal Delay = (HORD*6+16) dots** The default value is 0Fh.

- **Character Height Control Register (Row 15, Coln 14)**

7	6	5	4	3	2	1	0
	CLR	CH5	CH4	CH3	CH2	CH1	CH0

Address: Row 15, Column 14 default:00h

Bit	Mode	Function
7	---	Reserved
6	W	**Clear** (CLR). 1: all display registers, character attribute and row attribute registers from Row 0 to Row 14 are all cleared but not affecting registers in the Row 15 and special control registers in Row 16 and user's font SRAM. The 'CLR' bit should be auto cleared after this action finished. *The external RESET set the content of all registers in Row 15 and Row 16 to their default value, and clear the contents in the display registers and attribute register ,and user's font SRAM.
5:0	W	**Character Height** (CH5:0). These bits determine the displayed character height. The OSD adopts 12*18 font matrix and the middle 16 lines (line 1 to line 16) are expands by the BRM algorithm according CH3~0. CH5:4 determine the size of expanded font matrix. CHS CH5:CH4 multiplier N --- 0 0:0 N=1 0 0:1 N=1 0 1:0 N=2 0 1:1 N=3 1 0:0 N=2 1 0:1 N=2 1 1:0 N=4 1 1:1 N=6 The expanded font matrix : ([CH3:0]+18) * N



Character Height = N * ([CH3:0] + 18)

Figure 20 Character height modification

Table 3 Repeat line number of character (12*18 font) by BRM algorithm

CH3:0	Repeat Line Number															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0001	-	-	-	-	-	-	-	-	✓	-	-	-	-	-	-	-
0010	-	-	-	-	✓	-	-	-	-	-	-	-	✓	-	-	-
0011	-	-	-	-	✓	-	-	-	✓	-	-	-	✓	-	-	-
0100	-	-	✓	-	-	-	✓	-	-	-	✓	-	-	-	✓	-
0101	-	-	✓	-	-	-	✓	-	✓	-	✓	-	-	-	✓	-
0110	-	-	✓	-	✓	-	✓	-	-	-	✓	-	✓	-	✓	-
0111	-	-	✓	-	✓	-	✓	-	✓	-	✓	-	✓	-	✓	-
1000	-	✓	-	✓	-	✓	-	✓	-	✓	-	✓	-	✓	-	✓
1001	-	✓	-	✓	-	✓	-	✓	✓	✓	-	✓	-	✓	-	✓
1010	-	✓	-	✓	✓	✓	-	✓	-	✓	-	✓	✓	✓	-	✓
1011	-	✓	-	✓	✓	✓	-	✓	✓	✓	-	✓	✓	✓	-	✓
1100	-	✓	✓	✓	-	✓	✓	✓	-	✓	✓	✓	-	✓	✓	✓
1101	-	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	-	✓	✓	✓
1110	-	✓	✓	✓	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	✓
1111	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

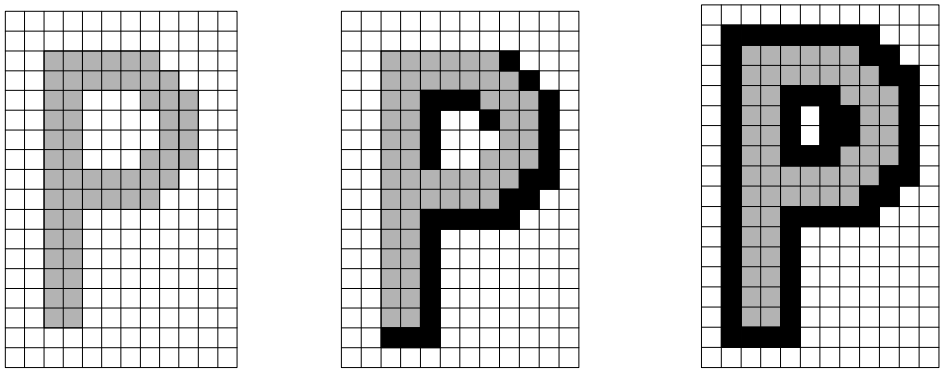
‘ – ‘ : not repeat ‘✓ ’ : repeat

- **Frame Control Register (Row 15, Coln 15)**

7	6	5	4	3	2	1	0
OSD_EN	BSEN	SHADOW	DWE	VST	PWM_EN	FAD	FBKGC

Address: Row 15, Column 15 default:00h

Bit	Mode	Function
7	W	**OSD enable**.(OSD_EN) 0: OSD circuits is inactivated. 1: OSD circuits is activated, and output R,G,B,FBKG signals.
6	W	**Bordering/Shadowing function enable**.(BSEN) 0: disable Bordering/Shadowing function. 1: enable Bordering/Shadowing function.
5	W	**Bordering/Shadowing selection**. 0: Bordering is selected. 1: Shadowing is selected.
4	W	**Double Width Enable**.(DWE) 0: each output pixel of the OSD is counted on 1 clock from PIX_{IN}. 1: each output pixel of the OSD is counted on 2 clocks from PIX_{IN}.
3	W	**OSD vertical start (VST) input signal source select** 0: Select “DVS” as OSD VS input 1: Select “ENA” as OSD VS input
2	W	**PWM_EN**. (PWM output enable) 0 : disable PWM output 1 : enable PWM output When RTD2522 is power down and PWM clock source is forbidden, it is programmer’s duty to disable PWM output.
41	W	**Fade-In/Fade-Out enable**. 0: disable the fade-in/fade-out function. 1: enable the fade-in/fade-out function. *It enables the OSD takes about 1 second to display fully menu from off state (Fade–In). Similarly, it takes 1 second to close fully menu from on state (Fade-Out). **This bit must be set when OSD is disable (OSD_EN=0)**, otherwise a wrong fade action will be generated.
0	W	**Configuration FBKG**. 0: FBKG outputs high during displaying characters or windows. 1: FBKG outputs high only during display characters.



Original character shadowing Bordering

Figure 21 Character effect

- **Frame Control Register (Row 15, Coln 16)**

7	6	5	4	3	2	1	0
WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Address: Row 15, Column 16 default:00h

Bit	Mode	Function
7:6	W	**Window 4 shadow width**.(WW41,WW40) When the window shadow function is activated(W_SHD=1), the Shadow width is determined by (WW41,WW40): (WW41,WW40) Shadow Width M (pixel) --- (0,0) 2 (0,1) 4 (1,0) 6 (1,1) 8
5:4	W	**Window 3 shadow width**.(WW31,WW30) When the window shadow function is activated(corresponding W_SHD=1), the Shadow width is determined by (WW31,WW30).
3:2	W	**Window 2 shadow width**.(WW21,WW20) When the window shadow function is activated(corresponding W_SHD=1), the Shadow width is determined by (WW21,WW20).
1:0	W	**Window 1 shadow width**.(WW11,WW10) When the window shadow function is activated(corresponding W_SHD=1), the Shadow width is determined by (WW11,WW10).

- **Frame Control Register (Row 15, Coln 17)**

7	6	5	4	3	2	1	0
WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Address: Row 15, Column 17 default:00h

Bit	Mode	Function
7:6	W	**Window 4 shadow height**.(WH41,WH40) When the window shadow function is activated(W_SHD=1), the Shadow width is determined by (WH41,WH40): (WH41,WH40) Shadow Height N (pixel) --- (0,0) 2 (0,1) 4 (1,0) 6 (1,1) 8
5:4	W	**Window 3 shadow height**. (WH31,WH30) When the window shadow function is activated (corresponding W_SHD=1), the Shadow height is determined by (WH31,WH30).
3:2	W	**Window 2 shadow height**. (WH21,WH20) When the window shadow function is activated (corresponding W_SHD=1), the Shadow height is determined by (WH21,WH20).
1:0	W	**Window 1 shadow height**. (WH11,WH10) When the window shadow function is activated (corresponding W_SHD=1), the Shadow height is determined by (WH11,WH10).

- **Frame Control Register (Row 15, Coln 18)**

7	6	5	4	3	2	1	0
RSPACE							RS_EN

MSB LSB

Address: Row 15, Column 18 default:00h

Bit	Mode	Function
7:3	W	**Row Spacing Lines**. (RSPACE) These 5 bits define the row to row spacing horizontal line N. It means extra (RSPACE+1) lines will be appended for each display character row. It is usually used to maintain the constant OSD menu height for different display mode instead of adjusting the character height.
2:1	---	Reserved.
0	W	**Row Space Function Enable**. 0:disable RSPACE function. 1:enable RSPACE function

(VI) PWM Control Registers

- **Pulse Width Modulation Control Register (Row 15, Coln 20~22)**

7	6	5	4	3	2	1	0
PWM_n							

MSB LSB

Address: Row 15, Column **20~22** default:00h

Bit	Mode	Function
7:0	W	PWM_n – the 8 bits decides the output duty width and waveform of PWM at PWM channel n. (n=0~2)

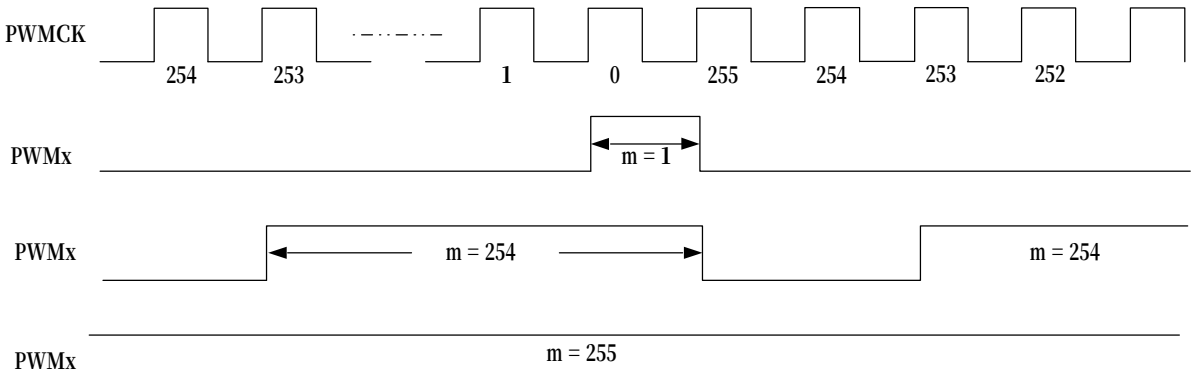


Figure 22 PWM timing

(VII) Special Control Registers

- **Configuration Register 1(Row 15, Coln 24)**

7	6	5	4	3	2	1	0
PWMF1	PWMF0	OUT_DELAY		PWM_CLK	CSR	CSG	CSB

Address: Row 15, Column 24 default:00h

Bit	Mode	Function
7:6	W	**PWM clock frequency selection.** The output PWM clock frequency is determined by PWMF1:F0. 00: PWM_CLK / 1 01: PWM_CLK / 2 10: PWM_CLK / 4 11: PWM_CLK / 8
5	W	**OSD Out Delay** 0: Normal 1:Delay(for high speed)
4	W	**Disp_Extend:** 1: extend disp, used when double pixel mode 0: no-extend disp, used when using 30x15 OSD to increase OSD operating speed.
3	W	**PWM Clock Source From** 0: DCLK; 1: Crystal Clock
2:0	W	**Character Shadow Configuration**. Define the shadow color of displayed characters.

		The color selection is shown in table 1.

- **Window Shadow Configuration Register 1 (Row 15, Coln 25)**

7	6	5	4	3	2	1	0
AB2	WSR2	WSG2	WSB2	AB1	WSR1	WSG1	WSB1

Address: Row 15, Column 25 default:00h

Bit	Mode	Function
7	W	**Enable Alpha Blending** (AB2) 1: enable window 2 alpha blending; 0: disable
6:4	W	**Define the shadow color of window 2.**
3	W	**Enable Alpha Blending** (AB1) 1: enable window 1 alpha blending; 0: disable
2:0	W	**Define the shadow color of window 1**.

- **Window Shadow Configuration Register 2 (Row 15, Coln 26)**

7	6	5	4	3	2	1	0
AB4	WSR4	WSG4	WSB4	AB3	WSR3	WSG3	WSB3

Address: Row 15, Column 26 default:00h

Bit	Mode	Function
7	W	**Enable Alpha Blending** (AB4) 1: enable window 4 alpha blending; 0: disable
6:4	W	**Define the shadow color of window 4**.
3	W	**Enable Alpha Blending** (AB3) 1: enable window 3 alpha blending; 0: disable
2:0	W	**Define the shadow color of window 3**.

Address: Row 15, Column 27 default:00h

Bit	Mode	Function
7	W	**Character Alpha Blending** **0: Disable** **1: Enable**
6	W	**Over range HS delay** **0: no delay** **1: delay one clock.**
5	W	**0: after VS rising edge, mask SRAM write pulse for 2 pixel-clock duration** **1: normal**
4	W	**0: after VS or HS rising edge, mask SRAM read pulse for 2 pixel-clock duration** **1: normal**

3:0	W	**Color User Font Selection**

Programming Notes

1.1.16 *7.5.1 Display Menu Size and Location on Panel*

The OSD display menu size depended on resolution and pixel clock speed of RTD2522. When DWE (double width enable) bit is enabled, this OSD use 1/2 pixel clock speed to display the menu, so the menu width will be doubled. The menu height is decided by CHS and CH5:0. The displayed location is decided by VERTD and HORD, so it is programmer's responsibility to control the display location.

1.1.17 *7.5.2 Programmable User's Font*

The programmer can use those symbols defined in user's RAM instead of embedded symbols in ROM. Surely, programmer must program the user's RAM before using these symbols. It's better to program the user's RAM before the OSD is enabled (OSD_EN=1).

To program a symbol, you must write the content of row 17 first, and others row in sequence. The content of row 0 is written last. Figure 36 shows the programming example.

Row address =	**8'b110XXXXX**	programming user's RAM
Column address =	**8'b01010101**	the 55th symbol in user's RAM
Data (0-th byte) =	8'b00000000	the 7^{th} ~0^{th} dot in row 17 of this symbol
Data (1-th byte) =	8'bxxxx0000	the 11^{th} ~8^{th} dot in row 17 of this symbol
Data (2-th byte) =	8'b00000000	the 7^{th} ~6^{th} dot in row 16 of this symbol
Data (3-th byte) =	8'bxxxx0000	the 11^{th} ~8^{th} dot in row 16 of this symbol
…	…	…
Data (16-th byte) =	8'b11111100	the 7^{th} ~6^{th} dot in row 9 of this symbol
Data (17-th byte) =	8'bxxxx0000	the 11^{th} ~8^{th} dot in row 9 of this symbol
…	…	…
Data (34-th byte) =	8'b00000000	the 0^{th} ~7^{th} dot in row 0 of this symbol
Data (35-th byte) =	8'bxxxx0000	the 11^{th} ~8^{th} dot in row 0 of this symbol

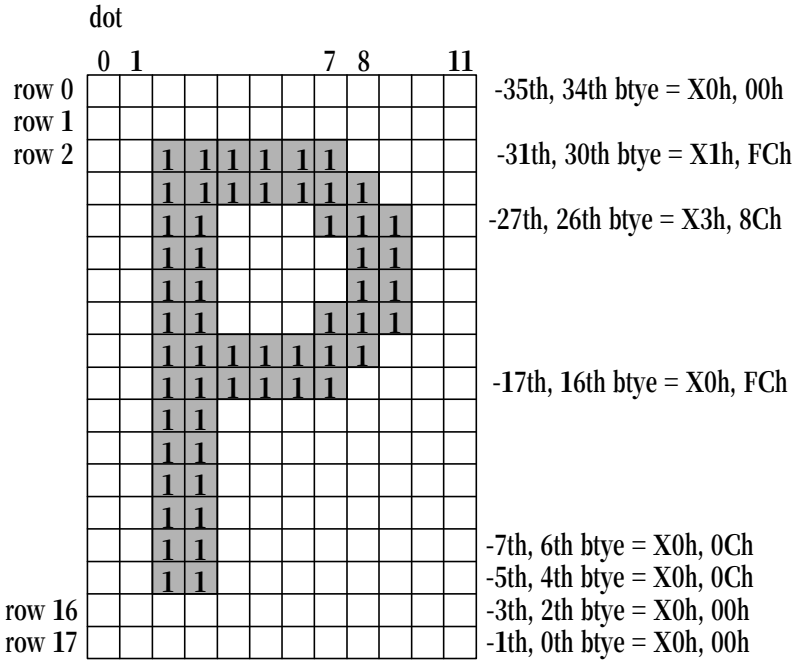


Figure 23 Programming example for User's font RAM

1.1.18 *7.5.3 The Multiple Color Font*

The embedded OSD supports 16 multi-color font in internal ROM address 10h to 1Fh. Because of selectable shadow color for display symbol, if the multi-color symbol and its shadow use the same color, it will be hard to be distinguished. So once the multi-color symbol is displayed, the shadow and border function for this symbol is auto disabled. The multi-color fonts in this version of embedded OSD and those shown in session 7 are difference in contour. **The multi-color fonts in current OSD have the black contour**.

1.1.19 *7.5.4 Overlap of Display Symbol and Window*

When you want to display symbols and windows in the same region, symbol will be shown on the top layer, the order is like below:

Symbol (top layer) Symbol shadow (2nd layer) Window 1 (3rd layer) Window 1 shadow (4th layer) Window 2 Window 2 shadow … Window 4 shadow (the lowest layer).

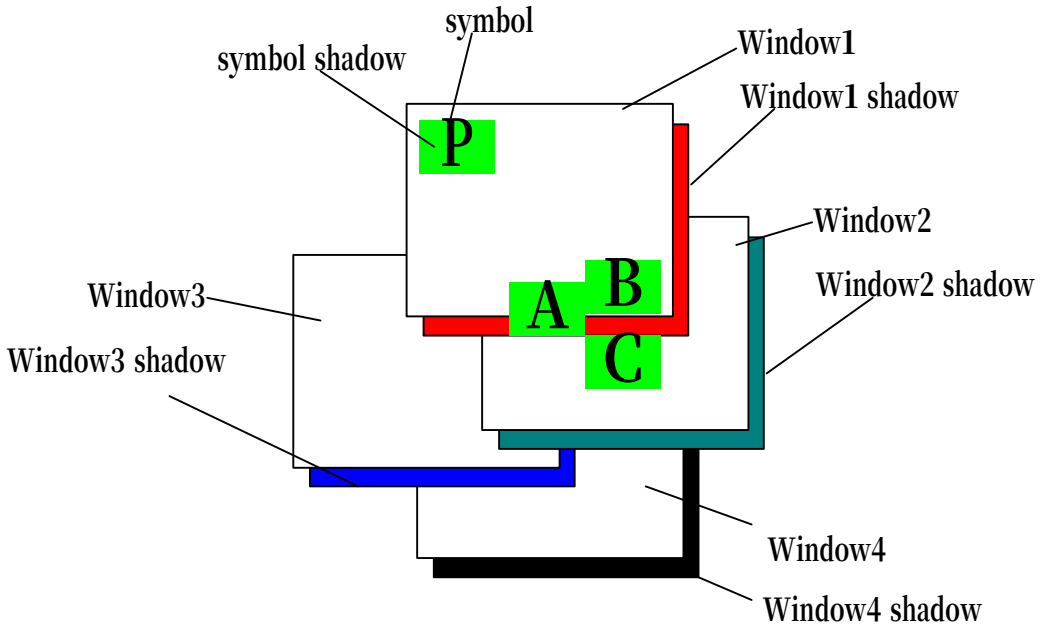


Figure 24 Display priority

A symbol has the first priority to be shown on the top layer. If you located the 'A' in window 2, and display window 1 and windows 2 at the same time, the 'A' will be shown. That is misunderstanding. In this case, 'A' should be hide by window 1, but for hardware simplicity, it's programmer's responsibility to remove 'A' from window 2. The location of 'B' or 'C' is the better choice for displaying symbol in window.

1.1.20

1.1.21

1.1.22 *7.5.5 The User Color Font*

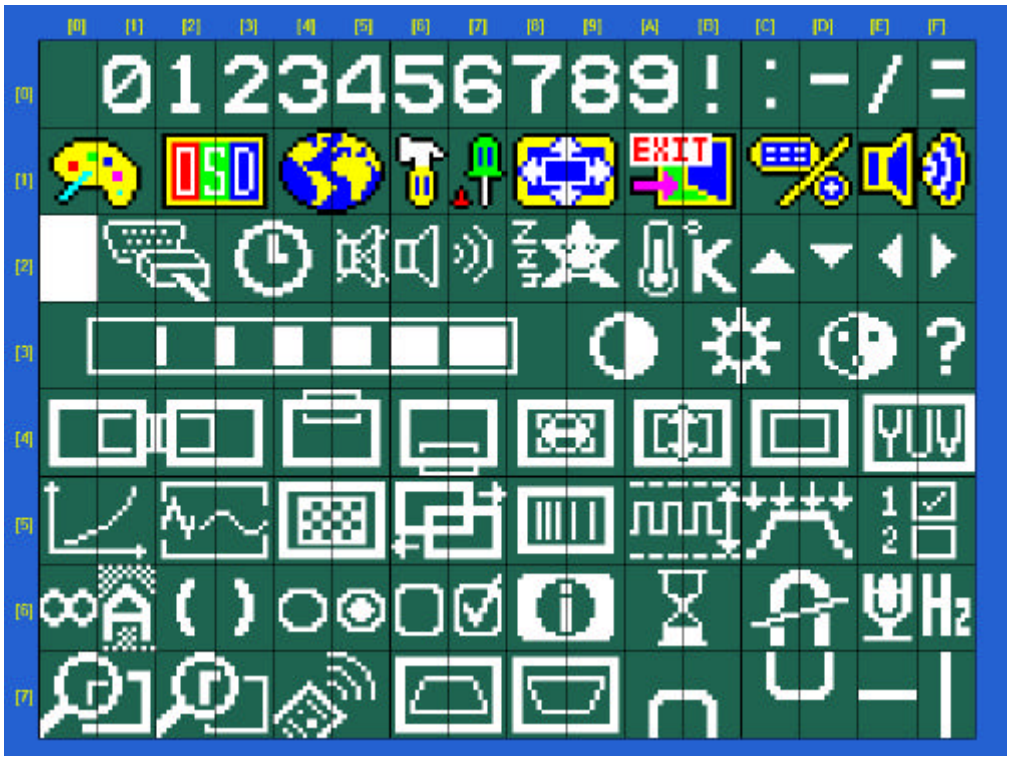
The color font symbol can be programmed in OSD SRAM, maximum of 32 characters. Each color font symbol consists of three font-size SRAM. Address 0x00~0x1f represent red pattern of color font, address 0x20~0x3f represent green pattern, and address 0x40~0x5f represent blue pattern. Color User Font Selection defines how many color fonts is used. Color User Font Selection bit3

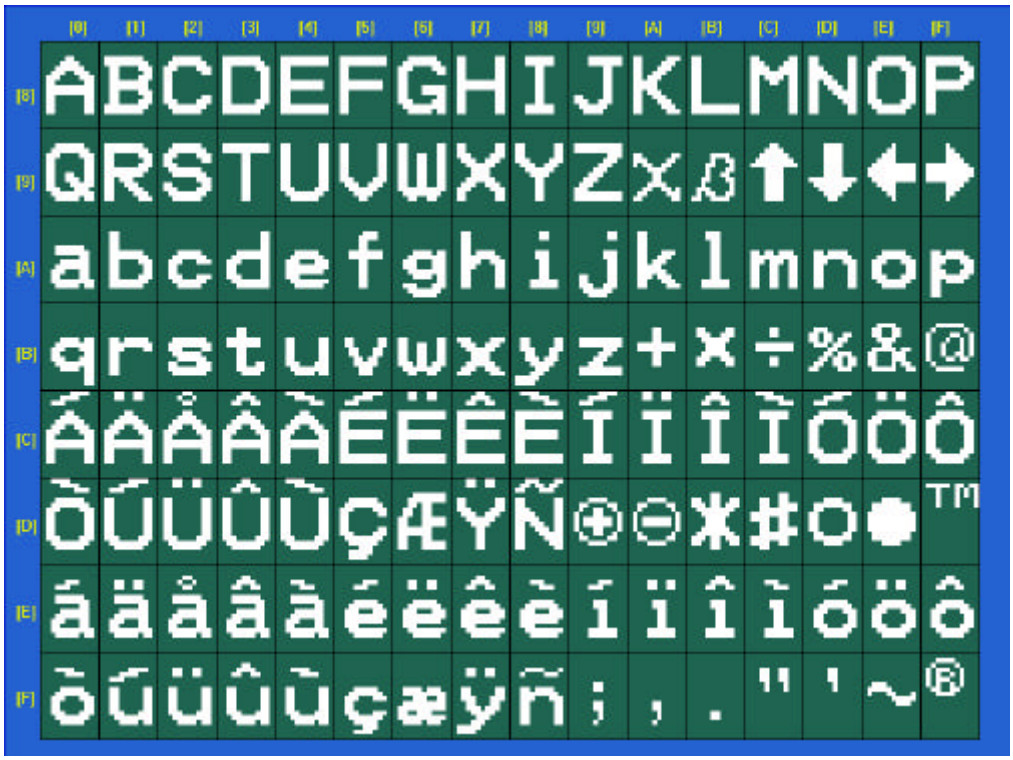
enables programmable color font function, and selects address 0x00~0x03 as color font. Color User Font Selection bit2 selects address 0x10~0x1f as color font, bit1 selects address 0x08~0f, bit0 selects address 0x04~07. The user's font in address 0x60~0x7f is mono color. Color font programming example is shown below.

Number of Color Font	color user font selection	Red Pattern Address	Green Pattern Address	Blue Pattern Address
4	4'b1000	0x00~0x03	0x20~0x23	0x40~0x43
8	4'b1001	0x00~0x07	0x20~0x27	0x40~0x47
12	4'b1010	0x00~0x03, 0x08~0x0f	0x20~0x23, 0x28~0x2f	0x40~0x43, 0x48~0x4f
16	4'b1011	0x00~0x0f	0x20~0x2f	0x40~0x4f
20	4'b1100	0x00~0x03, 0x10~0x1f	0x20~0x23, 0x30~0x3f	0x40~0x43, 0x50~0x5f
24	4'b1101	0x00~0x07, 0x10~0x1f	0x20~0x27, 0x30~0x3f	0x40~0x47, 0x50~0x5f
28	4'b1110	0x00~0x03, 0x08~0x1f	0x20~0x23, 0x28~0x3f	0x40~0x43, 0x48~0x5f
32	4'b1111	0x00~0x1f	0x20~0x3f	0x40~0x5f

Color User Font Selection determines which user fonts are as chromatic. In the utilization of color user's font, the display register must be filled the address of red pattern. Green and blue patterns corresponding to the address of red pattern are combined to form a color font. For example, a display register is set 0x00, and then a color font consists of red, green, blue pattern in the address 0x00, 0x20, 0x40, respectively.

The Embedded Fonts





Electric Specification
DC Characteristics

Table 4 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on VDD	V_{VDD}	-1		4.6	V
Voltage on Input (5V tolerant)	V_{IN}	-1		5.5	V
Voltage on Output or I/O or NC	V_{IO}	-1		4.6	V
Electrostatic Discharge	V_{ESD}			±2.5	kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Storage temperature (plastic)	T_{STG}	-55		125	ºC
Thermal Resistance (Junction to Air)	$è_{JA}$			18	º C/W

Table 5 DC Characteristics/Operating Condition
(0℃<TA<70℃; VDD = 3.3V ± 0.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	VDD	3.0	3.3	3.6	V
Supply Current(All function on at 135M)	I_{VDD}		255.2		mA
digital supply	I_{DVCC}		244		
DCLK PLL supply	I_{AVCC}		5.2		
MCLK PLL supply	I_{PVCC}		6		
Supply Current(Power Saving)	I_{VDD}		7.2		mA
digital supply	I_{DVCC}		5.6		
DCLK PLL supply	I_{AVCC}		0.6		
MCLK PLL supply	I_{PVCC}		1		
Output High Voltage	V_{OH}	2.4		VDD	V
Output Low Voltage	V_{OL}	GND		0.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
I/O Pull-up resistance	R_{PU}	100		300	Ù
I/O Pull-down resistance	R_{PD}	50		150	Ù
Input Leakage Current(VI=VCC or GND)	I_{LI}	-10		+10	ì A
Output Leakage Current(VO=VCC or GND)	I_{LO}	-20		+20	ì A

AC Characteristics

1.1.23 *Input Signal*

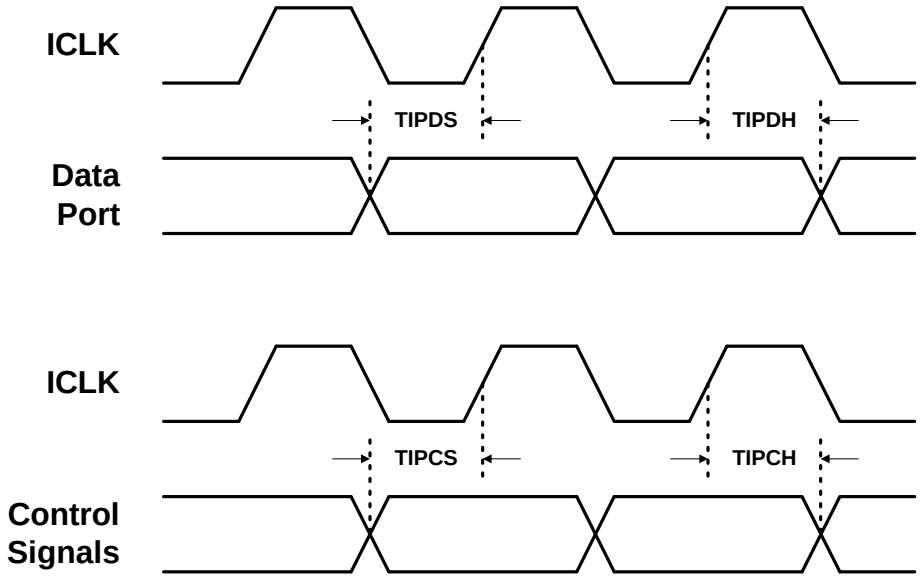


Figure 25 Input Signal Timing

Symbol	Parameter	Min	Max	Unit
TIPCS	Input control signals setup time for ICLK	2		ns
TIPCH	Input control signals hold time for ICLK	1		ns
TIPDS	Input data setup time for ICLK	2		ns
TIPDH	Input data hold time for ICLK	1		ns

1.1.24 *Output Signal*

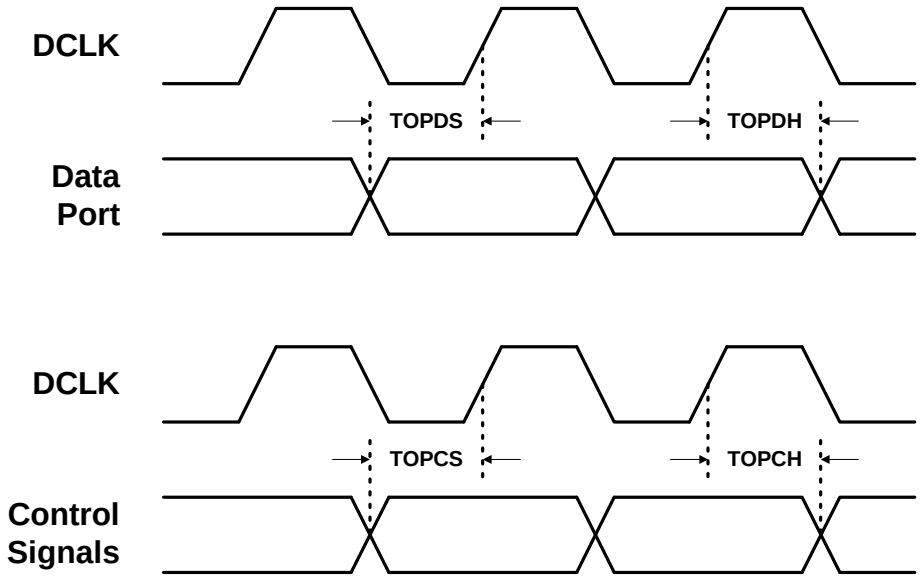


Figure 26 Output Signal Timing

Symbol	Parameter	Min	Max	Unit
TOPCS	Output control signals setup time for	4		ns
TOPCH	Output control signals hold time for	1		ns
TOPDS	Output data setup time for DCLK	4		ns
TOPDH	Output data hold time for DCLK	1		ns

1.1.25 *Serial Port Signal*

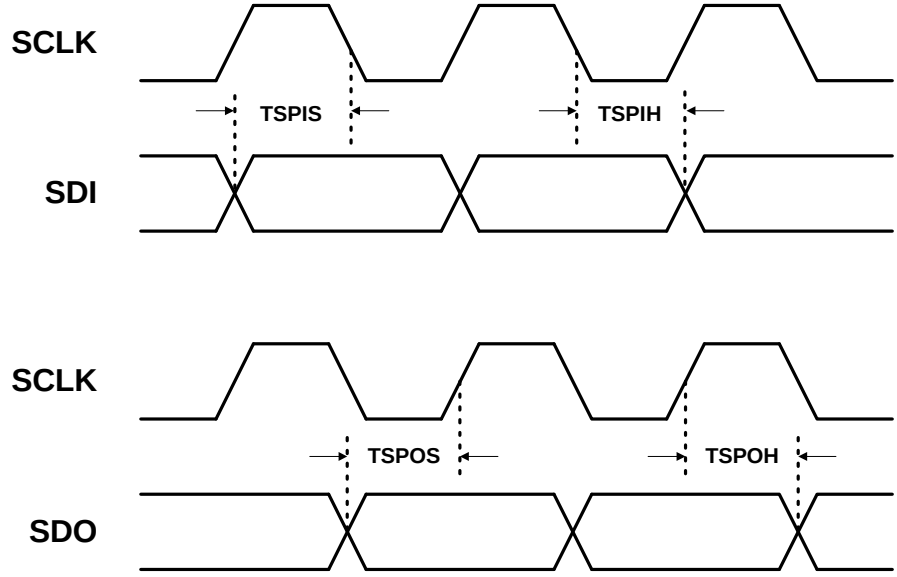
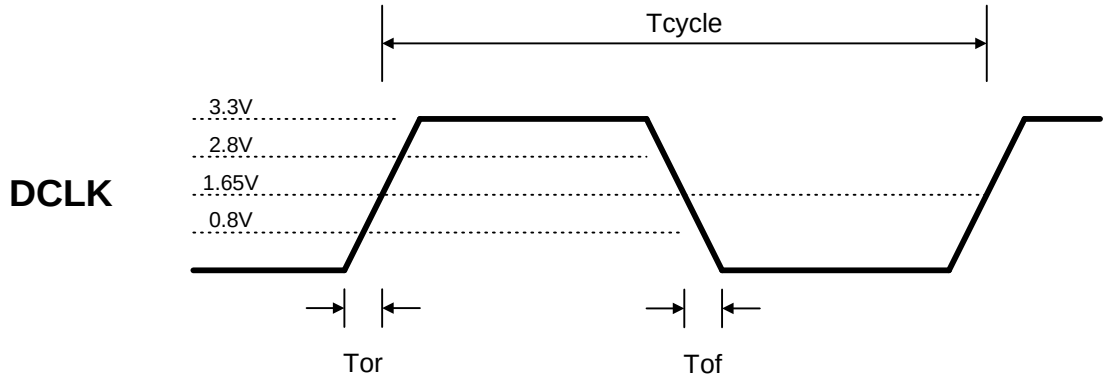


Figure 27 Serial Port Signal Timing

Symbol	Parameter	Min	Max	Unit
TSPIS	Serial port input signal setup time for	2		ns
TSPIH	Serial port input signal hold time for	8		ns
TSPOS	Serial port output signal setup time for	1/3		TCK
TSPOH	Serial port output signal for SCLK	1/2		TCK

1.1.26 *PLL*

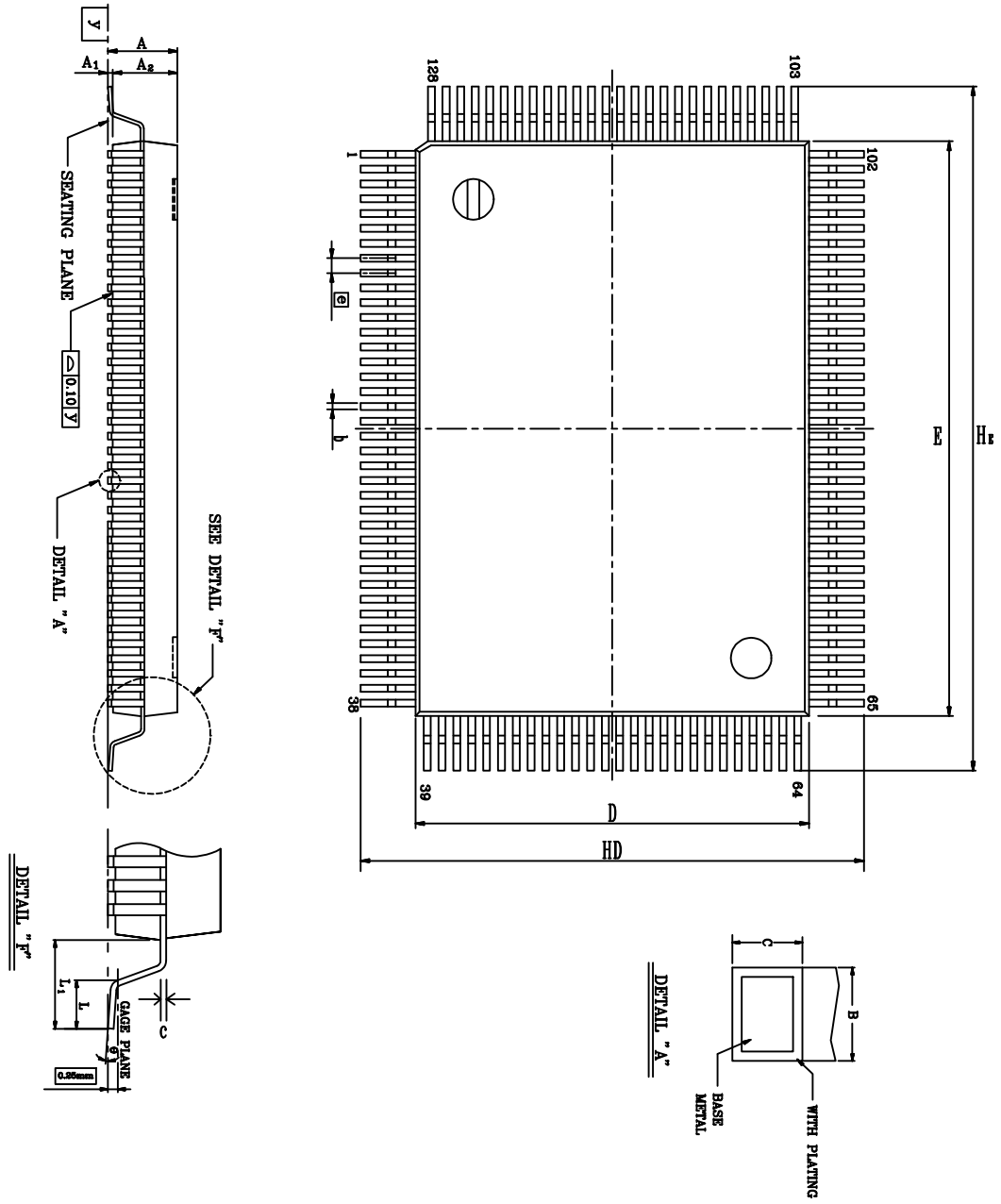


Electrical Characteristics

Characteristics	Symbol	Conditions	Mix	Type	Max	Unit
Output rise time (20pf Load)	Tor	From 0.8V to 2.0V,Vdd=3.3V			2.0	ns
Output fall time (20pf Load)	Tof	From 2.0V to 0.8V,Vdd=3.3V			2.0	ns
Duty cycle (20pf Load, at 1.5V)	Tduty	DCLK	45	50	55	%
Clock Skew (20pf Load, at 1.5V)	Tskw1	DCLK to DCLK			250	ps
Jitter, Absolute (20pf Load)	Tj1	DCLK			300	ps

Mechanical Specification

128 Pin Package



Note:

Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A	—		0.134	—	—	3.40
A_1	0.004	0.010	0.036	0.10	**0.25**	0.91
A_2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
H_D	0.665	0.677	0.689	16.90	**17.20**	17.50
H_E	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L_1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	—	—	0.004	—	—	0.10
θ	0 °	—	12 °	0 °	—	12 °

1.Dimension D & E do not include interlead flash.
2.Dimension b does not include dambar protrusion/intrusion.
3.Controlling dimension: Millimeter
4.General appearance spec. should be based on final visual inspection spec.

TITLE : 128LD QFP (14x20 mm*2) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	MAR. 25.1997
REALTEK SEMI-CONDUCTOR CO., LTD			