Lab 11

To Explain the Working of LATCHES and Implement SR & D LATCH

Note: For all the circuits in the tasks, your logic diagrams should be either hand drawn or from the software logicly. Keep them neat and legible. These circuits will be having many connections so, for simulations, make sure that you label the inputs and outputs clearly. Use Label tag in "logically". You can also edit the pictures of your outputs in "paint" easily.

Tasks

1. **Construct a logic circuit for SR LATCH. Simulate your circuit to verify the outputs. Also, show its working in terms of a timing diagram. You can take any random timing diagram and display it here. The waveforms should be hand-drawn (neatly).**

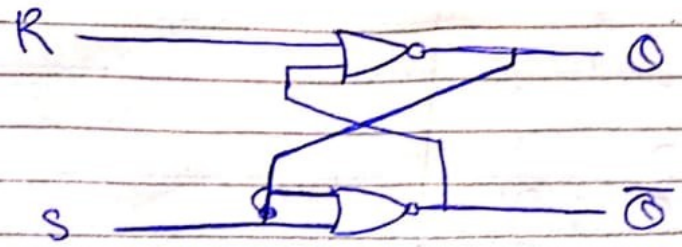
SR LATCH

a) Logic Diagram

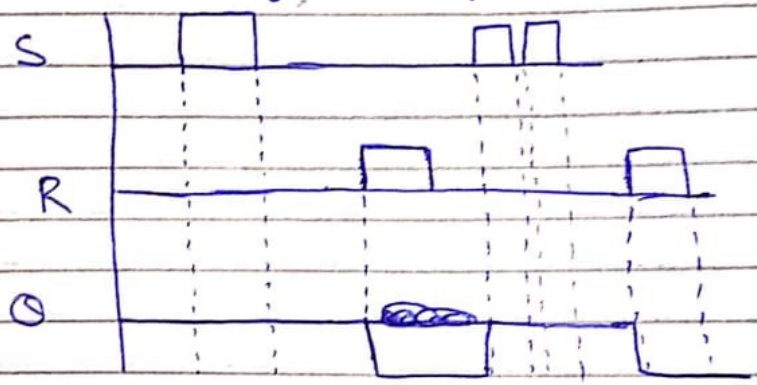
b) Truth Table

Lab Task 11

(a) Logic Diagram.



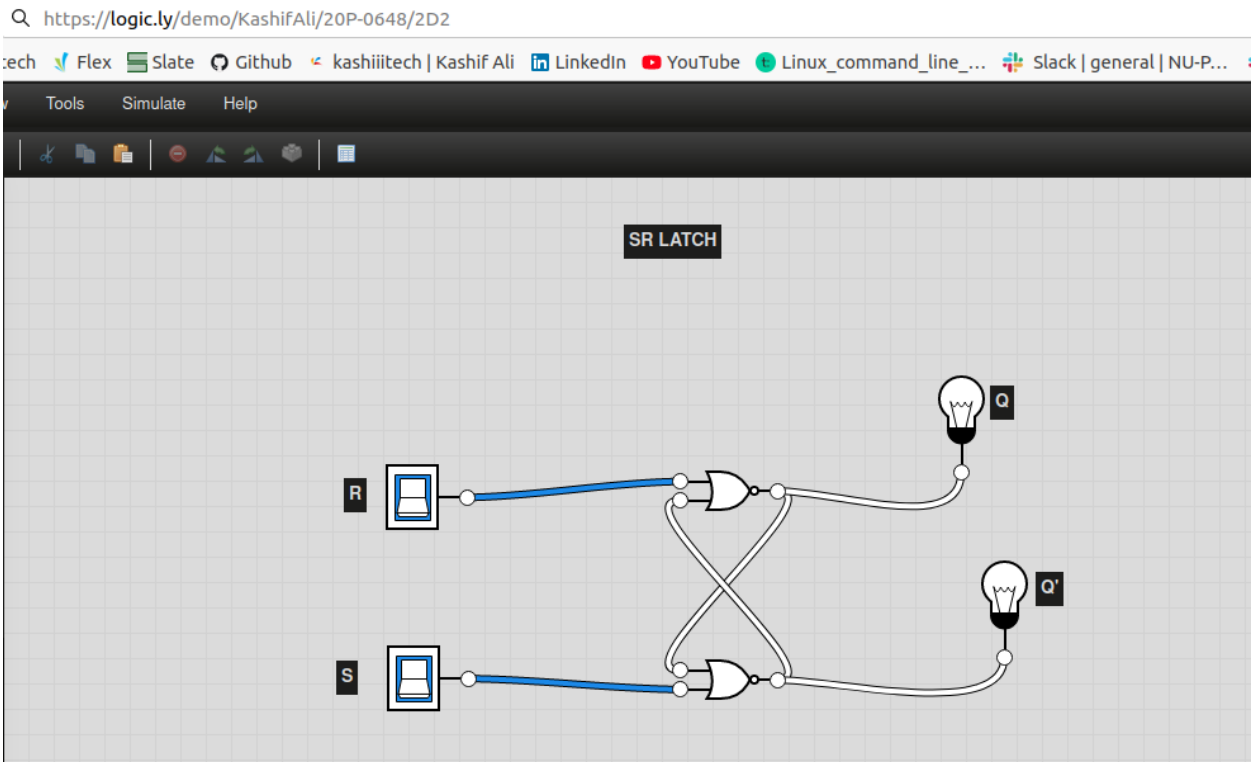
Timing diagram.



Truth Table.

S	R	Q	$\overline{Q}$
0	0	Latch	Latch
0	1	0	1
1	0	1	0
1	1	0	0

c) Software Simulation

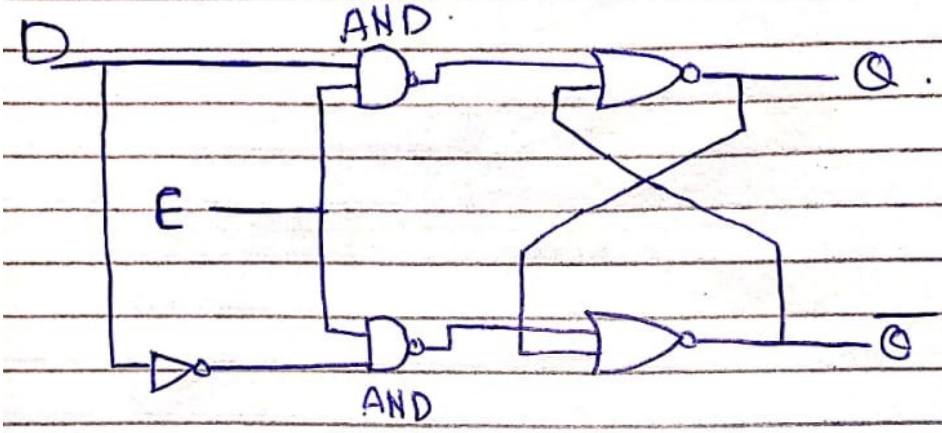


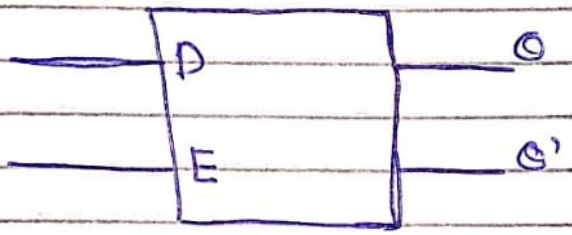
2. **Construct a logic circuit for D LATCH. Simulate your circuit to verify the outputs. Also, show its working in terms of a timing diagram. You can take any random timing diagram and display it here. The waveforms should be hand-drawn (neatly).**

a) Logic Diagram

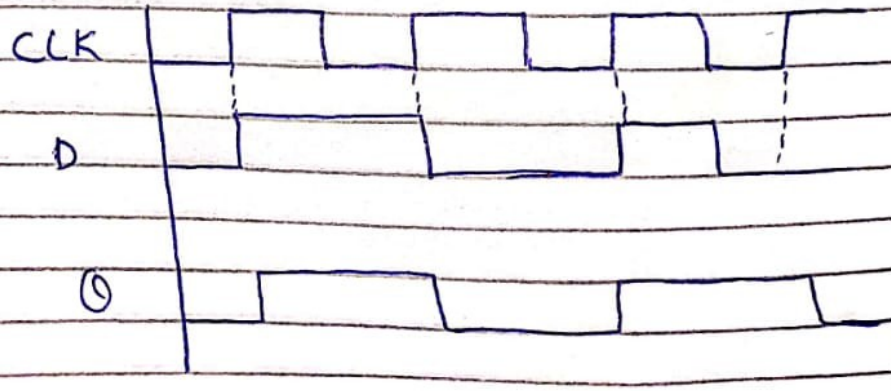
b) Truth Table

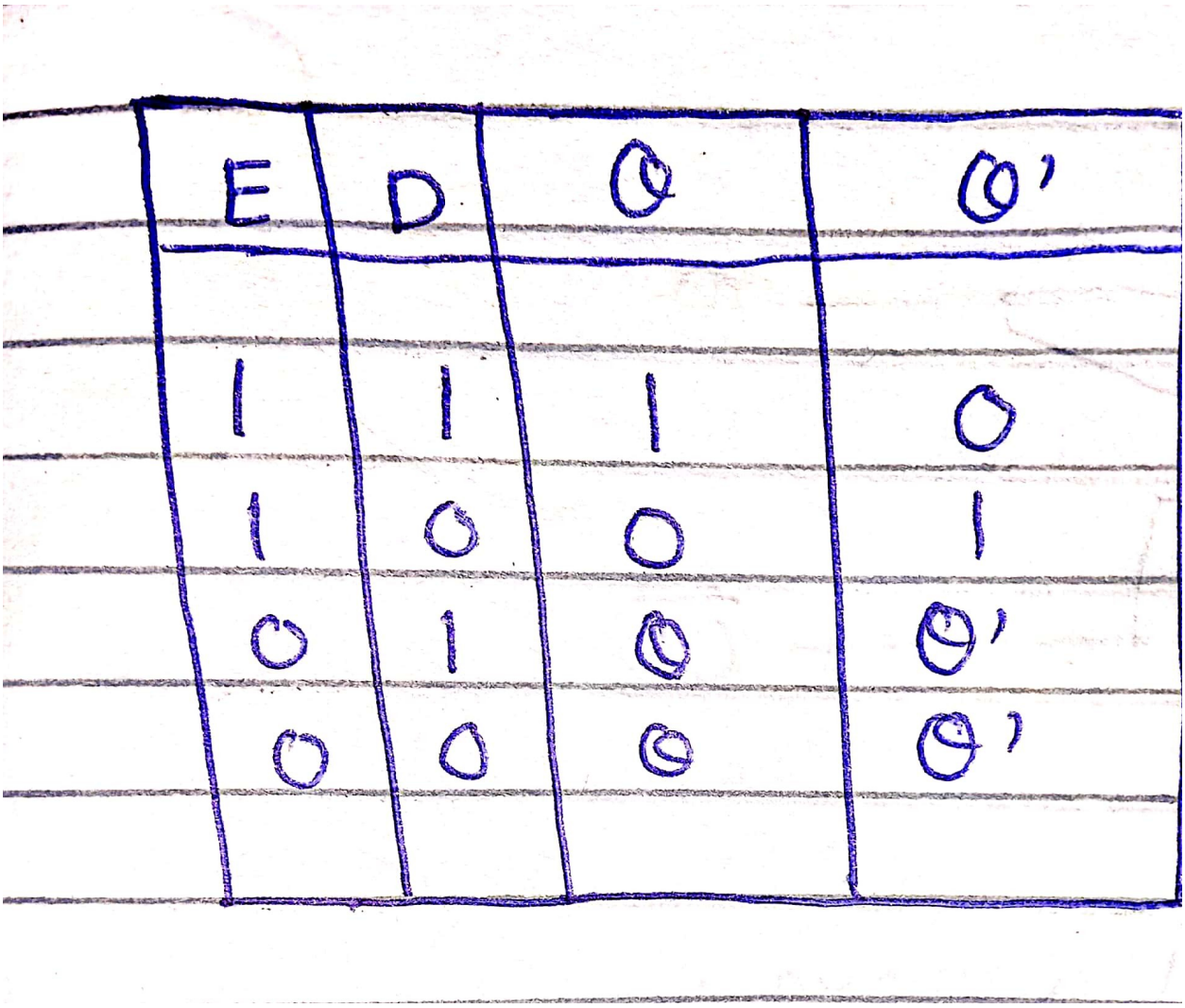
Logic Diagram.





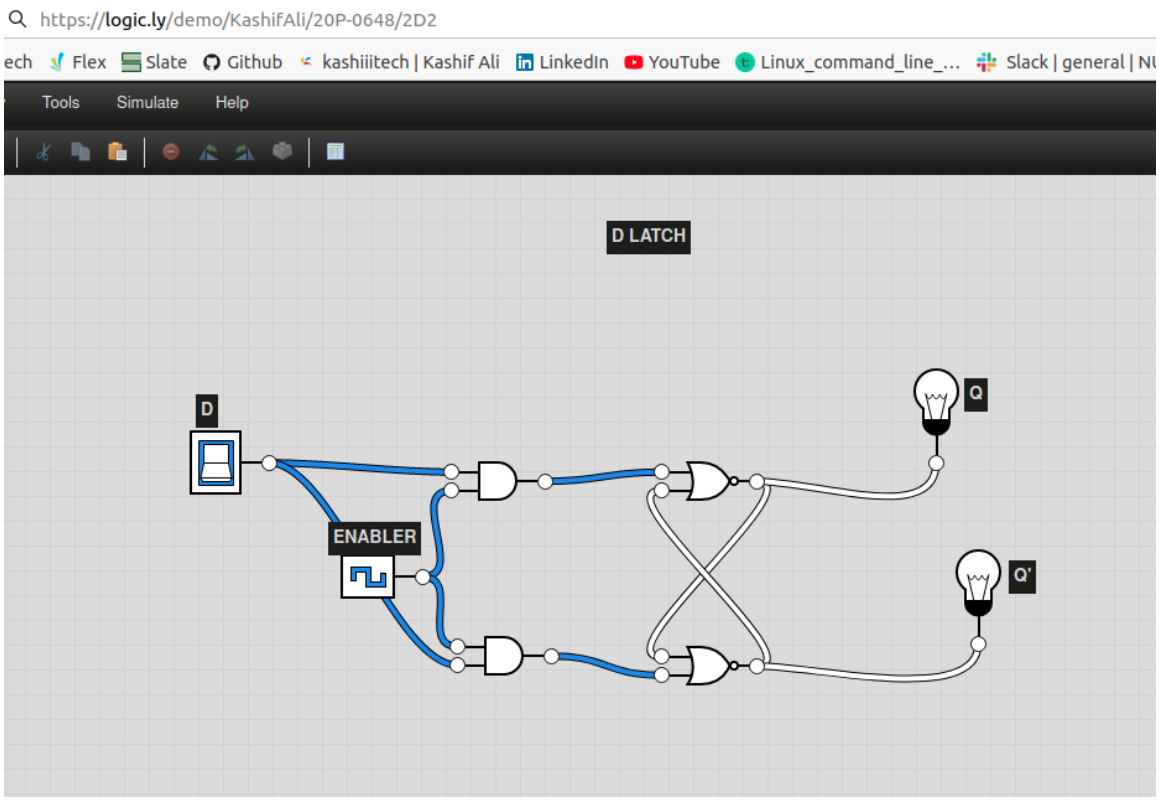
Timming Diagram.





E	D	Q	Q'
1	1	1	0
1	0	0	1
0	1	0	0'
0	0	0	0'

c) Software Simulation


https://logic.ly/demo/KashifAli/20P-0648/2D2
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Slate
Github
kashiiitech | Kashif Ali
LinkedIn
YouTube
Linux_command_line_...
Slack | general | NU
Tools
Simulate
Help
D LATCH
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