

Lab 12

To Explain the Working of Flip Flops and Implement JK Flip Flop & D Flip Flop

Note: For all the circuits in the tasks, your logic diagrams should be either hand drawn or from the software logically. Keep them neat and legible. These circuits will be having many connections so, for simulations, make sure that you label the inputs and outputs clearly. Use Label tag in “logically”. You can also edit the pictures of your outputs in “paint” easily.

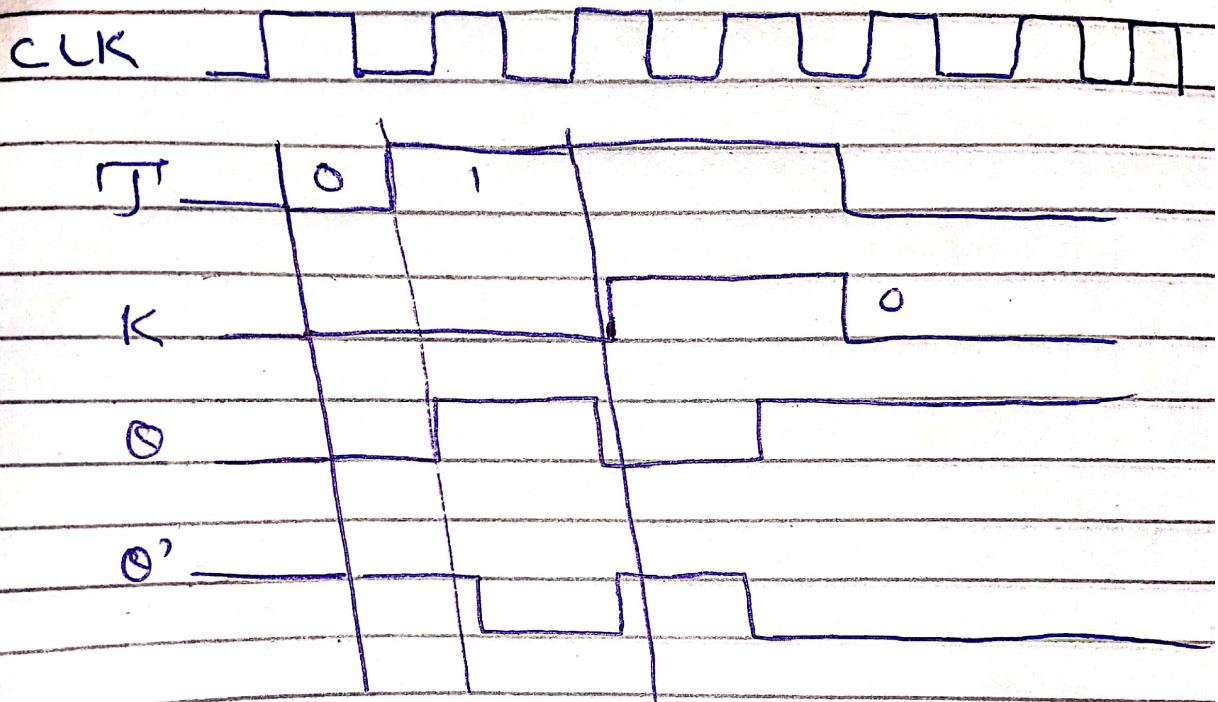
Tasks

1. Construct a logic circuit for JK Flip Flop. Simulate your circuit to verify the outputs. Also, show its working in terms of a timing diagram. You can take any random timing diagram and display it here. The waveforms should be hand-drawn (neatly).

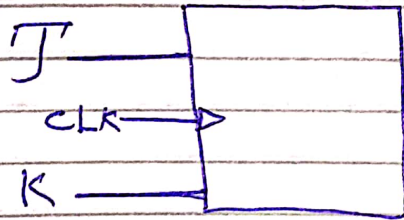
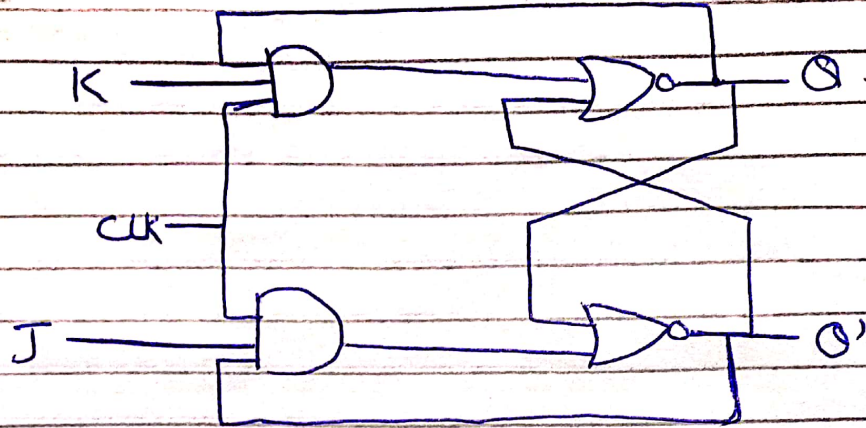
JK Flip Flop

- a) Logic Diagram
- b) Truth Table

Timing Diagram.



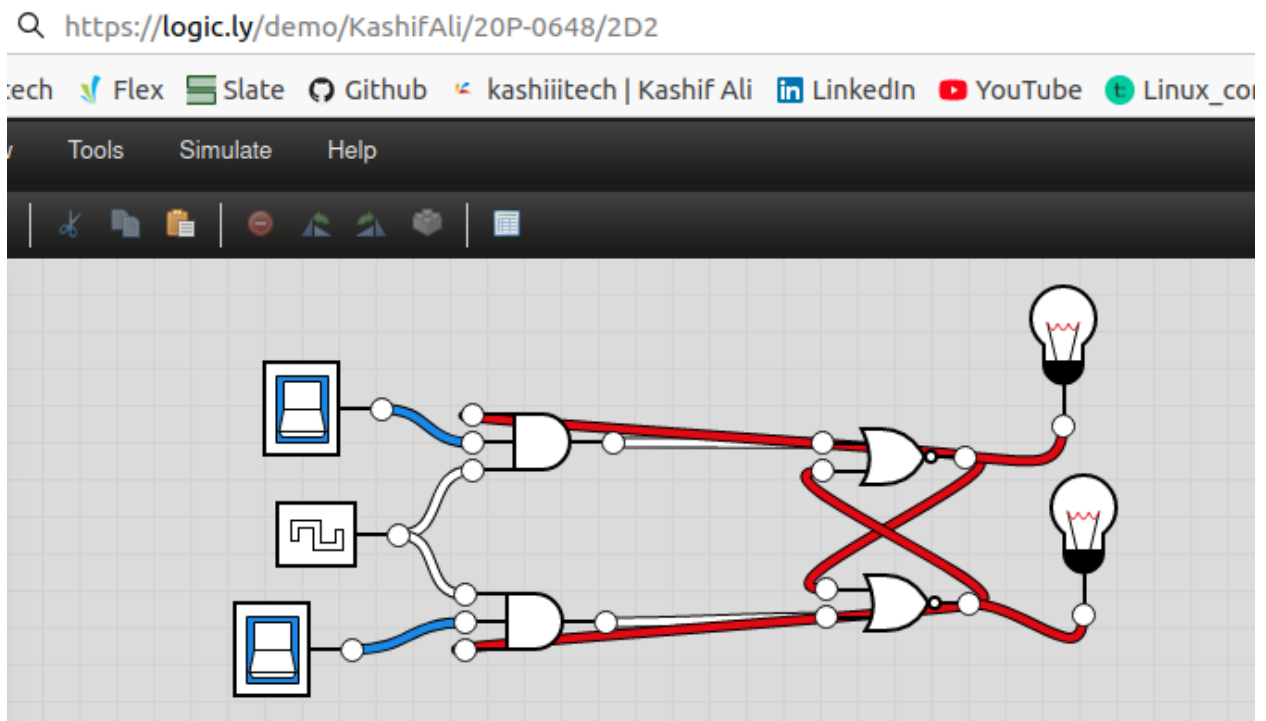
Lab-12.



Truth Table.

C	J	K	Q	Q'
0	0	0	Latch	Latch
0	0	1	0	1
0	1	0	1	0
0	1	1	Toggle	Toggle
1	0	0	Latch	Latch
1	0	1	0	1
1	1	0	1	0
1	1	1	Toggle	Toggle

c) Software Simulation



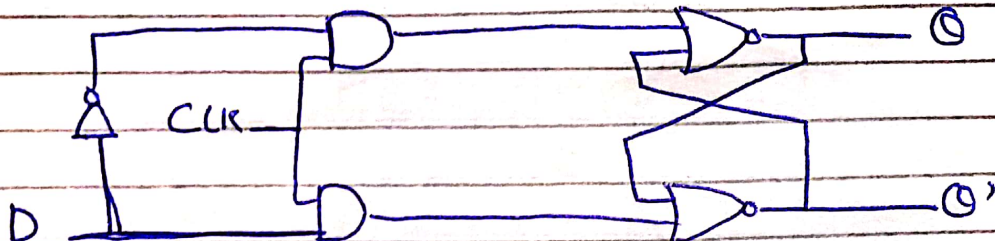
2. **Construct a logic circuit for D Flip Flop. Simulate your circuit to verify the outputs. Also, show its working in terms of a timing diagram. You can take any random timing diagram and display it here. The waveforms should be hand-drawn (neatly).**

a) Logic Diagram

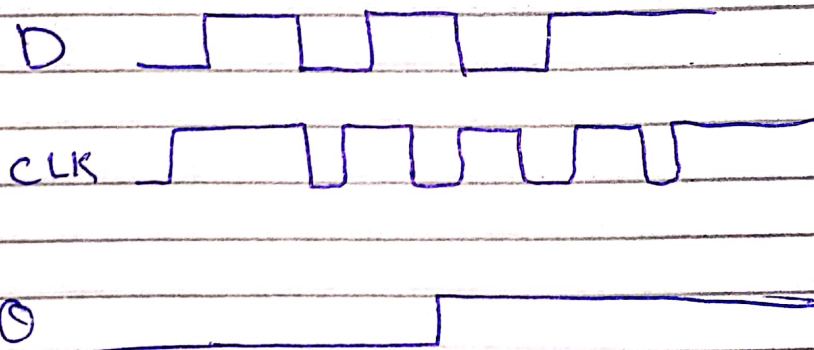
b) Truth Table

(2)

(a) Logic Diagram.



Timing Diagram.



Truth table.

D	S	R	Q
0	0	0	NC
1	0	1	0
	1	0	1
	1	1	?

c) Software Simulation

Q <https://logic.ly/demo/KashifAli/20P-0648/2D2>

