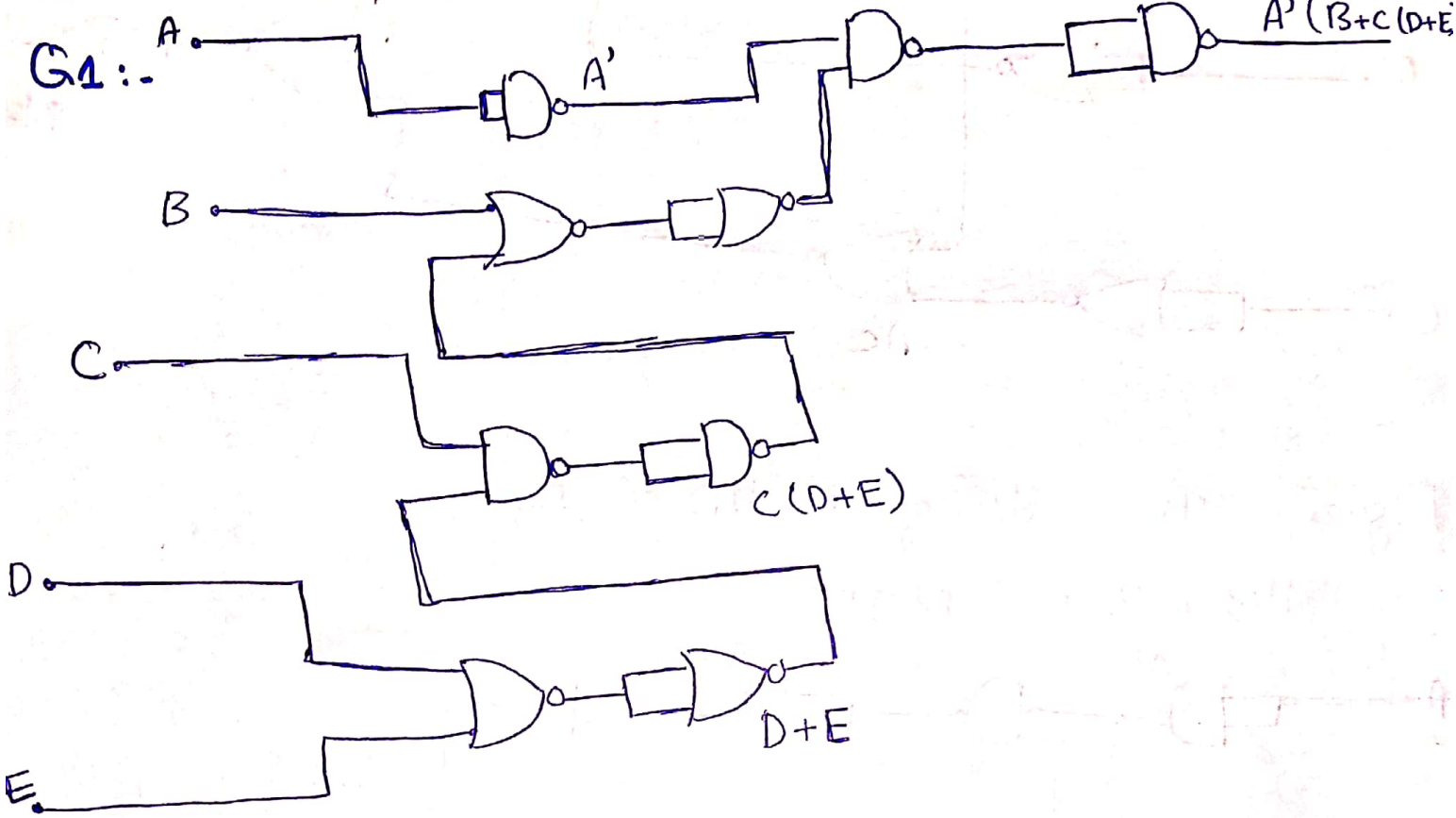
Name:- Kashif Ali Section:- 2D.

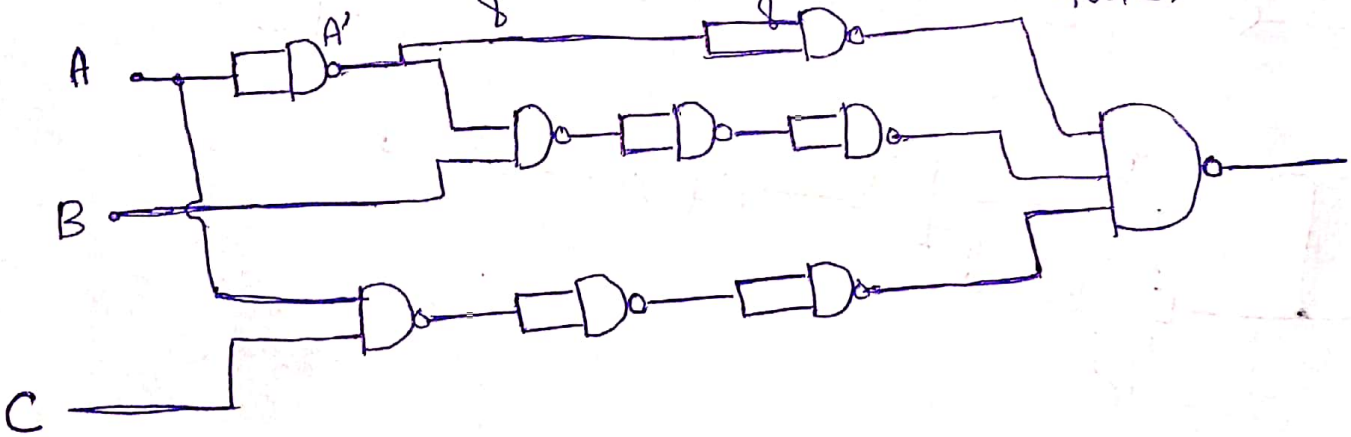
Roll No:- 20P-0648 Assignment 05

Q1:-



$$X = A' + A'B + AC$$

Q2:- Now Figer using NAND Gates.



Now Using NOR Gate

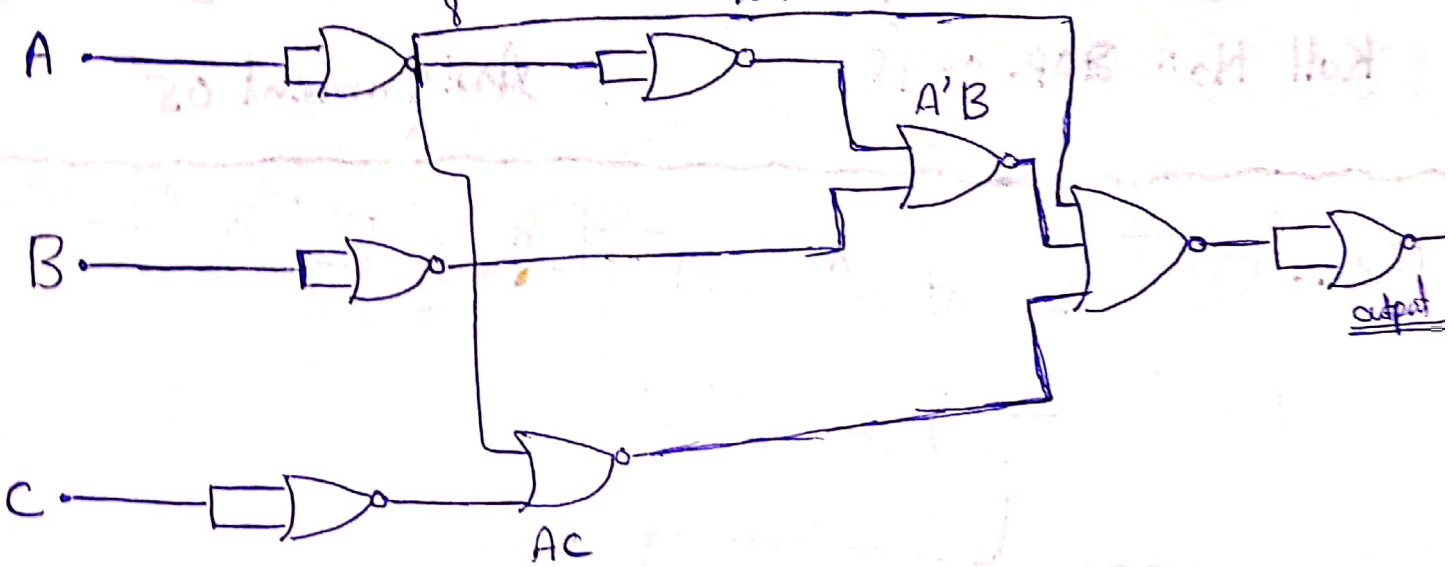
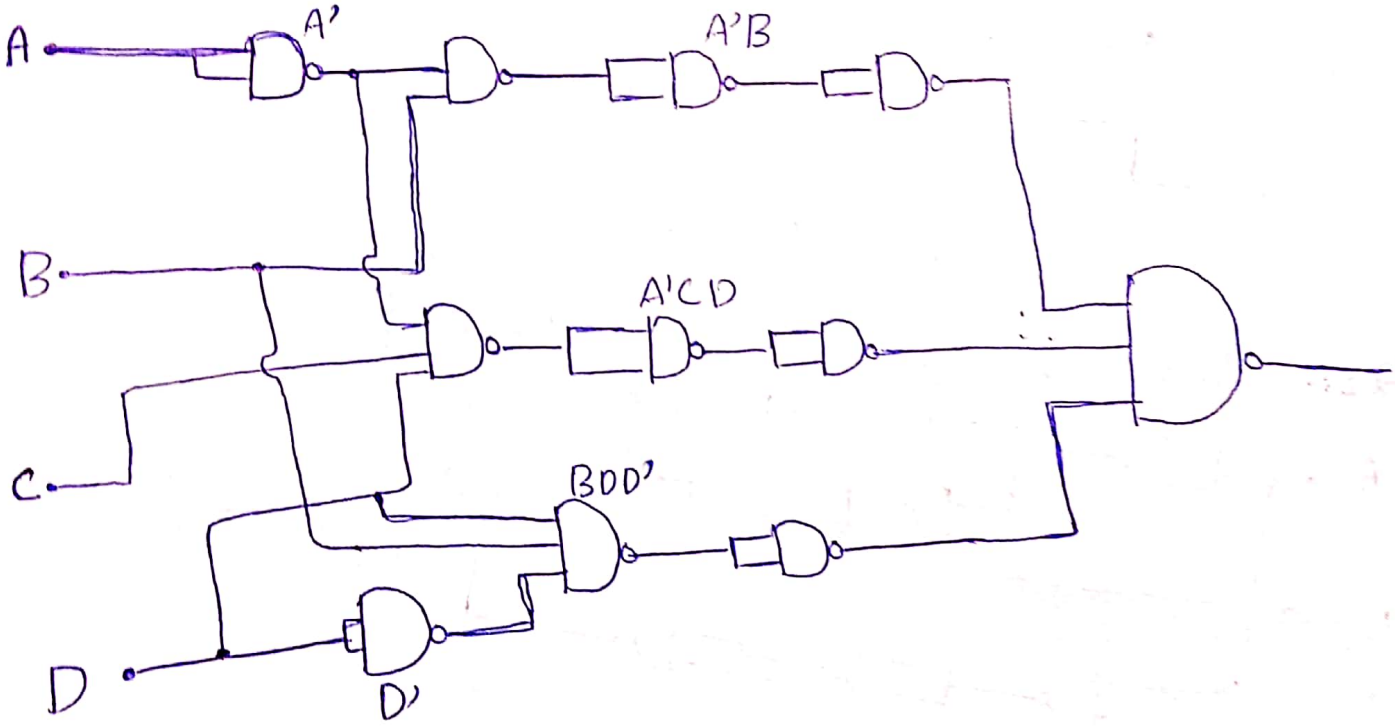


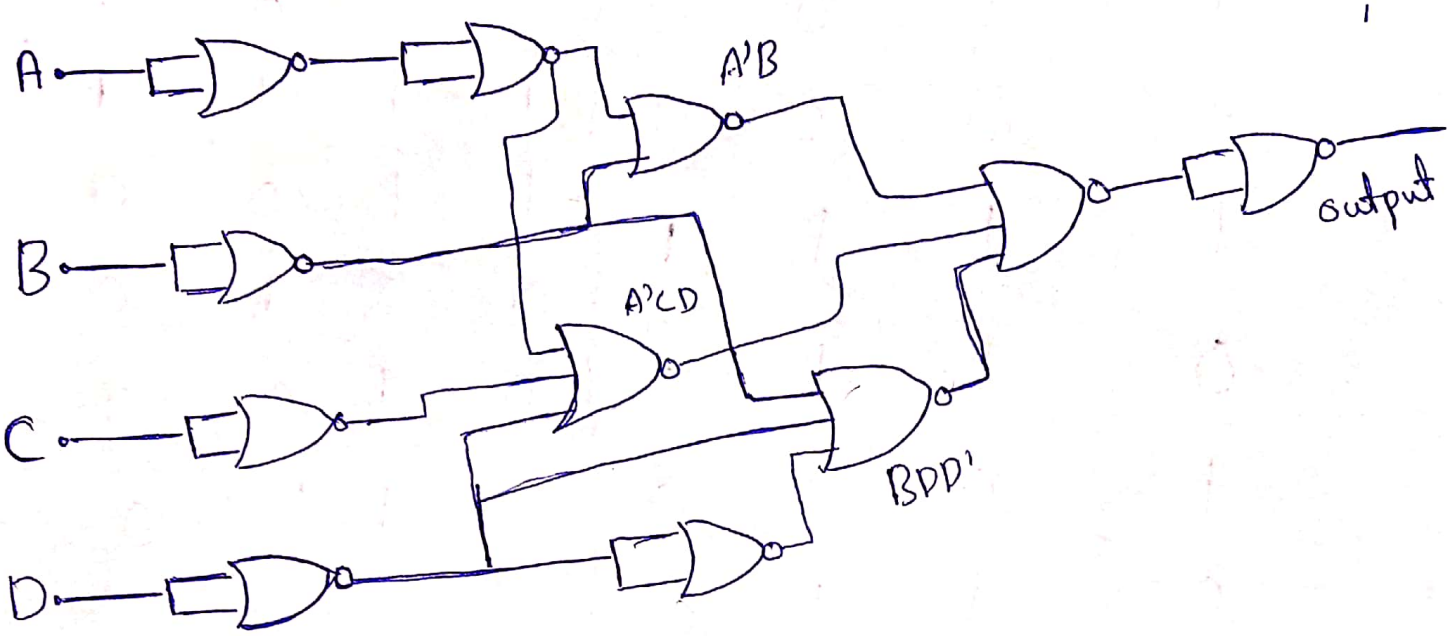
Figure (b) Using NAND Gates.

$A'B + A'CD + BDD'$



Figer (b) using NOR Gates.

$A'B + A'CD + BDD''$



QNo3:

JK flip-flop is basically a flip-flop that allows only one of its Inputs terminals, which can be Set or reset at anytime under normal Switching. So if it removes the Invalid State. that occurs in the SR flip-flop. however when both the Inputs J and K are high means (1). when the clock input rises it will change as its changing Position accordingly and when the Inputs are high (1) The Clock will "Toggle"

Q NO4:-

J_1	J_2	J_3	J	K_1	K_2	K_3	K
1	0	0	0	0	0	1	0
1	1	0	0	1	0	0	0
1	0	0	0	1	1	1	1
0	0	0	0	1	1	0	0
1	1	1	1	0	0	1	0
0	1	1	0	0	1	0	0
1	0	1	0	0	1	1	0
0	1	1	0				

J	K	Q
0	0	0
0	1	0
0	0	0
1	0	1
0	0	1
0	0	1

Q No 4:-