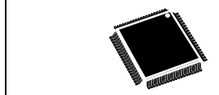
STM32F030x4 STM32F030x6 STM32F030x8

Value-line ARM-based 32-bit MCU with 16 to 64-KB Flash, timers, ADC, communication interfaces, 2.4-3.6 V operation

Datasheet – target specification

Features

- Core: ARM® 32-bit Cortex™-M0 CPU, frequency up to 48 MHz
- Memories
  - 16 to 64 Kbytes of Flash memory
  - 4 to 8 Kbytes of SRAM with HW parity checking
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.4 V to 3.6 V
  - Power-on/Power down reset (POR/PDR)
  - Low power modes: Sleep, Stop, Standby
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
- Up to 55 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 36 I/Os with 5 V tolerant capability
- 5-channel DMA controller
- 1 x 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply from 2.4 up to 3.6 V
- Up to 10 timers
  - One 16-bit 7-channel advanced-control timer for 6 channels PWM output, with deadtime generation and emergency stop
  - One 16-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - One 16-bit timer, with 2 IC/OC, 1 OCN, deadtime generation and emergency stop
  - Two 16-bit timers, each with IC/OC and OCN, deadtime generation, emergency stop and modulator gate for IR control
  - One 16-bit timer with 1 IC/OC



LQFP64 10x10 mm
LQFP48 7x7 mm
LQFP32 7x7 mm

TSSOP20

  - One 16-bit basic timer
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- Communication interfaces
  - Up to two I²C interfaces: one supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink
  - Up to two USARTs supporting master synchronous SPI and modem control; one with auto baud rate detection
  - Up to two SPIs (18 Mbit/s) with 4 to 16 programmable bit frame
- Serial wire debug (SWD)

Table 1. Device summary

Reference	Part number
STM32F030x4	STM32F030F4
STM32F030x6	STM32F030C6, STM32F030K6
STM32F030x8	STM32F030C8, STM32F030R8

STM32F030x4 STM32F030x6 STM32F030x8

基于 ARM 的超值 32 位 MCU，具有 16 至 64 KB 闪存、定时器、 ADC 、通信接口、 2.4-3.6 V 工作电压

数据表 – 目标规格

特性 • 内核：ARM® 32位 Cortex™-M0 CPU，频率高达 48 MHz• 内存 – 16 至 64 KB 闪存 – 4 至 8 KB SRAM，带硬件奇偶校验

- CRC 计算单元
- 复位和电源管理 – 电压范围：2.4V 至 3.6V – 加电 / 断电复位 (POR/PDR) – 低功耗模式：睡眠、停止、待机
- 时钟管理
  – 4 至 32 MHz 晶体振荡器 – 用于带校准的 RTC 的 32kHz 振荡器 – 内部 8 MHz RC，带 x6 PLL 选项 – 内部 40 kHz RC 振荡器
- 多达 55 个快速 I/O
  – 全部可映射到外部中断向量 – 多达 36 个 I/O，具有 5 V 耐受能力
- 5- 通道 DMA 控制器
- 1 x 12 位、 1.0 µs ADC （最多 16 个通道）
  – 转换范围：0 至 3.6 V – 2.4 至 3.6 V 的独立模拟电源
- 最多 10 个计时器
  – 1 个 16 位 7 通道高级控制定时器，用于 6 通道 PWM 输出，具有死区生成和紧急停止 – 1 个 16 位定时器，最多 4 个 IC/OC，可用于 IR 控制解码 – 1 个 16 位定时器，具有 2 个 IC/OC 、 1 个 OCN 、死区生成和紧急停止 – 2 个 16 位定时器，每个定时器都有 IC/OC 和 OCN 、死区生成、紧急停止和用于 IR 控制的调制器门 – 1 个带 1 个 IC/OC 的 16 位定时器

LQFP64 10x10 mm
LQFP48 7x7 mm
LQFP32 7x7 mm

TSSOP20

  – 1 个 16 位基本定时器 – 独立和系统看门狗定时器 – SysTick 定时器：24 位递减计数器
- 带有闹钟和定期从停止 / 待机状态唤醒的日历 RTC
- Communication interfaces
  - Up to two I²C interfaces: one supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink
  - Up to two USARTs supporting master synchronous SPI and modem control; one with auto baud rate detection
  - Up to two SPIs (18 Mbit/s) with 4 to 16 programmable bit frame
- 串行线调试（ SWD ）

表 1. 器件摘要

Reference	Part number
STM32F030x4	STM32F030F4
STM32F030x6	STM32F030C6, STM32F030K6
STM32F030x8	STM32F030C8, STM32F030R8

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F030x microcontrollers.

This STM32F030x4, STM32F030x6, and STM32F030x8 datasheet should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM Cortex™-M0 core, please refer to the Cortex™-M0 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0432c/index.html.

1 介绍

该数据表提供了 STM32F030x 微控制器的订购信息和机械设备特性。

本 STM32F030x4 、 STM32F030x6 和 STM32F030x8 数据表应与 STM32F0xxxx 参考手册 (RM0091) 一起阅读。该参考手册可从 STMicroElectronics 网站 www.st.com 获取。

有关 ARM Cortex™-M0 内核的信息，请参阅 Cortex™-M0 技术参考手册，该手册可从 www.arm.com 网站获取，地址如下：http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0432c/index.html。

2 Description

The STM32F030x microcontroller incorporates the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 64 Kbytes of Flash memory and up to 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I^2Cs, up to two SPIs, and up to two USARTs), one 12-bit ADC, up to 6 general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F030x microcontroller operates in the -40 to +85 °C temperature range, from a 2.4 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F030x microcontroller includes devices in four different packages ranging from 20 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F030x peripherals proposed.

These features make the STM32F030x microcontroller suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming platforms, e-bikes, consumer appliances, printers, scanners, alarm systems, video intercoms, and HVACs.

2 说明

STM32F030x 微控制器集成了以 48 MHz 频率运行的高性能 ARM Cortex™-M0 32 位 RISC 内核、高速嵌入式存储器（高达 64 KB 闪存和高达 8 KB SRAM ）以及各种增强型外设和 I/O。所有器件均提供标准通信接口（最多两个 I^2C 、最多两个 SPI 和最多两个 USART ）、一个 12 位 ADC 、最多 6 个通用 16 位定时器和一个高级控制 PWM 定时器。

STM32F030x 微控制器的工作温度范围为 -40 至 +85 °C，电源电压为 2.4 至 3.6 V。一套全面的节能模式允许设计低功耗应用。

STM32F030x 微控制器包括采用 20 引脚到 64 引脚四种不同封装的器件。根据所选择的设备，包括不同的外围设备组。以下描述概述了建议的 STM32F030x 外设的全系列。

这些功能使 STM32F030x 微控制器适用于各种应用，例如应用控制和用户界面、手持设备、A/V 接收器和数字电视、 PC 外设、游戏平台、电动自行车、消费类电器、打印机、扫描仪、报警系统、可视对讲机和 HVAC。

Table 2. STM32F030x device features and peripheral counts

Peripheral		STM32F030F4	STM32F030K6	STM32F030C6/C8		STM32F030R8
Flash (Kbytes)		16	32	32	64	64
SRAM (Kbytes)		4	4	4	8	8
Timers	Advanced control	1 (16-bit)				
	General purpose	4 (16-bit)(1)	4 (16-bit)(1)	4 (16-bit)(1)	5 (16-bit)	5 (16-bit)
	Basic	-	-	-	1 (16-bit)	1 (16-bit)
Comm. interfaces	SPI	1(2)	1(2)	1(2)	2	2
	I^2C	1(3)	1(3)	1(3)	2	2
	USART	1(4)	1(4)	1(4)	2	2
12-bit synchronized ADC (number of channels)		1 (11 channels)	1 (12 channels)	1 (12 channels)		1 (18 channels)
GPIOs		15	26	39		55
Max. CPU frequency		48 MHz				
Operating voltage		2.4 to 3.6 V				
Operating temperature		Ambient operating temperature: -40 °C to 85 °C				
Packages		TSSOP20	LQFP32	LQFP48		LQFP64

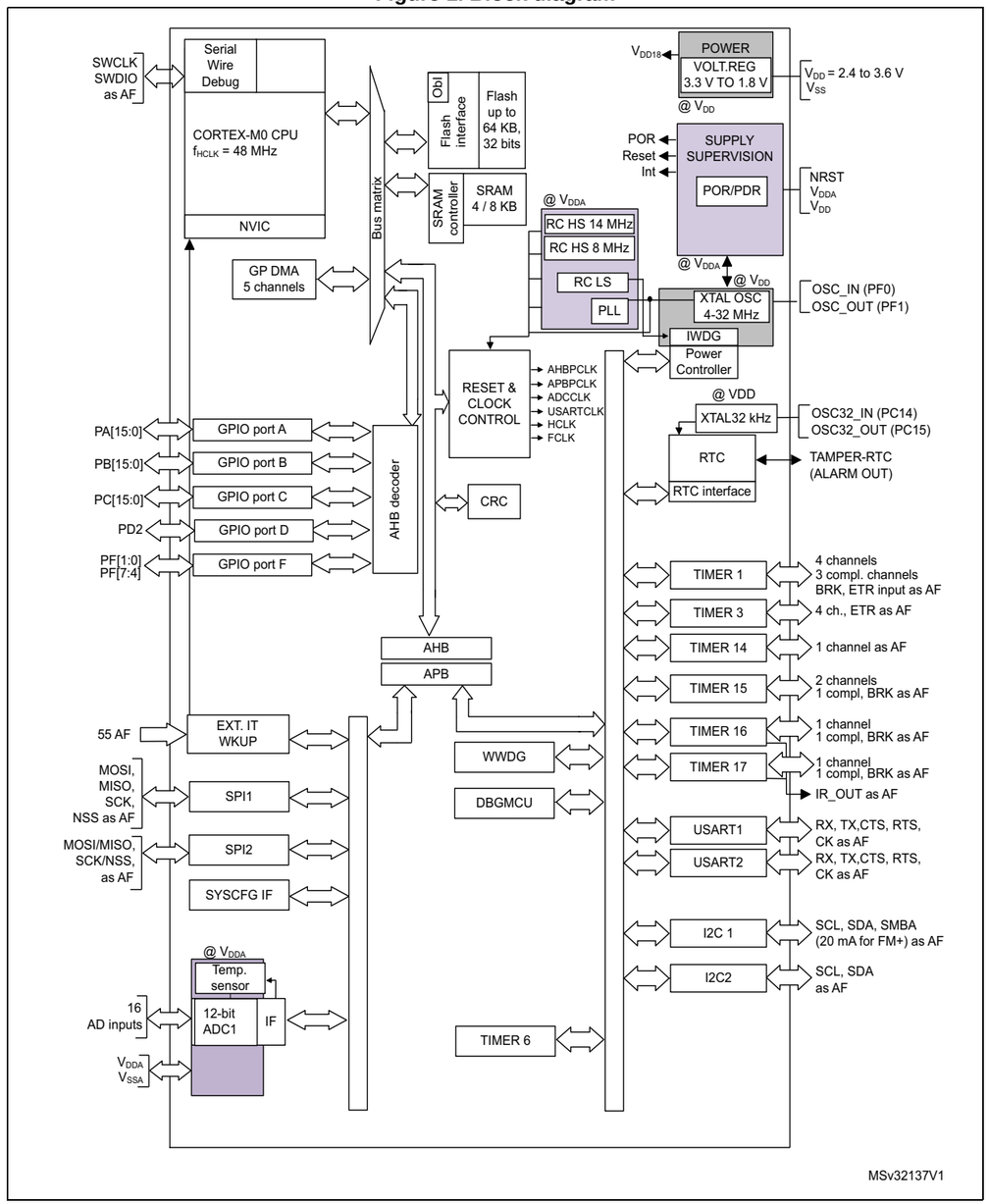
1. TIM15 is not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART2 is not present.

表 2. STM32F030x 器件特性和外设数量

Peripheral		STM32F030F4	STM32F030K6	STM32F030C6/C8		STM32F030R8
Flash (Kbytes)		16	32	32	64	64
SRAM (Kbytes)		4	4	4	8	8
Timers	Advanced control	1 (16-bit)				
	General purpose	4 (16-bit)(1)	4 (16-bit)(1)	4 (16-bit)(1)	5 (16-bit)	5 (16-bit)
	Basic	-	-	-	1 (16-bit)	1 (16-bit)
Comm. interfaces	SPI	1(2)	1(2)	1(2)	2	2
	I^2C	1(3)	1(3)	1(3)	2	2
	USART	1(4)	1(4)	1(4)	2	2
12-bit synchronized ADC (number of channels)		1 (11 channels)	1 (12 channels)	1 (12 channels)		1 (18 channels)
GPIOs		15	26	39		55
Max. CPU frequency		48 MHz				
Operating voltage		2.4 to 3.6 V				
Operating temperature		Ambient operating temperature: -40 °C to 85 °C				
Packages		TSSOP20	LQFP32	LQFP48		LQFP64

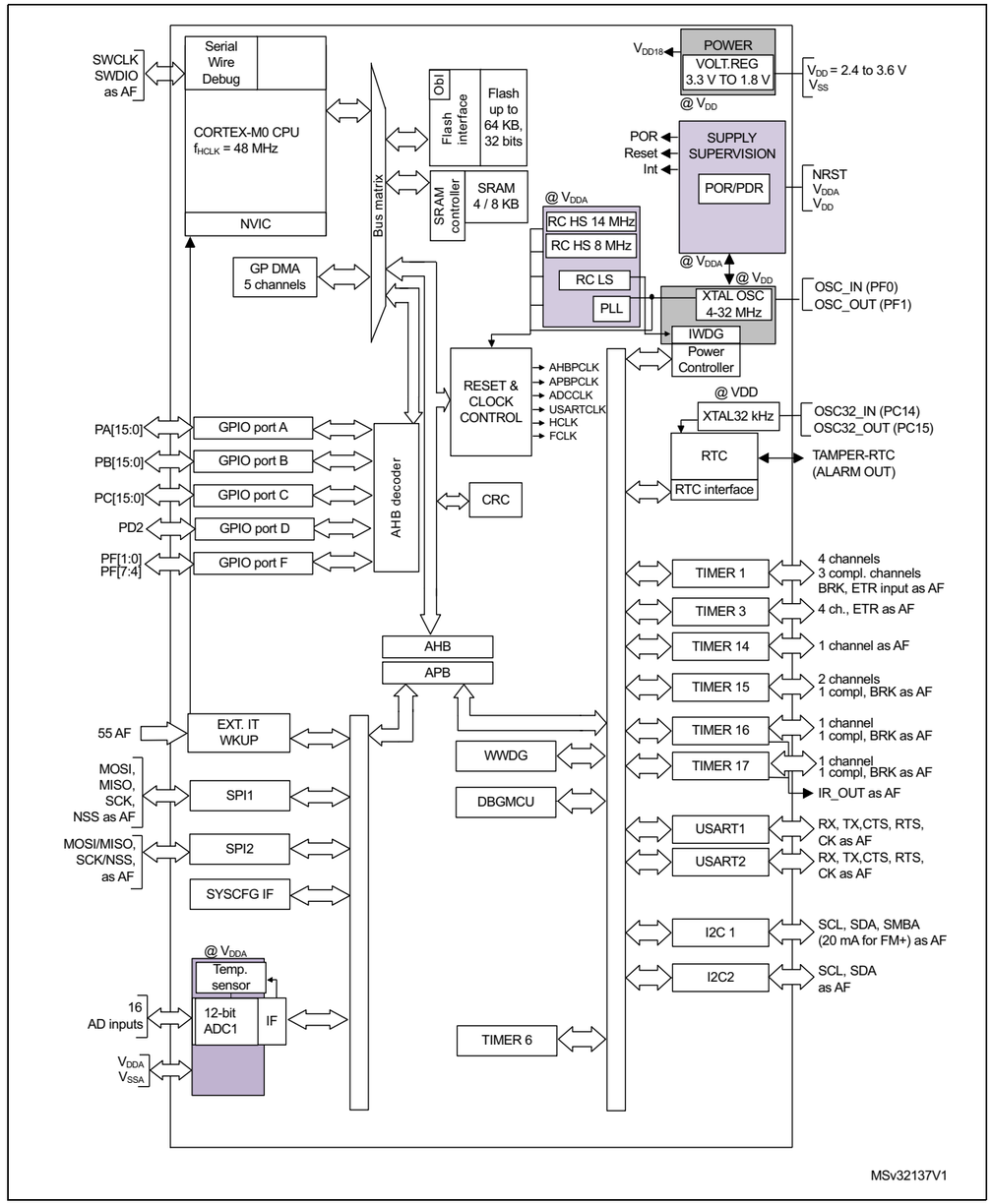
1. TIM15 is not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART2 is not present.

Figure 1. Block diagram



1. TIMER6, TIMER15, SPI2, USART2 and I2C2 are available on STM32F030x8 devices only.

图 1. 框图



1. TIMER6 、 TIMER15 、 SPI2 、 USART2 和 I2C2 仅在 STM32F030x8 器件上可用。

3 Functional overview

3.1 ARM® Cortex™-M0 core with embedded Flash and SRAM

The ARM Cortex™-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- Up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 64 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

3 Functional overview

3.1 带有嵌入式 Flash 和 SRAM 的 ARM® CortexTM-M0 内核

ARM Cortex™-M0 处理器是用于嵌入式系统的最新一代 ARM 处理器。它的开发目的是提供一个满足 MCU 实施需求的低成本平台，具有减少的引脚数和低功耗，同时提供出色的计算性能和先进的系统中断响应。

ARM Cortex™-M0 32 位 RISC 处理器具有卓越的代码效率，可在通常与 8 位和 16 位设备相关的内存大小中提供 ARM 内核所期望的高性能。

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

图 1 显示了该器件系列的总体框图 .

3.2 记忆

该装置具有以下特点：

• 以 CPU 时钟速度访问（读 / 写）高达 8 KB 的嵌入式 SRAM，0 等待状态，并具有嵌入式奇偶校验功能，并为故障关键型应用生成异常。• 非易失性存储器分为两个阵列： – 用于程序和数据的 16 至 64 KB 嵌入式闪存 – 选项字节 选项字节用于对存储器进行写保护（粒度为 4 KB ）和 / 或读出 - 使用以下选项保护整个存储器： – 级别 0：无读出保护 – 级别 1：存储器读出保护，如果连接了调试功能或选择了在 RAM 中启动，则无法读取或写入闪存 – 级别 2：禁用芯片读出保护、调试功能（ Cortex-M0 串行线）和在 RAM 中启动选择

3.3 启动模式

启动时，启动引脚和启动选择器选项位用于选择三个启动选项之一：

• 从用户闪存启动 • 从系统内存启动 • 从嵌入式 SRAM 启动

引导加载程序位于系统内存中。它用于通过使用引脚 PA14/PA15 或 PA9/PA10 上的 USART 对闪存进行重新编程。

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = 2.4 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} = 2.4 to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

3.5.3 Voltage regulator

The regulator has three operating modes: main (MR), low power (LPR) and power down.

- MR is used in normal operating mode (Run)
- LPR can be used in Stop mode where the power demand is reduced
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

3.4 循环冗余校验计算单元（CRC）

CRC （循环冗余校验）计算单元用于从 32 位数据字和 CRC-32 （以太网）多项式中获取 CRC 代码。

在其他应用中，基于 CRC 的技术用于验证数据传输或存储的完整性。在 EN/IEC 60335-1 标准范围内，它们提供了一种验证闪存完整性的方法。 CRC 计算单元帮助在运行时计算软件的签名，以与在链接时生成并存储在给定存储器位置的参考签名进行比较。

3.5 电源管理

3.5.1 供电方案

- VDD = 2.4 至 3.6 V：I/O 和内部稳压器的外部电源。通过 VDD 引脚从外部提供。
- VDDA = 2.4 至 3.6 V：ADC 、复位模块、 RC 和 PLL 的外部模拟电源。 VDDA 电压电平必须始终大于或等于 VDD 电压电平，并且必须首先提供。

For 有关如何连接电源引脚的更多详细信息，请参阅图 10：电源方案 *e*.

3.5.2 电源监控器

该器件具有集成的上电复位 (POR) 和掉电复位 (PDR) 电路。它们始终处于活动状态，并确保在 2V 阈值以上正常工作。当监控的电源电压低于指定阈值 VPOR/PDR 时，器件保持复位模式，无需外部复位电路。

- POR 仅监控 VDD 电源电压。在启动阶段，要求 VDDA 首先到达并大于或等于 VDD。
- PDR 监控 VDD 和 VDDA 电源电压，但如果应用设计确保 VDDA 高于或等于 VDD，则可以禁用 VDDA 电源监控器（通过编程专用选项位）以降低功耗。

3.5.3 电压调节器

该稳压器具有三种工作模式：主模式 (MR) 、低功耗模式 (LPR) 和掉电模式。

- MR 用于正常工作模式（ Run ）• LPR 可用于 Stop 模式，降低功耗 • Power down 用于 Standby 模式：稳压器输出处于高阻抗：内核电路掉电，导致零功耗（但寄存器和 SRAM 的内容丢失）

该调节器在复位后始终启用。它在待机模式下被禁用，提供高阻抗输出。

3.5.4 Low-power modes

The STM32F030x microcontroller supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines or the RTC alarm.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for the Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

3.5.4 低功耗模式

STM32F030x 微控制器支持三种低功耗模式，以实现低功耗、短启动时间和可用唤醒源之间的最佳折衷：

- 睡眠模式

  在睡眠模式下，只有 CPU 停止运行。当中断 / 事件发生时，所有外设继续运行并可以唤醒 CPU。

- 停止模式

  停止模式可实现非常低的功耗，同时保留 SRAM 和寄存器的内容。 1.8 V 域中的所有时钟均停止，PLL 、 HSI RC 和 HSE 晶体振荡器被禁用。电压调节器也可以置于正常或低功耗模式。

  可以通过任何 EXTI 线将器件从停止模式唤醒。 EXTI 线路源可以是 16 条外部线路之一或 RTC 闹钟。

- 待机模式

  待机模式用于实现最低功耗。内部稳压器关闭，从而整个 1.8 V 域断电。 PLL 、 HSI RC 和 HSE 晶体振荡器也被关闭。进入待机模式后，除待机电路外，SRAM 和寄存器内容都会丢失。

  当外部复位（ NRST 引脚）、 IWDG 复位、 WKUP 引脚上的上升沿或 RTC 闹钟发生时，器件退出待机模式。

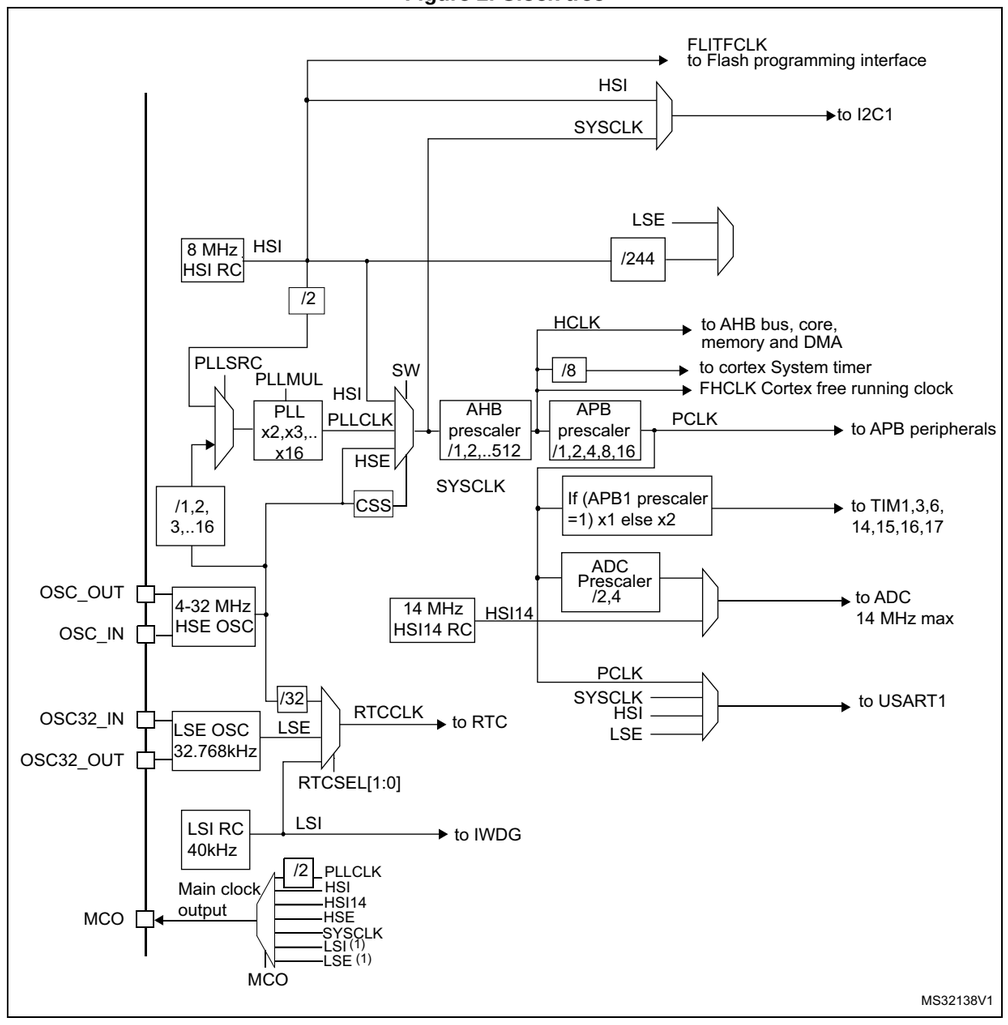
笔记： RTC 、 IWDG 和相应的时钟源不会因进入停止或待机模式而停止。

3.6 时钟和启动

系统时钟选择在启动时执行，但内部 RC 8 MHz 振荡器在复位时被选择作为默认 CPU 时钟。可以选择外部 4-32 MHz 时钟，在这种情况下会监视其是否出现故障。如果检测到故障，系统会自动切换回内部 RC 振荡器。如果启用，则会生成软件中断。同样，必要时（例如，间接使用的外部晶体、谐振器或振荡器发生故障时），可以使用 PLL 时钟条目的完整中断管理。

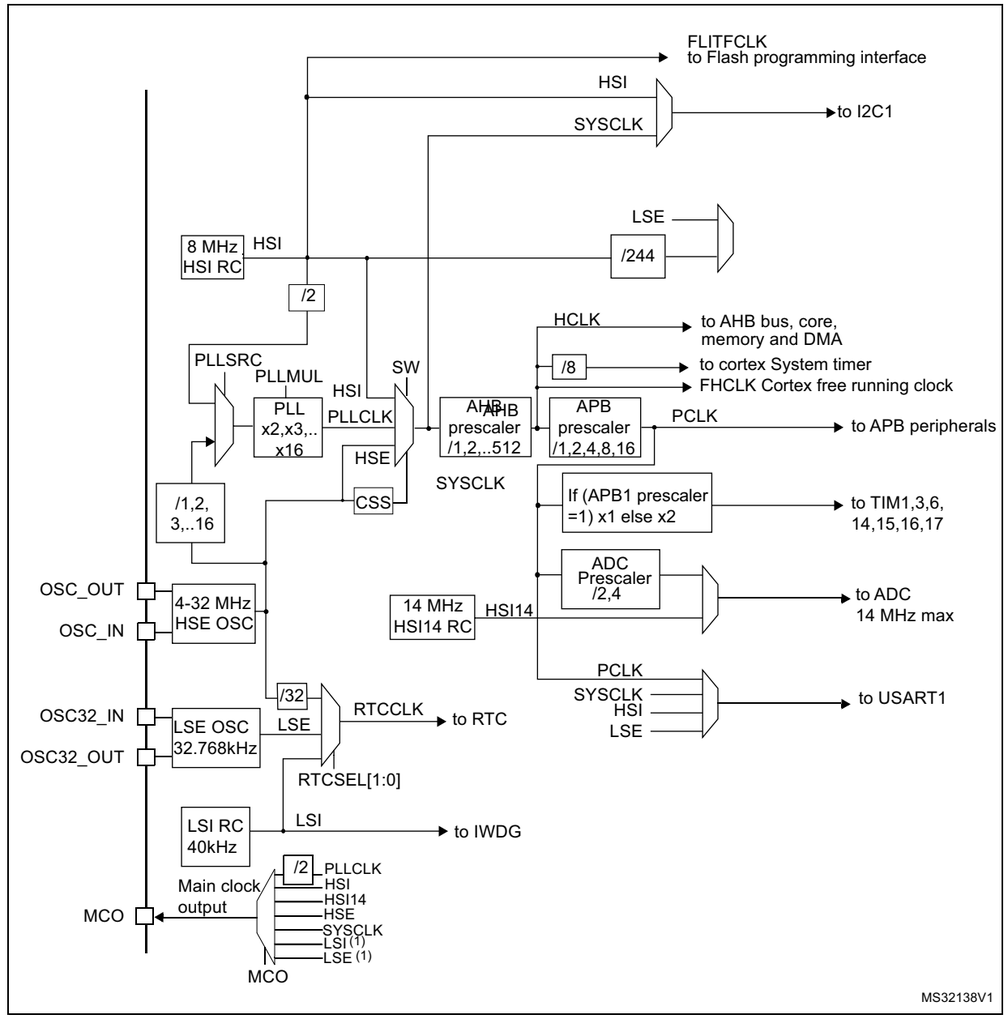
多个预分频器允许应用程序配置 AHB 和 APB 域的频率。 AHB 和 APB 域的最大频率为 48 MHz。

Figure 2. Clock tree



1. LSI/LSE is not available on STM32F030x8 devices.

图 2. 时钟树



1. LSI/LSE 在 STM32F030x8 器件上不可用。

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2C, USART, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

3.7 General-purpose inputs/outputs (GPIOs)

每个 GPIO 引脚均可通过软件配置为输出（推挽或开漏）、输入（带或不带上拉或下拉）或外设备用功能。大多数 GPIO 引脚与数字或模拟备用功能共享。

如果需要，可以按照特定顺序锁定 I/O 配置，以避免对 I/O 寄存器进行虚假写入。

3.8 直接内存访问控制器（ DMA ）

5 通道通用 DMA 管理内存到内存、外设到内存以及内存到外设的传输。

DMA 支持循环缓冲区管理，当控制器到达缓冲区末尾时无需用户代码干预。

每个通道都连接到专用硬件 DMA 请求，并支持每个通道上的软件触发。配置由软件进行，源和目标之间的传输大小是独立的。

DMA 可与主要外设一起使用：SPI 、 I2C 、 USART 、所有 TIMx 定时器（ TIM14 除外）和 ADC。

3.9 中断和事件

3.9.1 嵌套向量中断控制器 (NVIC)

STM32F0xx 系列嵌入了一个嵌套向量中断控制器，能够处理多达 32 个可屏蔽中断通道（不包括 Cortex™-M0 的 16 个中断线）和 4 个优先级。

• 紧密耦合的 NVIC 提供低延迟中断处理 • 直接传递到内核的中断入口向量表地址 • 紧密耦合的 NVIC 内核接口 • 允许提前处理中断 • 处理迟到的较高优先级中断 • 支持尾链 • 处理器状态自动保存 • 中断退出时恢复中断入口，无指令开销

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 扩展中断 / 事件控制器（ EXTI ）

扩展中断 / 事件控制器由 24 个边沿检测器线组成，用于生成中断 / 事件请求并唤醒系统。每条线都可以独立配置以选择触发事件（上升沿、下降沿、两者），并且可以独立屏蔽。挂起寄存器维护中断请求的状态。 EXTI 可以检测脉冲宽度短于内部时钟周期的外部线路。最多 55 个 GPIO 可以连接到 16 条外部中断线。

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 2 internal (temperature sensor/voltage reference measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

3.10 模数转换器（ADC）

12 位模数转换器具有多达 16 个外部通道和 2 个内部通道（温度传感器 / 电压参考测量），并以单次或扫描模式执行转换。在扫描模式下，对选定的一组模拟输入执行自动转换。

ADC 可由 DMA 控制器提供服务。

模拟看门狗功能可以非常精确地监控一个、部分或所有选定通道的转换电压。当转换电压超出编程阈值时，会生成中断。

3.10.1 温度传感器

温度传感器 (TS) 生成随温度线性变化的电压 VSENSE。

温度传感器内部连接至 ADC_IN16 输入通道，用于将传感器输出电压转换为数字值。

该传感器提供良好的线性度，但必须对其进行校准才能获得良好的温度测量整体精度。由于工艺变化导致温度传感器的偏移因芯片而异，因此未校准的内部温度传感器适用于仅检测温度变化的应用。

为了提高温度传感器测量的准确性，每个设备均由 ST 单独进行工厂校准。温度传感器工厂校准数据由 ST 存储在系统存储区域中，可以只读模式访问。

表 3. 温度传感器校准值

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 内部参考电压（VREFINT）

内部参考电压 (VREFINT) 为 ADC 提供稳定（带隙）电压输出。 VREFINT 在内部连接到 ADC_IN17 输入通道。 ST 在生产测试期间对每个部件单独测量 VREFINT 的精确电压，并将其存储在系统存储区域中。它可以在只读模式下访问。

表 4. 内部参考电压校准值

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

3.11 Timers and watchdogs

Devices of the STM32F0xx family include up to six general-purpose timers, one basic timer and an advanced control timer.

Table 5 compares the features of the advanced-control, general-purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM15(1)	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
Basic	TIM6(1)	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

1. Available on STM32F030x8 devices only.

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.11 定时器和看门狗

STM32F0xx 系列器件包括多达 6 个通用定时器、 1 个基本定时器和 1 个高级控制定时器。

*Tab*le 5 比较高级控制定时器、通用定时器和基本定时器的特性 .

表 5. 定时器功能比较

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM15(1)	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
Basic	TIM6(1)	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

1. Available on STM32F030x8 devices only.

3.11.1 高级控制定时器（ TIM1 ）

高级控制定时器 (TIM1) 可以看作是 6 个通道上多路复用的三相 PWM。它具有互补 PWM 输出和可编程插入死区时间。它也可以看作是一个完整的通用定时器。 4 个独立通道可用于:

- 输入捕捉
- 输出比较
- PWM 生成（边沿或中心对齐模式）
- 单脉冲模式输出

如果配置为标准 16 位定时器，它具有与 TIMx 定时器相同的功能。如果配置为 16 位 PWM 发生器，则具有完整的调制能力 (0-100%)。

计数器可以在调试模式下冻结。

许多功能与具有相同架构的标准定时器共享。因此，高级控制定时器可以通过定时器链接功能与其他定时器一起工作，以实现同步或事件链接。

3.11.2 General-purpose timers (TIM3, TIM14..17)

There are five synchronizable general-purpose timers embedded in the STM32F030x devices (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM3

STM32F030x devices feature a synchronizable 4-channel general-purpose timer based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 features 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM3 general-purpose timer can work with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

It provides independent DMA request generation.

The TIM3 timer is capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Its counter can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.11.3 Basic timer TIM6

This timer is mainly used as a generic 16-bit time base.

3.11.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free

3.11.2 通用定时器（TIM3 、 TIM14..17 ）

STM32F030x 器件中嵌入了五个可同步的通用定时器（差异见表 5 ）。每个通用定时器均可用于生成 PWM 输出，或作为简单的时基。

TIM3

STM32F030x 器件具有基于 16 位自动重载向上 / 向下计数器和 16 位预分频器的可同步 4 通道通用定时器。 TIM3 具有 4 个独立通道，用于输入捕捉 / 输出比较、 PWM 或单脉冲模式输出。这在最大的封装上提供了多达 12 个输入捕获 / 输出比较 /PWM。

TIM3 通用定时器可通过定时器链接功能与 TIM1 高级控制定时器配合使用，以实现同步或事件链接。

它提供独立的 DMA 请求生成。

TIM3 定时器能够处理正交（增量）编码器信号和 1 至 3 个霍尔效应传感器的数字输出。

其计数器可以在调试模式下冻结。

TIM14

该定时器基于 16 位自动重载向上计数器和 16 位预分频器。

TIM14 具有一个用于输入捕捉 / 输出比较、 PWM 或单脉冲模式输出的单通道。

其计数器可以在调试模式下冻结。

TIM15 、 TIM16 和 TIM17

这些定时器基于 16 位自动重载向上计数器和 16 位预分频器。

TIM15 具有两个独立通道，而 TIM16 和 TIM17 则具有一个用于输入捕获 / 输出比较、 PWM 或单脉冲模式输出的单通道。

TIM15 、 TIM16 和 TIM17 定时器可以一起工作，TIM15 还可以通过定时器链接功能与 TIM1 一起操作，以实现同步或事件链接。

TIM15 可以与 TIM16 和 TIM17 同步。

TIM15 、 TIM16 和 TIM17 具有互补输出，具有死区时间生成和独立 DMA 请求生成功能。

它们的计数器可以在调试模式下冻结。

3.11.3 基本定时器 TIM6

该定时器主要用作通用 16 位时基。

3.11.4 Independent watchdog (IWDG)

独立看门狗基于 8 位预分频器和 12 位递减计数器，并具有用户定义的刷新窗口。它由独立的 40 kHz 内部 RC 提供时钟，并且由于它独立于主时钟运行，因此它可以在停止和待机模式下运行。它可以用作看门狗，在出现问题时重置设备，也可以用作免费的

running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.11.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.11.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC)

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Programmable alarm with wake up from Stop and Standby mode capability
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Periodic wakeup from Stop/Standby
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

运行应用程序超时管理的计时器。它可以通过选项字节进行硬件或软件配置。计数器可以在调试模式下冻结。

3.11.5 System window watchdog (WWDG)

系统窗口看门狗基于可设置为自由运行的 7 位递减计数器。它可以用作看门狗，在出现问题时重置设备。它由 APB 时钟 (PCLK) 提供时钟。它具有预警中断能力，并且计数器可以在调试模式下冻结。

3.11.6 SysTick 定时器

该定时器专用于实时操作系统，但也可以用作标准递减计数器。其特点：

- 24 位递减计数器 • 自动重载功能 • 计数器达到 0 时生成可屏蔽系统中断 • 可编程时钟源（ HCLK 或 HCLK/8 ）

3.12 实时时钟（ RTC ）

RTC 是一个独立的 BCD 定时器 / 计数器。其主要特点如下：

- 带有亚秒、秒、分钟、小时（ 12 或 24 格式）、星期、日期、月份、年的日历，采用 BCD （二进制编码的十进制）格式 • 自动校正每月的 28 、 29 （闰年）、 30 和 31 天
- 可编程闹钟，可从停止和待机模式唤醒功能 • 从 1 到 32767 个 RTC 时钟脉冲进行动态校正。这可用于将其与主时钟同步。 • 分辨率为 1 ppm 的数字校准电路，以补偿石英晶体的不准确性 • 2 具有可编程滤波器的防篡改检测引脚。当检测到篡改事件时，可以将 MCU 从停止和待机模式中唤醒。 • 时间戳功能，可用于保存日历内容。该函数可以由时间戳引脚上的事件或篡改事件触发。 MCU 可以在时间戳事件检测时从停止和待机模式中唤醒。 • 从停止 / 待机中定期唤醒 • 参考时钟检测：可以使用更精确的第二源时钟（ 50 或 60 Hz ）来提高日历精度。

RTC 时钟源可以是：

- 32.768kHz 外部晶振 • 谐振器或振荡器 • 内部低功耗 RC 振荡器（典型频率为 40kHz ） • 高速外部时钟 32 分频

3.13 Inter-integrated circuit interfaces (I^2C)

Up to two I^2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) or Fast mode (up to 400 kbit/s). I2C1 also supports Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F030x I^2C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	-
SMBus	X	-

1. X = supported.

3.13 集成电路间接口（I^2C）

最多两个 I^2C 接口（I2C1 和 I2C2）可以在多主模式或从模式下运行。两者均可支持标准模式（高达 100 kbit/s）或快速模式（高达 400 kbit/s）。I2C1 还支持具有 20 mA 输出驱动的快速模式 Plus（高达 1 Mbit/s）。

两者都支持 7 位和 10 位寻址模式，多个 7 位从机地址（2 个地址，1 个带可配置掩码）。它们还包括可编程模拟和数字噪声滤波器。

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

此外，I2C1 还为 SMBUS 2.0 和 PMBUS 1.1 提供硬件支持：ARP 功能、主机通知协议、硬件 CRC (PEC) 生成 / 验证、超时验证和 ALERT 协议管理。

I2C 接口可由 DMA 控制器提供服务。

I2C1 和 I2C2 之间的差异请参见表 7。

表 7. STM32F030x I^2C 实现

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	-
SMBus	X	-

1. X = supported.

3.14 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds up to two universal synchronous/asynchronous receiver transmitters (USART1 and USART2), which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS and RTS signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. The USART1 supports also auto baud rate feature.

The USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the differences between USART1 and USART2.

Table 8. STM32F030x USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Single-wire half-duplex communication	X	X
Receiver timeout interrupt	X	-
Auto baud rate detection	X	-

1. X = supported.

3.15 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Refer to *Table 9* for the differences between SPI1 and SPI2.

Table 9. STM32F030x SPI implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
TI mode	X	X

1. X = supported.

3.16 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

3.14 通用同步 / 异步接收发送器（ USART ）

该器件嵌入最多两个通用同步 / 异步接收发送器（ USART1 和 USART2 ），其通信速度高达 6 Mbit/s。

它们提供 CTS 和 RTS 信号的硬件管理、多处理器通信模式、主同步通信和单线半双工通信模式。 USART1 还支持自动波特率功能。

The USART interfaces can be served by the DMA controller.

USART1 和 USART2 之间的差异请参见表 8。

Table 8. STM32F030x USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Single-wire half-duplex communication	X	X
Receiver timeout interrupt	X	-
Auto baud rate detection	X	-

1. X = supported.

3.15 串行外设接口（ SPI ）

在全双工和半双工通信模式下，最多两个 SPI 在从模式和主模式下能够以高达 18 Mbits/s 的速度进行通信。 3 位预分频器提供 8 个主模式频率，帧大小可从 4 位配置到 16 位。

SPI1 和 SPI2 之间的差异请参见表 9。

表 9. STM32F030x SPI 实现

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
TI mode	X	X

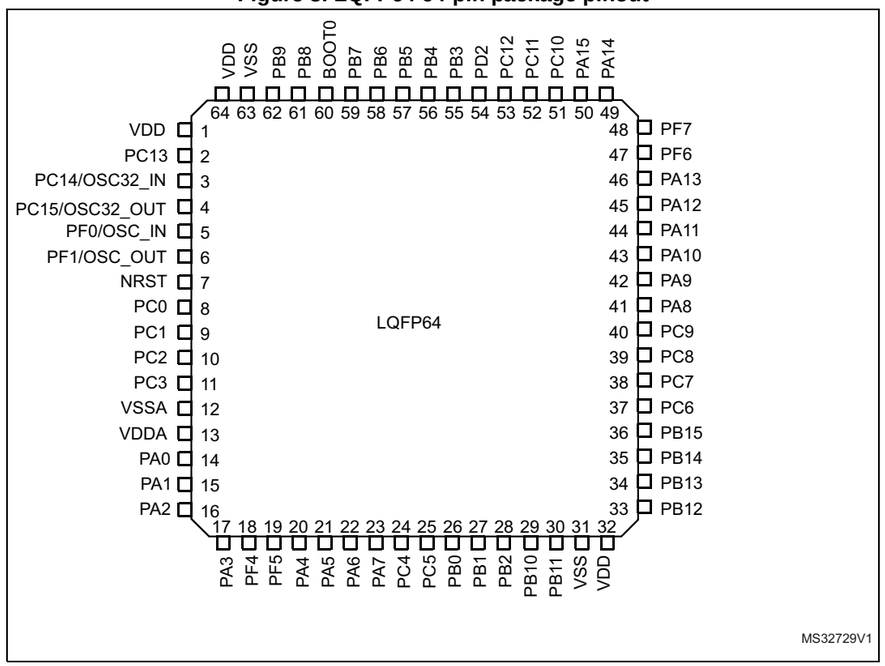
1. X = supported.

3.16 串行线调试端口（ SW-DP ）

提供 ARM SW-DP 接口以允许将串行线调试工具连接到 MCU。

4 Pinouts and pin descriptions

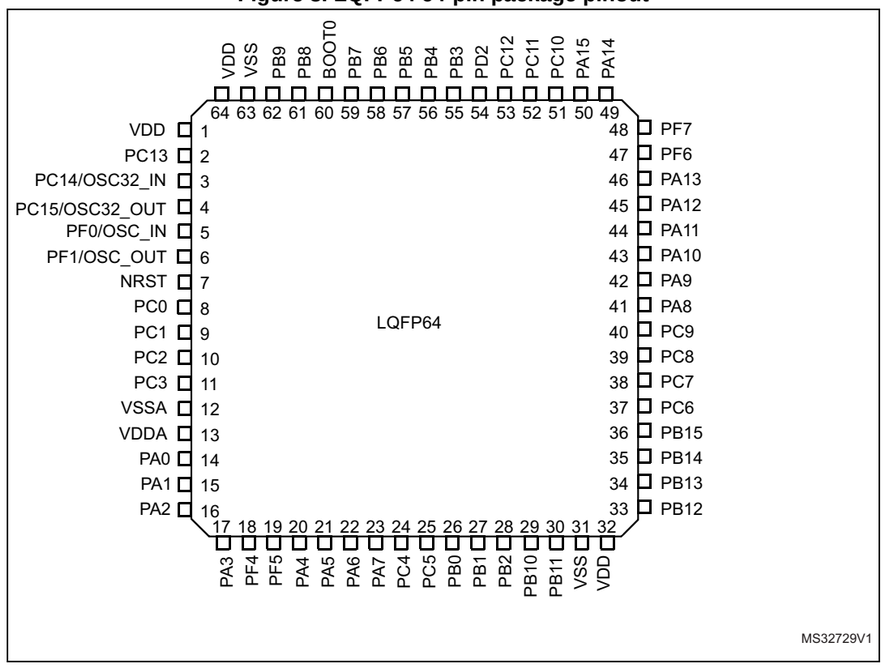
Figure 3. LQFP64 64-pin package pinout



1. The above figure shows the package top view.

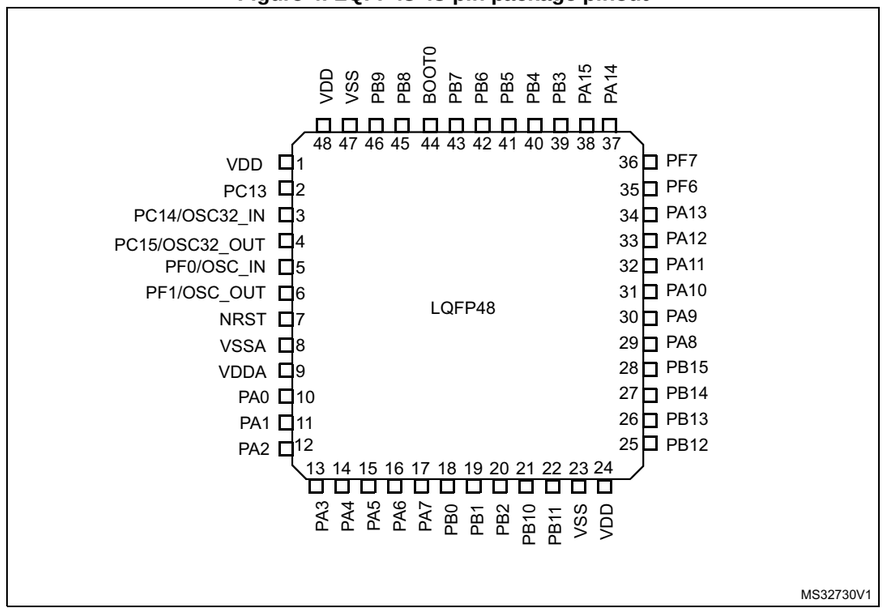
4 引脚排列和引脚描述

Figure 3. LQFP64 64-pin package pinout



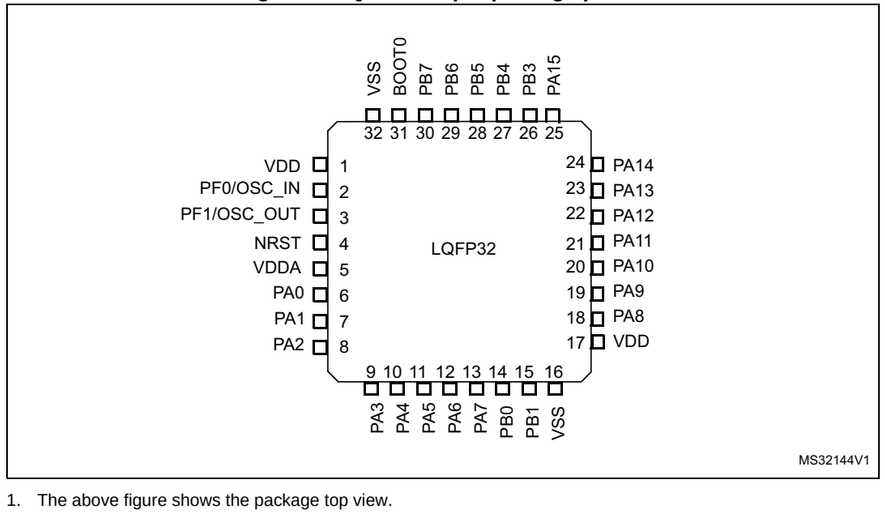
1. 上图为封装俯视图。

Figure 4. LQFP48 48-pin package pinout



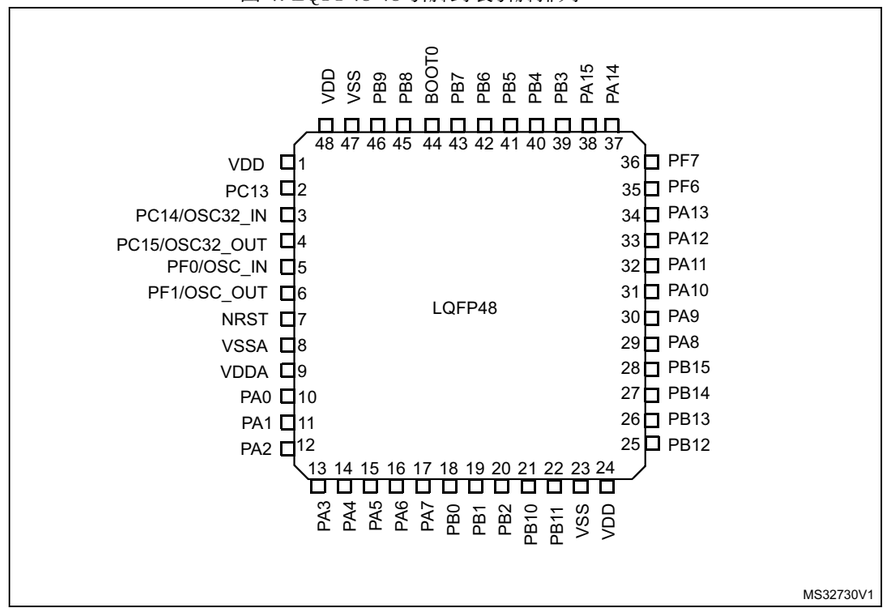
1. The above figure shows the package top view.

Figure 5. LQFP32 32-pin package pinout



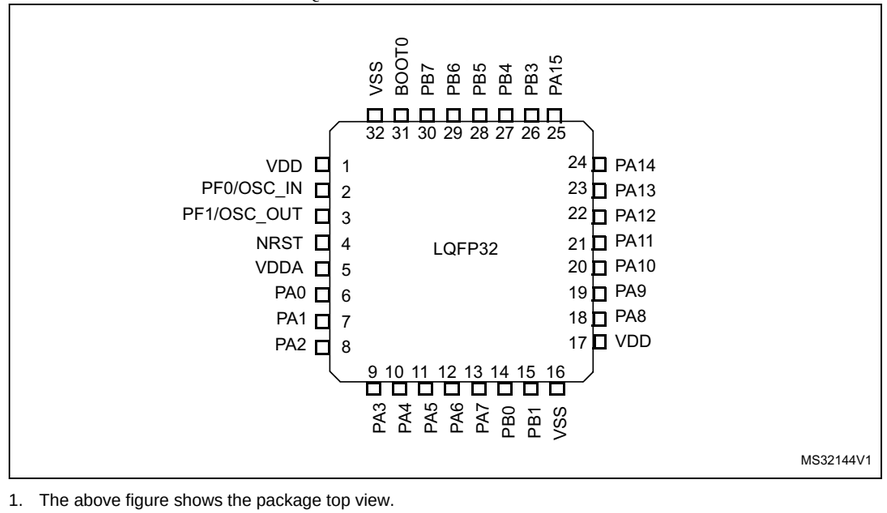
1. The above figure shows the package top view.

图 4. LQFP48 48 引脚封装引脚排列



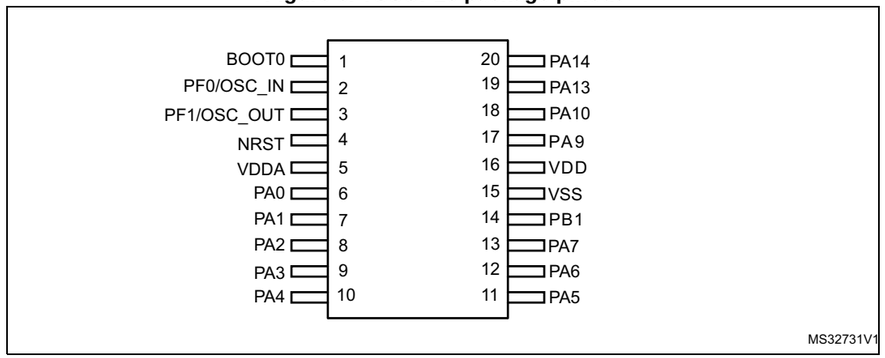
1. The above figure shows the package top view.

图 5. LQFP32 32 引脚封装引脚排列



1. The above figure shows the package top view.

Figure 6. TSSOP20 package pinout

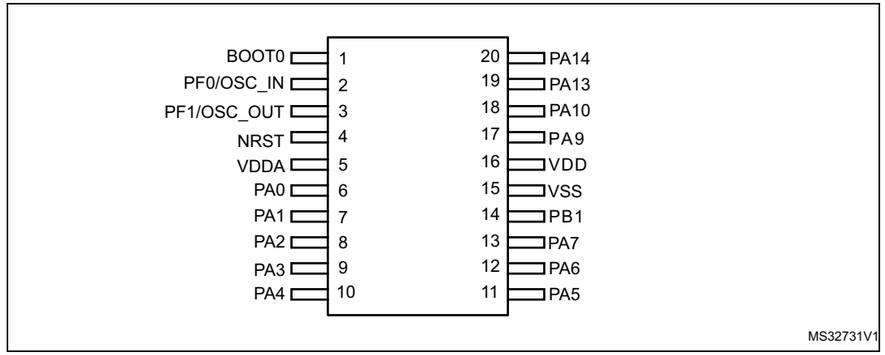


1. The above figure shows the package top view.

Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

图 6. TSSOP20 封装引脚排列



1. 上图为封装俯视图。

表 10. 引脚分配表中使用的图例 / 缩写

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. Pin definitions

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
1	1	-	-	VDD	S			Complementary power supply	
2	2	-	-	PC13	I/O	TC	(1)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	3	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)	-	OSC32_IN
4	4	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)	-	OSC32_OUT
5	5	2	2	PF0-OSC_IN (PF0)	I/O	FT		-	OSC_IN
6	6	3	3	PF1-OSC_OUT (PF1)	I/O	FT		-	OSC_OUT
7	7	4	4	NRST	I/O	RST		Device reset input / internal reset output (active low)	
8	-	-	-	PC0	I/O	TTa		EVENTOUT	ADC_IN10
9	-	-	-	PC1	I/O	TTa		EVENTOUT	ADC_IN11
10	-	-	-	PC2	I/O	TTa		EVENTOUT	ADC_IN12
11	-	-	-	PC3	I/O	TTa		EVENTOUT	ADC_IN13
12	8	-	-	VSSA	S			Analog ground	
13	9	5	5	VDDA	S			Analog power supply	
14	10	6	6	PA0	I/O	TTa		USART1_CTS(2), USART2_CTS(3)	ADC_IN0, RTC_TAMP2, WKUP1
15	11	7	7	PA1	I/O	TTa		USART1_RTS(2), USART2_RTS(3), EVENTOUT	ADC_IN1
16	12	8	8	PA2	I/O	TTa		USART1_TX(2), USART2_TX(3), TIM15_CH1(3)	ADC_IN2
17	13	9	9	PA3	I/O	TTa		USART1_RX(2), USART2_RX(3), TIM15_CH2(3)	ADC_IN3
18	-	-	-	PF4	I/O	FT		EVENTOUT	-
19	-	-	-	PF5	I/O	FT		EVENTOUT	-

表 11. 引脚定义

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
1	1	-	-	VDD	S			Complementary power supply	
2	2	-	-	PC13	I/O	TC	(1)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	3	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)	-	OSC32_IN
4	4	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)	-	OSC32_OUT
5	5	2	2	PF0-OSC_IN (PF0)	I/O	FT		-	OSC_IN
6	6	3	3	PF1-OSC_OUT (PF1)	I/O	FT		-	OSC_OUT
7	7	4	4	NRST	I/O	RST		Device reset input / internal reset output (active low)	
8	-	-	-	PC0	I/O	TTa		EVENTOUT	ADC_IN10
9	-	-	-	PC1	I/O	TTa		EVENTOUT	ADC_IN11
10	-	-	-	PC2	I/O	TTa		EVENTOUT	ADC_IN12
11	-	-	-	PC3	I/O	TTa		EVENTOUT	ADC_IN13
12	8	-	-	VSSA	S			Analog ground	
13	9	5	5	VDDA	S			Analog power supply	
14	10	6	6	PA0	I/O	TTa		USART1_CTS(2), USART2_CTS(3)	ADC_IN0, RTC_TAMP2, WKUP1
15	11	7	7	PA1	I/O	TTa		USART1_RTS(2), USART2_RTS(3), EVENTOUT	ADC_IN1
16	12	8	8	PA2	I/O	TTa		USART1_TX(2), USART2_TX(3), TIM15_CH1(3)	ADC_IN2
17	13	9	9	PA3	I/O	TTa		USART1_RX(2), USART2_RX(3), TIM15_CH2(3)	ADC_IN3
18	-	-	-	PF4	I/O	FT		EVENTOUT	-
19	-	-	-	PF5	I/O	FT		EVENTOUT	-

Table 11. Pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
20	14	10	10	PA4	I/O	TTa		SPI1_NSS, USART1_CK(2) USART2_CK(3), TIM14_CH1	ADC_IN4
21	15	11	11	PA5	I/O	TTa		SPI1_SCK	ADC_IN5
22	16	12	12	PA6	I/O	TTa		SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6
23	17	13	13	PA7	I/O	TTa		SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
24	-	-	-	PC4	I/O	TTa		EVENTOUT	ADC_IN14
25	-	-	-	PC5	I/O	TTa		-	ADC_IN15
26	18	14	-	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, EVENTOUT	ADC_IN8
27	19	15	14	PB1	I/O	TTa		TIM3_CH4, TIM14_CH1, TIM1_CH3N	ADC_IN9
28	20	-	-	PB2	I/O	FT	(4)	-	-
29	21	-	-	PB10	I/O	FT		I2C1_SCL(2), I2C2_SCL(3)	-
30	22	-	-	PB11	I/O	FT		I2C1_SDA(2), I2C2_SDA(3), EVENTOUT	-
31	23	16	-	VSS	S			Ground	
32	24	17	16	VDD	S			Digital power supply	
33	25	-	-	PB12	I/O	FT		SPI1_NSS(2), SPI2_NSS(3), TIM1_BKIN, EVENTOUT	-

表 11. 引脚定义（续）

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
20	14	10	10	PA4	I/O	TTa		SPI1_NSS, USART1_CK(2) USART2_CK(3), TIM14_CH1	ADC_IN4
21	15	11	11	PA5	I/O	TTa		SPI1_SCK	ADC_IN5
22	16	12	12	PA6	I/O	TTa		SPI1_MISO, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6
23	17	13	13	PA7	I/O	TTa		SPI1_MOSI, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
24	-	-	-	PC4	I/O	TTa		EVENTOUT	ADC_IN14
25	-	-	-	PC5	I/O	TTa		-	ADC_IN15
26	18	14	-	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, EVENTOUT	ADC_IN8
27	19	15	14	PB1	I/O	TTa		TIM3_CH4, TIM14_CH1, TIM1_CH3N	ADC_IN9
28	20	-	-	PB2	I/O	FT	(4)	-	-
29	21	-	-	PB10	I/O	FT		I2C1_SCL(2), I2C2_SCL(3)	-
30	22	-	-	PB11	I/O	FT		I2C1_SDA(2), I2C2_SDA(3), EVENTOUT	-
31	23	16	-	VSS	S			Ground	
32	24	17	16	VDD	S			Digital power supply	
33	25	-	-	PB12	I/O	FT		SPI1_NSS(2), SPI2_NSS(3), TIM1_BKIN, EVENTOUT	-

Table 11. Pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
34	26	-	-	PB13	I/O	FT		SPI1_SCK(2), SPI2_SCK(3), TIM1_CH1N	-
35	27	-	-	PB14	I/O	FT		SPI1_MISO(2), SPI2_MISO(3), TIM1_CH2N, TIM15_CH1(3)	-
36	28	-	-	PB15	I/O	FT		SPI1_MOSI(2), SPI2_MOSI(3), TIM1_CH3N, TIM15_CH1N(3), TIM15_CH2(3)	RTC_REFIN
37	-	-	-	PC6	I/O	FT		TIM3_CH1	-
38	-	-	-	PC7	I/O	FT		TIM3_CH2	-
39	-	-	-	PC8	I/O	FT		TIM3_CH3	-
40	-	-	-	PC9	I/O	FT		TIM3_CH4	-
41	29	18	-	PA8	I/O	FT		USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	30	19	17	PA9	I/O	FT		USART1_TX, TIM1_CH2, TIM15_BKIN(3) I2C1_SCL(2)	-
43	31	20	18	PA10	I/O	FT		USART1_RX, TIM1_CH3, TIM17_BKIN I2C1_SDA(2)	-
44	32	21	-	PA11	I/O	FT		USART1_CTS, TIM1_CH4, EVENTOUT	-
45	33	22	-	PA12	I/O	FT		USART1_RTS, TIM1_ETR, EVENTOUT	-
46	34	23	19	PA13 (SWDIO)	I/O	FT	(5)	IR_OUT, SWDIO	-
47	35	-	-	PF6	I/O	FT		I2C1_SCL(2), I2C2_SCL(3)	-

表 11. 引脚定义（续）

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
34	26	-	-	PB13	I/O	FT		SPI1_SCK(2), SPI2_SCK(3), TIM1_CH1N	-
35	27	-	-	PB14	I/O	FT		SPI1_MISO(2), SPI2_MISO(3), TIM1_CH2N, TIM15_CH1(3)	-
36	28	-	-	PB15	I/O	FT		SPI1_MOSI(2), SPI2_MOSI(3), TIM1_CH3N, TIM15_CH1N(3), TIM15_CH2(3)	RTC_REFIN
37	-	-	-	PC6	I/O	FT		TIM3_CH1	-
38	-	-	-	PC7	I/O	FT		TIM3_CH2	-
39	-	-	-	PC8	I/O	FT		TIM3_CH3	-
40	-	-	-	PC9	I/O	FT		TIM3_CH4	-
41	29	18	-	PA8	I/O	FT		USART1_CK, TIM1_CH1, EVENTOUT, MCO	-
42	30	19	17	PA9	I/O	FT		USART1_TX, TIM1_CH2, TIM15_BKIN(3) I2C1_SCL(2)	-
43	31	20	18	PA10	I/O	FT		USART1_RX, TIM1_CH3, TIM17_BKIN I2C1_SDA(2)	-
44	32	21	-	PA11	I/O	FT		USART1_CTS, TIM1_CH4, EVENTOUT	-
45	33	22	-	PA12	I/O	FT		USART1_RTS, TIM1_ETR, EVENTOUT	-
46	34	23	19	PA13 (SWDIO)	I/O	FT	(5)	IR_OUT, SWDIO	-
47	35	-	-	PF6	I/O	FT		I2C1_SCL(2), I2C2_SCL(3)	-

Table 11. Pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
48	36	-	-	PF7	I/O	FT		I2C1_SDA(2), I2C2_SDA(3)	-
49	37	24	20	PA14 (SWCLK)	I/O	FT	(5)	USART1_TX(2), USART2_TX(3), SWCLK	-
50	38	25	-	PA15	I/O	FT		SPI1_NSS, USART1_RX(2), USART2_RX(3), EVENTOUT	-
51	-	-	-	PC10	I/O	FT		-	-
52	-	-	-	PC11	I/O	FT		-	-
53	-	-	-	PC12	I/O	FT		-	-
54	-	-	-	PD2	I/O	FT		TIM3_ETR	-
55	39	26	-	PB3	I/O	FT		SPI1_SCK, EVENTOUT	-
56	40	27	-	PB4	I/O	FT		SPI1_MISO, TIM3_CH1, EVENTOUT	-
57	41	28	-	PB5	I/O	FT		SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
58	42	29	-	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N	-
59	43	30	-	PB7	I/O	FTf		I2C1_SDA, USART1_RX, TIM17_CH1N	-
60	44	31	1	BOOT0	I	B		Boot memory selection	
61	45	-	-	PB8	I/O	FTf	(5)	I2C1_SCL, TIM16_CH1	-
62	46	-	-	PB9	I/O	FTf		I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-

表 11. 引脚定义（续）

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
48	36	-	-	PF7	I/O	FT		I2C1_SDA(2), I2C2_SDA(3)	-
49	37	24	20	PA14 (SWCLK)	I/O	FT	(5)	USART1_TX(2), USART2_TX(3), SWCLK	-
50	38	25	-	PA15	I/O	FT		SPI1_NSS, USART1_RX(2), USART2_RX(3), EVENTOUT	-
51	-	-	-	PC10	I/O	FT		-	-
52	-	-	-	PC11	I/O	FT		-	-
53	-	-	-	PC12	I/O	FT		-	-
54	-	-	-	PD2	I/O	FT		TIM3_ETR	-
55	39	26	-	PB3	I/O	FT		SPI1_SCK, EVENTOUT	-
56	40	27	-	PB4	I/O	FT		SPI1_MISO, TIM3_CH1, EVENTOUT	-
57	41	28	-	PB5	I/O	FT		SPI1_MOSI, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
58	42	29	-	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N	-
59	43	30	-	PB7	I/O	FTf		I2C1_SDA, USART1_RX, TIM17_CH1N	-
60	44	31	1	BOOT0	I	B		Boot memory selection	
61	45	-	-	PB8	I/O	FTf	(5)	I2C1_SCL, TIM16_CH1	-
62	46	-	-	PB9	I/O	FTf		I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-

Table 11. Pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
63	47	32	15	VSS	S			Ground	
64	48	1	16	VDD	S			Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. This feature is available on STM32F030x6 and STM32F030x4 devices only.
3. This feature is available on STM32F030x8 devices only.
4. On LQFP32 package, PB2 and PB8 should be treated as unconnected pins (even when they are not available on the package, they are not forced to a defined level by hardware).
5. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on SWDIO pin and internal pull-down on SWCLK pin are activated.

表 11. 引脚定义（续）

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	LQFP32	TSSOP20					Alternate functions	Additional functions
63	47	32	15	VSS	S			Ground	
64	48	1	16	VDD	S			Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. This feature is available on STM32F030x6 and STM32F030x4 devices only.
3. This feature is available on STM32F030x8 devices only.
4. On LQFP32 package, PB2 and PB8 should be treated as unconnected pins (even when they are not available on the package, they are not forced to a defined level by hardware).
5. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on SWDIO pin and internal pull-down on SWCLK pin are activated.

Table 12. Alternate functions selected through GPIOA_AFR registers for port A

AF0	AF1	AF2	AF3	AF4	AF5	AF6
-	USART1_CTS(1)	-	-	-	-	-
	USART2_CTS(2)					
EVENTOUT	USART1_RTS(1)	-	-	-	-	-
	USART2_RTS(2)					
TIM15_CH1(2)	USART1_TX(1)	-	-	-	-	-
	USART2_TX(2)					
TIM15_CH2(2)	USART1_RX(1)	-	-	-	-	-
	USART2_RX(2)					
SPI1_NSS	USART1_CK(1)	-	-	TIM14_CH1	-	-
	USART2_CK(2)					
SPI1_SCK	-	-	-	-	-	-
SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	EVENTOUT
SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT
MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-
TIM15_BKIN(2)	USART1_TX	TIM1_CH2	-	I2C1_SCL(1)	-	-
TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA(1)	-	-
EVENTOUT	USART1_CTS	TIM1_CH4	-	-	-	-
EVENTOUT	USART1_RTS	TIM1_ETR	-	-	-	-
SWDIO	IR_OUT	-	-	-	-	-
SWCLK	USART1_TX(1)	-	-	-	-	-
	USART2_TX(2)					
SPI1_NSS	USART1_RX(1)	-	EVENTOUT	-	-	-
	USART2_RX(2)					

1. available on STM32F030x6 and STM32F030x4 devices only.
2. available on STM32F030x8 devices only.

表 12. 通过端口 A 的 GPIOA_AFR 寄存器选择的备用功能

Pin name	AF0	AF1	AF2	AF3	AF4
PA0	-	USART1_CTS(1) USART2_CTS(2) USART1_RTS(1)	-	-	-
PA1	EVENTOUT	USART2_RTS(2)	-	-	-
PA2	TIM15_CH1(2)	USART1_TX(1) USART2_TX(2)	-	-	-
PA3	TIM15_CH2(2)	USART1_RX(1) USART2_RX(2)	-	-	-
PA4	SPI1_NSS	USART1_CK(1) USART2_CK(2)	-	-	TIM14_CH1
PA5	SPI1_SCK	-	-	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-
PA9	TIM15_BKIN(2)	USART1_TX	TIM1_CH2	-	I2C1_SCL(1)
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA(1)

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Table 13. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-
PB2	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	-	-
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT	-
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-
PB8	-	I2C1_SCL	TIM16_CH1	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	-	I2C1_SCL(1) I2C2_SCL(2)	-	-
PB11	EVENTOUT	I2C1_SDA(1) I2C2_SDA(2)	-	-
PB12	SPI1_NSS(1) SPI2_NSS(2)	EVENTOUT	TIM1_BKIN	-
PB13	SPI1_SCK(1) SPI2_SCK(2)	-	TIM1_CH1N	-
PB14	SPI1_MISO(1) SPI2_MISO(2)	TIM15_CH1(2)	TIM1_CH2N	-
PB15	SPI1_MOSI(1) SPI2_MOSI(2)	TIM15_CH2(2)	TIM1_CH3N	TIM15_CH1N(2)

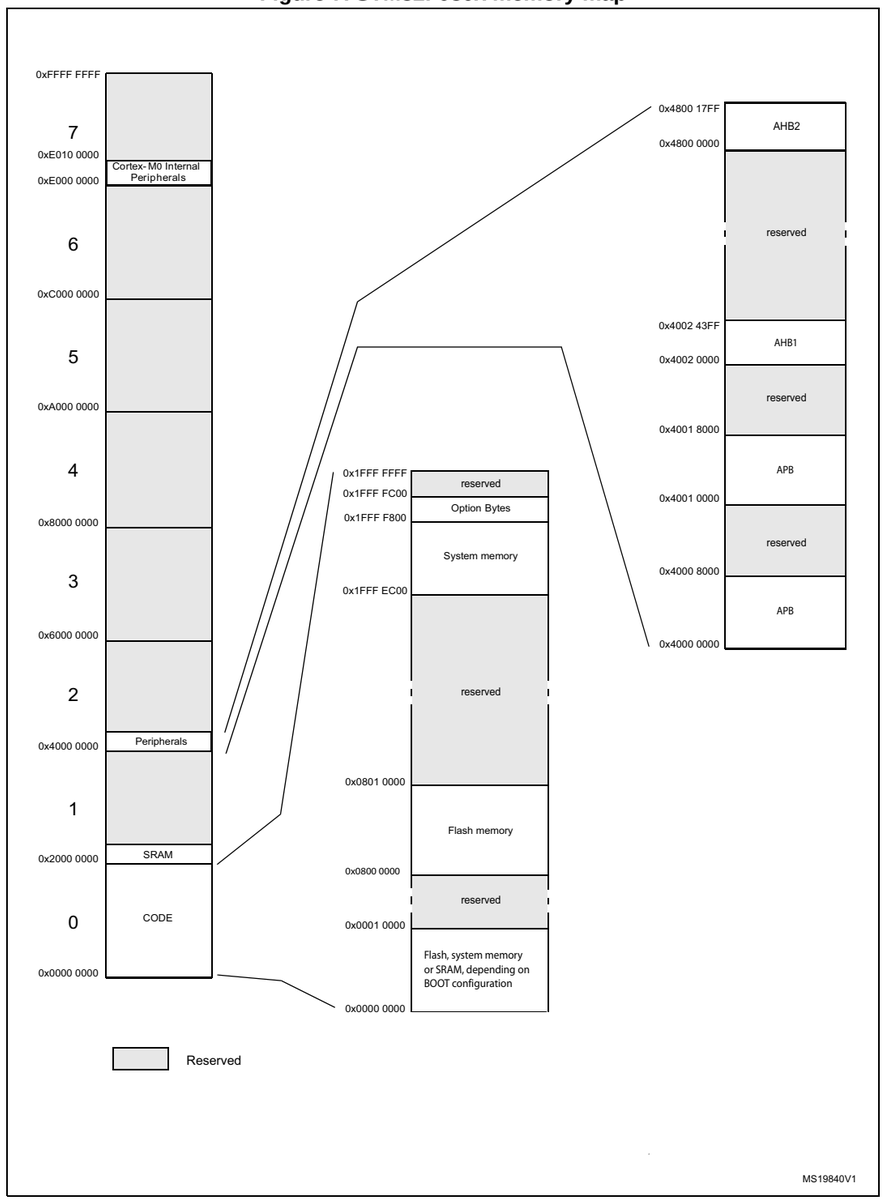
1. available on STM32F030x6 and STM32F030x4 devices only.
2. available on STM32F030x8 devices only.

表 13. 通过端口 B 的 GPIOB_AFR 寄存器选择的备用功能

Pin name	AF0	AF1	AF2
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N
PB2	-	-	-
PB3	SPI1_SCK	EVENTOUT	-
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N
PB8	-	I2C1_SCL	TIM16_CH1
PB9	IR_OUT	I2C1_SDA	TIM17_CH1
PB10	-	I2C1_SCL(1) I2C2_SCL(2)	-
PB11	EVENTOUT	I2C1_SDA(1) I2C2_SDA(2)	-
PB12	SPI1_NSS(1) SPI2_NSS(2)	EVENTOUT	TIM1_BKIN

5 Memory mapping

Figure 7. STM32F030x memory map



5 内存映射

图 7. STM32F030x 存储器映射

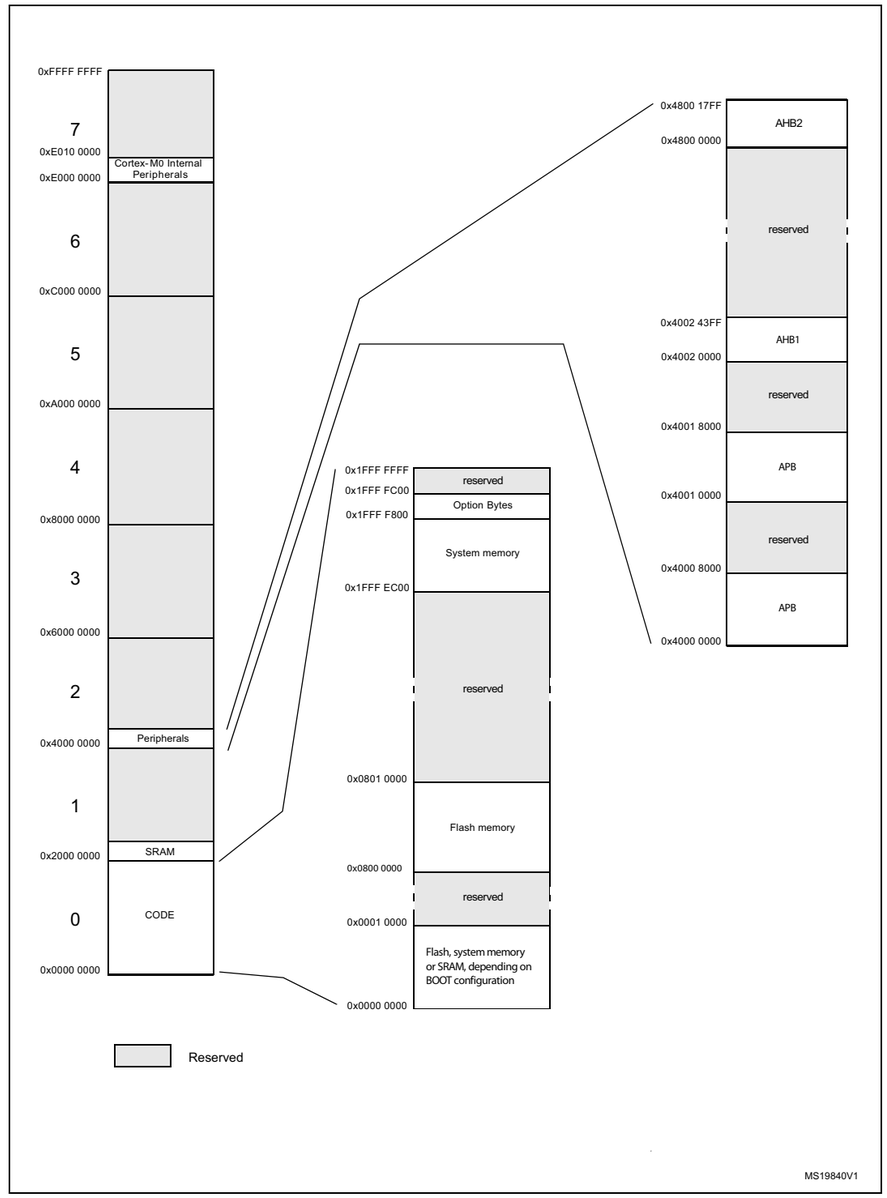


Table 14. STM32F030x peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 43FF	4 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15(1)
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

表 14. STM32F030x 外设寄存器边界地址

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1 KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 43FF	4 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15(1)
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 14. STM32F030x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7400 - 0x4000 7FFF	3 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 5C00 - 0x4000 6FFF	5 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2(1)
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	USART2(1)
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2(1)
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1400 - 0x4000 1FFF	3 KB	Reserved
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6(1)
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	Reserved

1. This feature is available on STM32F030x8 devices only. For STM32F030x6 and STM32F060x4, the area is Reserved.

表 14. STM32F030x 外设寄存器边界地址（续）

Bus	Boundary address	Size	Peripheral
APB	0x4000 7400 - 0x4000 7FFF	3 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 5C00 - 0x4000 6FFF	5 KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2(1)
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	USART2(1)
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2(1)
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1400 - 0x4000 1FFF	3 KB	Reserved
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6(1)
	0x4000 0800 - 0x4000 0FFF	2 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	Reserved

1. This feature is available on STM32F030x8 devices only. For STM32F030x6 and STM32F060x4, the area is Reserved.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

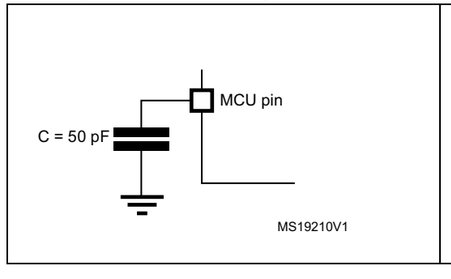
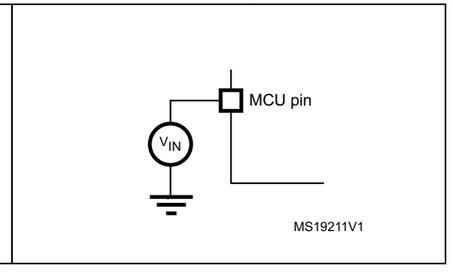


Figure 9. Pin input voltage



6 电气特性

6.1 参数条件

除非另有说明，所有电压均以 VSS 为基准。

6.1.1 最小值和最大值

除非另有说明，最小值和最大值是在最恶劣的环境温度、电源电压和频率条件下通过对环境温度为 TA = 25 °C 和 TA = TAmax （由所选温度范围给出）的 100% 器件进行生产测试来保证的。

基于特性分析结果、设计模拟和 / 或技术特性的数据在表脚注中标出，并未在生产中进行测试。根据表征，最小值和最大值是指样本测试，代表平均值加上或减去标准差的三倍（平均值 ±3σ ）。

6.1.2 典型值

除非另有说明，典型数据基于 TA = 25 °C 、 VDD = VDDA = 3.3 V。它们仅作为设计指南给出，未经测试。

典型的 ADC 精度值是通过在整个温度范围内对标准扩散批次中的一批样品进行表征来确定的，其中 95% 的器件的误差小于或等于所示值（平均值 ±2σ ） .

6.1.3 典型曲线

除非另有说明，所有典型曲线仅作为设计指南给出，未经测试。

6.1.4 负载电容

用于引脚参数测量的负载条件如图 8 所示。

6.1.5 引脚输入电压

图 9 描述了器件引脚上的输入电压测量。

图 8. 引脚负载条件

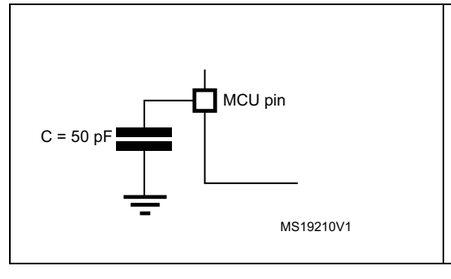
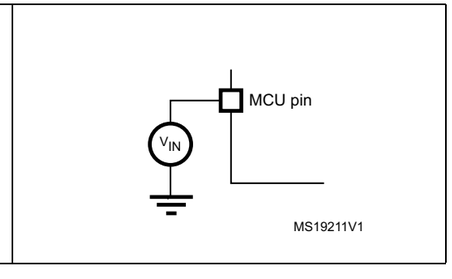
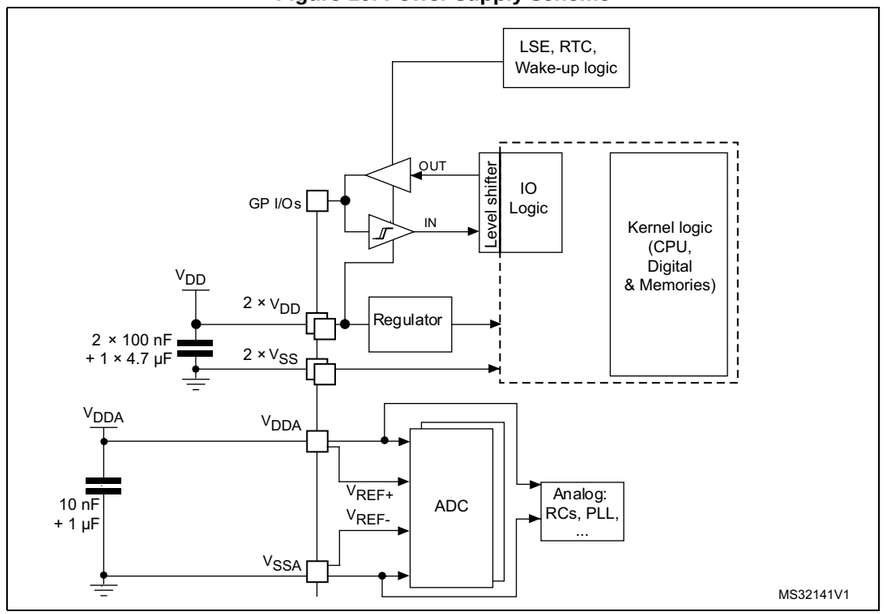


图 9. 引脚输入电压



6.1.6 Power supply scheme

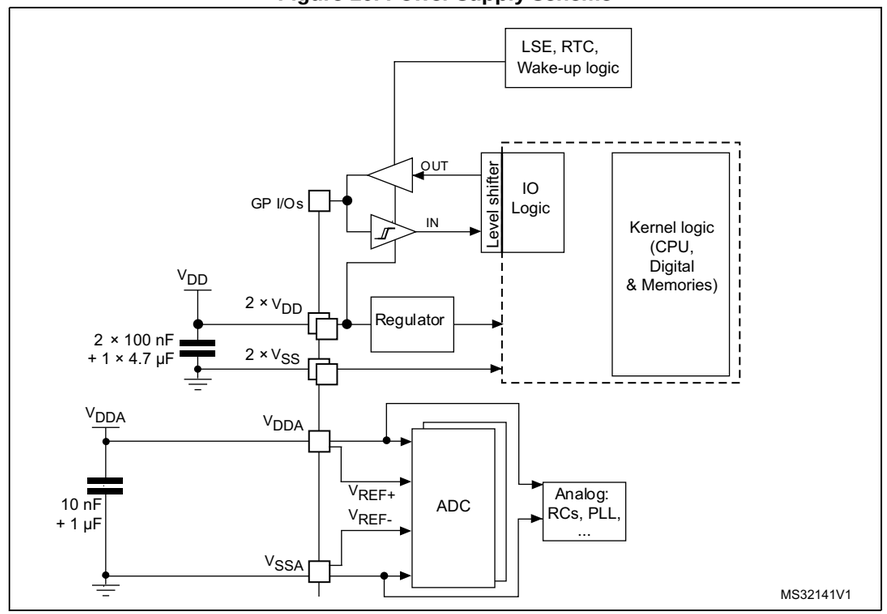
Figure 10. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.6 供电方案

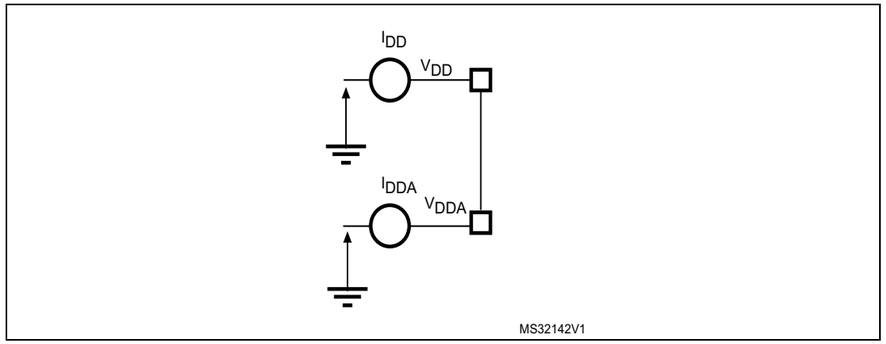
Figure 10. Power supply scheme



注意：每个电源对（VDD/VSS、VDDA/VSSA 等）必须使用滤波陶瓷电容器进行去耦，如上所示。这些电容器必须尽可能靠近或低于 PCB 底部的相应引脚，以确保设备的良好功能。

6.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics*, and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

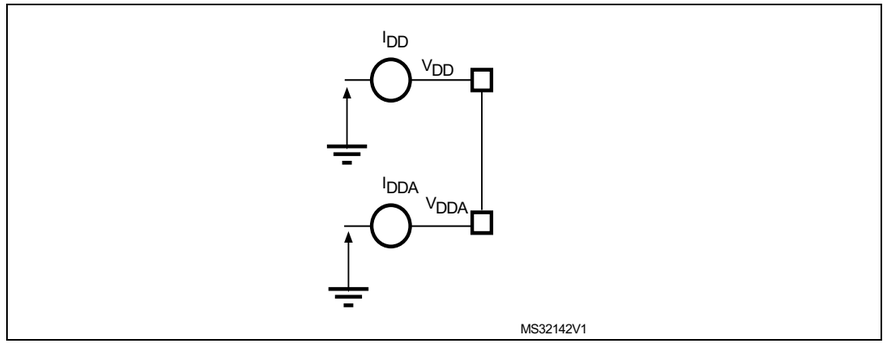
Table 15. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	–0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DD} + 4.0	V
	Input voltage on TTa pins	V_{SS} – 0.3	4.0	V
	Input voltage on any other pin	V_{SS} – 0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 16: Current characteristics* for the maximum allowed injected current values.

6.1.7 电流消耗测量

图 11. 电流消耗测量方案



6.2 绝对最大额定值

应力超过表 15：电压特性、表 16：电流特性和表 17：热特性中列出的绝对最大额定值可能会对器件造成永久性损坏。这些只是压力额定值，并不意味着器件在这些条件下可以正常运行。长时间暴露在最大额定条件下可能会影响器件的可靠性。

Table 15. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	–0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DD} + 4.0	V
	Input voltage on TTa pins	V_{SS} – 0.3	4.0	V
	Input voltage on any other pin	V_{SS} – 0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 16: Current characteristics* for the maximum allowed injected current values.

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x and VDDSDx power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS_x and VSSSD ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD_x or VDDSDx power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x or VSSSD ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN}<V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 15: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 50: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

表 16. 电流特性

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x and VDDSDx power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS_x and VSSSD ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD_x or VDDSDx power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x or VSSSD ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. 所有主电源（VDD、VDDA）和接地（VSS、VSSA）引脚必须始终连接到外部电源供应，在允许的范围内。
2. 该电流消耗必须正确分布在所有 I/O 和控制引脚上。总输出电流不得在两个连续电源引脚之间灌入 / 拉出，参考高引脚数 QFP 封装。
3. 正注入d 最大这些 I/O 上不可能发生此操作，并且输入电压低于指定时也不会发生此操作lue.
4. 。正注入由 VIN>VDD 引起，负注入由 VIN<VSS 引起。绝不能超过 IINJ(PIN)。请参阅表 15：最大允许输入电压值的电压特性。 5. V 诱导正向注射 IN>VDDA 而负注入是由 V 引起的 IN<VSS. IINJ(PIN) 必须永远不会被超越。另请参阅表 15：最大允许输入电压值的电压特性。负注入会干扰器件的模拟性能。请参见表 50 下面的注释 (2)：ADC 精度。
6. 当多个输入进行电流注入时，最大 ΣIINJ(PIN) 是正负注入电流（瞬时值）的绝对和。

表 17. 热特性

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK}	Internal APB clock frequency		0	48	
V_{DD}	Standard operating voltage		2.4	3.6	V
V_{DDA}	Analog operating voltage	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
V_{IN}(1)	Input voltage on FT and FTf pins		V_{SS} –0.3	V_{DD} +4.0	V
	Input voltage on TTa pins		V_{SS} –0.3	4.0	V
	Input voltage on any other pin		V_{SS} –0.3	4.0	V
P_D	Power dissipation at T_A = 85 °C for suffix 6(2)	LQFP64	-	444	mW
		LQFP48	-	364	
		LQFP32	-	357	
		TSSOP20	-	182	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
T_J	Junction temperature range	6 suffix version	–40	105	°C

1. V_{IN} maximum must always be respected. Refer to *Table 16: Current characteristics* for the maximum allowed injected current values.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

6.3 运行条件

6.3.1 一般操作条件

表 18. 一般操作条件

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK}	Internal APB clock frequency		0	48	
V_{DD}	Standard operating voltage		2.4	3.6	V
V_{DDA}	Analog operating voltage	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
V_{IN}(1)	Input voltage on FT and FTf pins		V_{SS} –0.3	V_{DD} +4.0	V
	Input voltage on TTa pins		V_{SS} –0.3	4.0	V
	Input voltage on any other pin		V_{SS} –0.3	4.0	V
P_D	Power dissipation at T_A = 85 °C for suffix 6(2)	LQFP64	-	444	mW
		LQFP48	-	364	
		LQFP32	-	357	
		TSSOP20	-	182	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
T_J	Junction temperature range	6 suffix version	–40	105	°C

1. V_{IN} maximum must always be respected. Refer to *Table 16: Current characteristics* for the maximum allowed injected current values.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 19* are derived from tests performed under the ambient temperature condition summarized in *Table 18*.

Table 19. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate		0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 20* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 20. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	2.06	V
		Rising edge	1.84	1.92	2.10	V
$V_{PDRhyst}$(1)	PDR hysteresis		-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset temporization		1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 21* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 21. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	V
$T_{S\_vrefint}$ (2)	ADC sampling time when reading the internal reference voltage		-	5.1	17.1(3)	µs

6.3.2 上电 / 断电时的工作条件

表 19 中给出的参数源自表 18 中总结的环境温度条件下进行的测试。

表 19. 上电 / 断电时的工作条件

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate		0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 嵌入式复位和电源控制块特性

表 20 中给出的参数源自在表 *18*：一般操作条件中总结的环境温度和 VDD 电源电压条件下执行的测试。

表 20. 嵌入式复位和电源控制模块特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	2.06	V
		Rising edge	1.84	1.92	2.10	V
$V_{PDRhyst}$(1)	PDR hysteresis		-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset temporization		1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

6.3.4 嵌入式参考电压

表 21 中给出的参数源自在表 *18*：一般操作条件中总结的环境温度和 VDD 电源电压条件下执行的测试。

表 21. 嵌入式内部参考电压

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	V
$T_{S\_vrefint}$ (2)	ADC sampling time when reading the internal reference voltage		-	5.1	17.1(3)	µs

Table 21. Embedded internal reference voltage (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V ±10 mV	-	-	10(3)	mV
T_{Coeff}	Temperature coefficient		-	-	100(3)	ppm/°C

1. Data based on characterization results, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.
3. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz and 1 wait state above 24 MHz)
- Prefetch is ON when the peripherals are enabled, otherwise it is OFF (to enable prefetch the PRFTBE bit in the FLASH_ACR register must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 22* to are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

表 21. 嵌入式内部参考电压（续）

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V ±10 mV	-	-	10(3)	mV
T_{Coeff}	Temperature coefficient		-	-	100(3)	ppm/°C

1. Data based on characterization results, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.
3. Guaranteed by design, not tested in production.

6.3.5 电源电流特性

电流消耗是多个参数和因素的函数，例如工作电压、环境温度、 I/O 引脚负载、器件软件配置、工作频率、 I/O 引脚切换速率、存储器中的程序位置和执行的二进制代码。

电流消耗的测量如图 11：电流消耗测量方案中所述。

本节中给出的所有运行模式电流消耗测量均使用简化代码执行，其消耗相当于 CoreMark 代码。

典型和最大电流消耗

MCU 置于以下条件下：

• 所有 I/O 引脚均处于输入模式，静态值为 VDD 或 VSS （无负载） • 除非明确提及，否则所有外设均被禁用 • 闪存访问时间调整为 fHCLK 频率（0 从 0 到 24 MHz 的等待状态和高于 24 MHz 的 1 个等待状态）

• 当外设处于工作状态时预取为 ON 使能，否则关闭（要使能预取，必须在时钟设置和总线预分频之前设置 FLASH_ACR 寄存器中的 PRFTBE 位） • 当外设使能时 fPCLK = fHCLK

表 22 中给出的参数源自在表 18：一般操作条件中总结的环境温度和电源电压条件下进行的测试。

Table 22. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled		Unit
				Typ	Max @ T_A(1) 85 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSI clock, PLL on	48 MHz	22	22.8	mA
			24 MHz	12.2	13.2	
		HSI clock, PLL off	8 MHz	4.4	5.2	
	Supply current in Run mode, code executing from RAM	HSI clock, PLL on	48 MHz	22.2	23.2	
			24 MHz	11.2	12.2	
		HSI clock, PLL off	8 MHz	4.0	4.5	
	Supply current in Sleep mode, code executing from Flash or RAM	HSI clock, PLL on	48 MHz	14	15.3	
			24 MHz	7.3	7.8	
		HSI clock, PLL off	8 MHz	2.6	2.9	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 23. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions(1)	f_{HCLK}	V_{DDA} = 3.6 V		Unit
				Typ	Max @ T_A(2) 85 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	175	215	µA
		HSE bypass, PLL off	8 MHz	3.9	4.9	
			1 MHz	3.9	4.1	
		HSI clock, PLL on	48 MHz	244	275	
		HSI clock, PLL off	8 MHz	85	105	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	174	215	
		HSE bypass, PLL off	8 MHz	3.9	4.9	
			1 MHz	3.9	4.9	
		HSI clock, PLL on	48 MHz	244	299	
		HSI clock, PLL off	8 MHz	85	105	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.

Table 22。 VDD = 3.6 时 VDD 电源的典型和最大电流消耗

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled		Unit
				Typ	Max @ T_A(1) 85 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSI clock, PLL on	48 MHz	22	22.8	mA
			24 MHz	12.2	13.2	
		HSI clock, PLL off	8 MHz	4.4	5.2	
	Supply current in Run mode, code executing from RAM	HSI clock, PLL on	48 MHz	22.2	23.2	
			24 MHz	11.2	12.2	
		HSI clock, PLL off	8 MHz	4.0	4.5	
	Supply current in Sleep mode, code executing from Flash or RAM	HSI clock, PLL on	48 MHz	14	15.3	
			24 MHz	7.3	7.8	
		HSI clock, PLL off	8 MHz	2.6	2.9	

1. Data based on characterization results, not tested in production unless otherwise specified.

表 23. VDDA 电源的典型和最大电流消耗

Symbol	Parameter	Conditions(1)	f_{HCLK}	V_{DDA} = 3.6 V		Unit
				Typ	Max @ T_A(2) 85 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	175	215	µA
		HSE bypass, PLL off	8 MHz	3.9	4.9	
			1 MHz	3.9	4.1	
		HSI clock, PLL on	48 MHz	244	275	
		HSI clock, PLL off	8 MHz	85	105	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	174	215	
		HSE bypass, PLL off	8 MHz	3.9	4.9	
			1 MHz	3.9	4.9	
		HSI clock, PLL on	48 MHz	244	299	
		HSI clock, PLL off	8 MHz	85	105	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.

Table 24. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD} = V_{DDA})	Max(1)	Unit
			3.6 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	19	48	µA
		Regulator in low-power mode, all oscillators OFF	5	32	
	Supply current in Standby mode	LSI ON and IWDG ON	2	-	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 25. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})	Max(1)	Unit
				3.6 V	T_A = 85 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run or low power mode, all oscillators OFF	2.9	3.5	µA
	Supply current in Standby mode		LSI ON and IWDG ON	3.3	-	
			LSI OFF and IWDG OFF	2.8	3.5	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode or low power, all oscillators OFF	1.7	-	
	Supply current in Standby mode		LSI ON and IWDG ON	2.3	-	
			LSI OFF and IWDG OFF	1.4	-	

1. Data based on characterization results, not tested in production.

表 24. 停止和待机模式下的典型和最大 VDD 消耗

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD} = V_{DDA})	Max(1)	Unit
			3.6 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	19	48	µA
		Regulator in low-power mode, all oscillators OFF	5	32	
	Supply current in Standby mode	LSI ON and IWDG ON	2	-	

1. Data based on characterization results, not tested in production unless otherwise specified.

表 25. 停止和待机模式下的典型和最大 VDDA 消耗

Symbol	Parameter	Conditions		Typ @V_{DD} (V_{DD} = V_{DDA})	Max(1)	Unit
				3.6 V	T_A = 85 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run or low power mode, all oscillators OFF	2.9	3.5	µA
	Supply current in Standby mode		LSI ON and IWDG ON	3.3	-	
			LSI OFF and IWDG OFF	2.8	3.5	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode or low power, all oscillators OFF	1.7	-	
	Supply current in Standby mode		LSI ON and IWDG ON	2.3	-	
			LSI OFF and IWDG OFF	1.4	-	

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD}=V_{DDA}=3.3 V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state above)
- Prefetch is ON when the peripherals are enabled, otherwise it is OFF
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively
- A development tool is connected to the board and the parasitic pull-up current is around 30 µA

Table 26. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	23.3	11.5	mA
			8 MHz	4.5	3.0	
I_{DDA}	Supply current in Run mode from V_{DDA} supply		48 MHz	158	158	µA
			8 MHz	2.43	2.43	

典型电流消耗

MCU 置于以下条件下:

• VDD=VDDA=3.3 V• 所有 I/O 引脚均处于模拟输入配置 • Flash 访问时间调整为 fHCLK 频率（0 从 0 到 24 MHz 的等待状态，以上 1 个等待状态） • 当外设使能时预取为 ON，否则为 ON OFF• 外设使能时，fPCLK = fHCLK• 频率大于 8 MHz 时使用 PLL• 频率为 4 MHz 、 2 MHz 、 1 MHz 和 500 kHz 时分别使用 2 、 4 、 8 和 16 的 AHB 预分频器 • 开发工具连接到电路板和寄生上拉电流约为 30 µA

表 26. 运行模式下的典型电流消耗，从闪存运行数据处理的代码

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	23.3	11.5	mA
			8 MHz	4.5	3.0	
I_{DDA}	Supply current in Run mode from V_{DDA} supply		48 MHz	158	158	µA
			8 MHz	2.43	2.43	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 44: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 26: Typical current consumption in Run mode, code with data processing running from Flash*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

I/O 系统电流消耗

I/O 系统的电流消耗有两个组成部分：静态和动态 c.

I/O 静态电流消耗

当引脚外部保持低电平时，所有用作带上拉输入的 I/O 都会产生电流消耗。该电流消耗的值可以通过使用表 44：I/O 静态特性中给出的上拉 / 下拉电阻值来简单计算。

对于输出引脚，还必须考虑任何外部下拉或外部负载来估计电流消耗。

如果外部施加中间电压电平，则 I/O 配置为输入会产生额外的 I/O 电流消耗。该电流消耗是由用于判别输入值的输入施密特触发电路引起的。除非应用需要这种特定配置，否则可以通过在模拟模式下配置这些 I/O 来避免这种电源电流消耗。 ADC 输入引脚的情况尤其如此，应将其配置为模拟输入。

警告 ：由于外部电磁噪声，任何浮动输入引脚也可能稳定到中间电压电平或无意中切换。为了避免与浮动引脚相关的电流消耗，它们必须配置为模拟模式，或者在内部强制为确定的数字值。这可以通过使用上拉 / 下拉电阻或将引脚配置为输出模式来完成。

I/O 动态电流消耗

除了之前测量的内部外设电流消耗（请参见表 26：运行模式下的典型电流消耗，从闪存运行数据处理的代码）之外，应用程序使用的 I/O 也会影响电流消耗。当 I/O 引脚切换时，它使用来自 MCU 电源电压的电流为 I/O 引脚电路供电，并对连接到该引脚的电容负载（内部或外部）进行充电 / 放电：

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

在哪里

ISW 是开关 I/O 对容性负载充电 / 放电所吸收的电流 VDD 是 MCU 电源电压

fSW 是 I/O 开关频率 C 是 I/O 引脚所见的总电容： $C = CINT + CEXT + CS$ CS 是包括焊盘引脚在内的 PCB 板电容。

测试引脚配置为推挽输出模式，并由软件以固定频率切换。

Table 27. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.18	mA
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DD} = 3.3 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	

1. C_S = 7 pF (estimated value)

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 28* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The event used to wake up the device depends from the current operating mode:

- Stop or sleep mode: the wakeup event is WFE.
- The wakeup pin used in stop and sleep mode is PA0 and in standby mode is PA1.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 28. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = 3.3 V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.2	5	µs
$t_{WUSTANDBY}$	Wakeup from Standby mode		50.96	-	
$t_{WUSLEEP}$	Wakeup from Sleep mode		1.1	-	

表 27. 开关输出 I/O 电流消耗

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.18	mA
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DD} = 3.3 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	

1. C_S = 7 pF (estimated value)

6.3.6 从低功耗模式唤醒时间

表 28 中给出的唤醒时间是在唤醒阶段使用 8 MHz HSI RC 振荡器测量的。用于唤醒设备的事件取决于当前的操作模式:

- 停止或睡眠模式：唤醒事件为 WFE。
- 停止和睡眠模式下使用的唤醒引脚为 PA0，待机模式下使用的唤醒引脚为 PA1。

所有时序均源自在环境温度和 VDD 电源电压条件下执行的测试，如表 18：一般工作条件中所总结。

表 28. 低功耗模式唤醒时序

Symbol	Parameter	Conditions	Typ @V_{DD} = 3.3 V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.2	5	µs
$t_{WUSTANDBY}$	Wakeup from Standby mode		50.96	-	
$t_{WUSLEEP}$	Wakeup from Sleep mode		1.1	-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

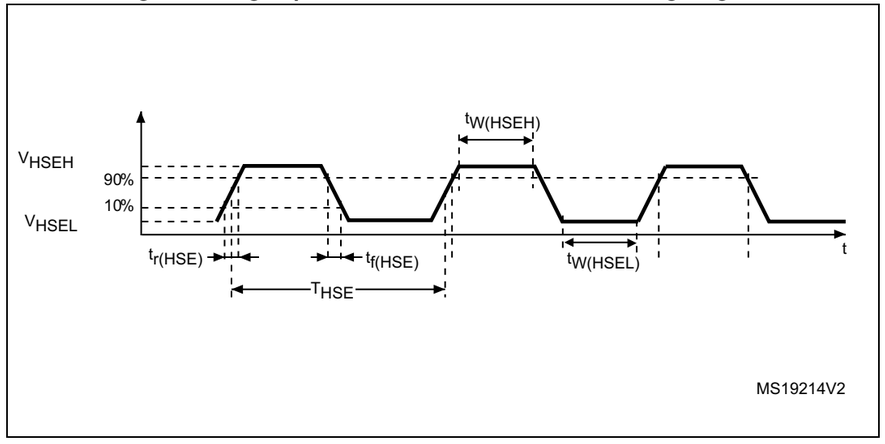
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12: High-speed external clock source AC timing diagram*.

Table 29. High-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 12. High-speed external clock source AC timing diagram



6.3.7 外部时钟源特性

从外部源生成的高速外部用户时钟

在旁路模式下，HSE 振荡器关闭，输入引脚为标准 GPIO。

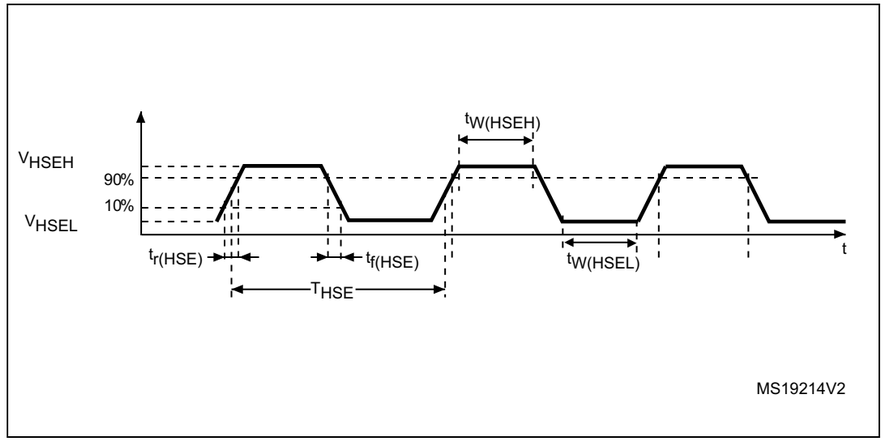
外部时钟信号必须遵守第 6.3.14 节中的 I/O 特性。不过，推荐的时钟输入波形如图 12：高速外部时钟源交流时序图所示。

表 29. 高速外部用户时钟特性

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	

1. Guaranteed by design, not tested in production.

图 12. 高速外部时钟源 AC 时序图



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

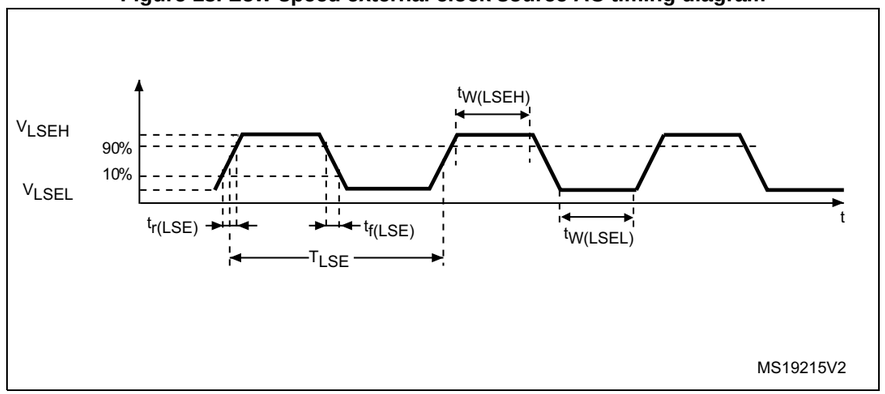
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 30. Low-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 13. Low-speed external clock source AC timing diagram



从外部源生成的低速外部用户时钟

在旁路模式下，LSE 振荡器关闭，输入引脚为标准 GPIO。

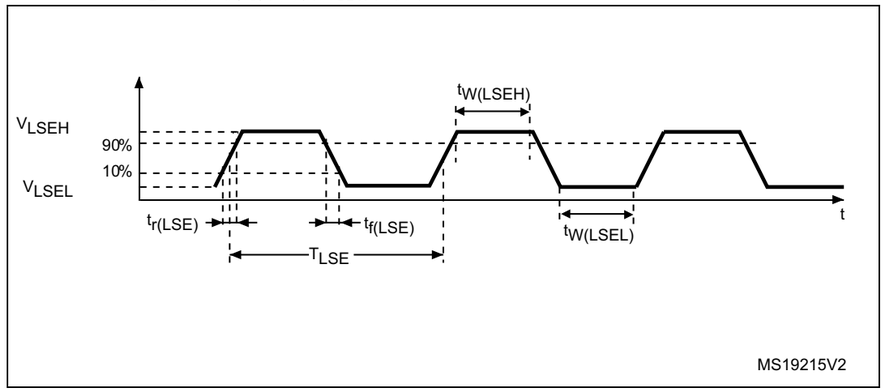
外部时钟信号必须遵守第 6.3.14 节中的 I/O 特性。然而，推荐的时钟输入波形如图 13 所示。

表 30. 低速外部用户时钟特性

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	50	

1. Guaranteed by design, not tested in production.

图 13. 低速外部时钟源 AC 时序图



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 31*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 31. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency		4	8	32	MHz
R_F	Feedback resistor		-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-		8.5	mA
		V_{DD}=3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

由晶体 / 陶瓷谐振器生成的高速外部时钟

高速外部 (HSE) 时钟可由 4 至 32 MHz 晶体 / 陶瓷谐振器振荡器提供。本段中给出的所有信息均基于使用表 31 中指定的典型外部组件获得的设计仿真结果。在应用中，谐振器和负载电容器必须尽可能靠近振荡器引脚放置，以最大限度地减少输出失真和启动稳定时间。有关谐振器特性（频率、封装、精度）的更多详细信息，请咨询晶体谐振器制造商。

表 31. HSE 振荡器特性

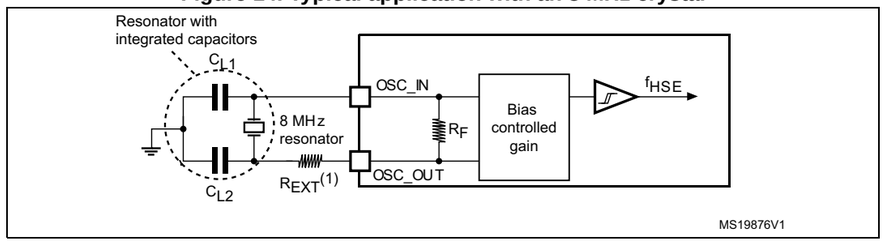
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency		4	8	32	MHz
R_F	Feedback resistor		-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-		8.5	mA
		V_{DD}=3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}=3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

对于 CL1 和 CL2，建议使用 5 pF 至 20 pF 范围（典型值）的高质量外部陶瓷电容器，该电容器专为高频应用而设计，并根据晶体或谐振器的要求进行选择（见图 14 ）。 CL1 和 CL2 通常尺寸相同。晶体制造商通常指定负载电容，该电容是 CL1 和 CL2 的串联组合。在确定 CL1 和 CL2 的尺寸时，必须包括 PCB 和 MCU 引脚电容（ 10 pF 可用作引脚和电路板组合电容的粗略估计）。

笔记：有关选择晶振的信息，请参阅应用笔记 AN2867“ST 微控制器振荡器设计指南 ”，可从 ST 网站 www.st.com 获取。

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

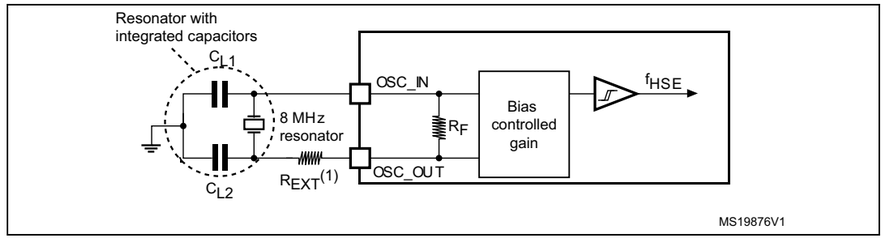
The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 32. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	-	µA
		LSEDRV[1:0]= 01 medium low driving capability	-	0.8	-	
		LSEDRV[1:0] = 10 medium high driving capability	-	1.1	-	
		LSEDRV[1:0]=11 higher driving capability	-	1.4	-	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

图 14. 8 MHz 晶体的典型应用



1。 REXT 值取决于晶体特性。

由晶体谐振器产生的低速外部时钟

低速外部 (LSE) 时钟可由 32.768 kHz 晶体谐振器振荡器提供。本段中给出的所有信息均基于使用表 32 中指定的典型外部组件获得的设计仿真结果。在应用中，谐振器和负载电容器必须尽可能靠近振荡器引脚放置，以最大限度地减少输出失真和启动稳定时间。有关谐振器特性（频率、封装、精度）的更多详细信息，请咨询晶体谐振器制造商。

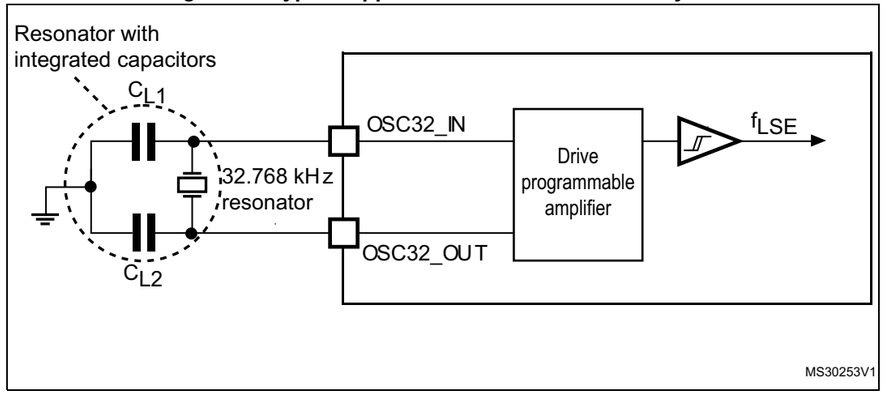
表 32. LSE 振荡器特性 (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	-	µA
		LSEDRV[1:0]= 01 medium low driving capability	-	0.8	-	
		LSEDRV[1:0] = 10 medium high driving capability	-	1.1	-	
		LSEDRV[1:0]=11 higher driving capability	-	1.4	-	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 33* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

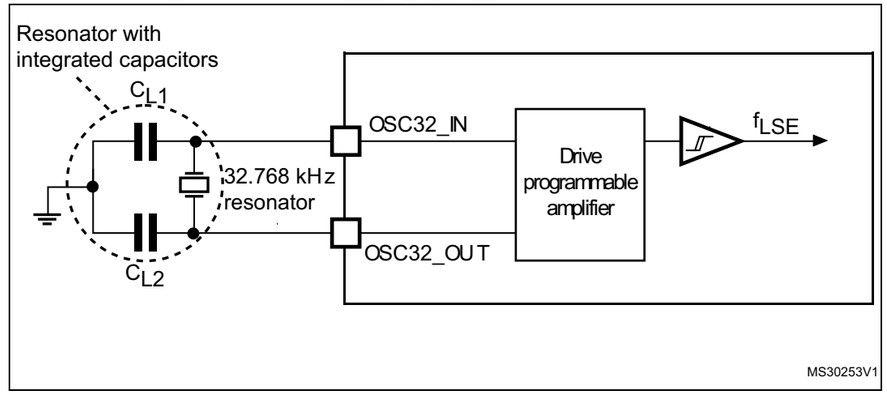
Table 33. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency		-	8		MHz
TRIM	HSI user trimming step		-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle		45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)(3)	T_A = –40 to 85 °C	-	±5	-	%
		T_A = 25 °C	-	±1	-	%
$t_{su(HSI)}$	HSI oscillator startup time		1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption		-	80	-	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. With user calibration.

笔记： 有关选择晶振的信息，请参阅应用笔记 AN2867“ST 微控制器振荡器设计指南”，可从 ST 网站 www.st.com 获取。

图 15. 32.768 kHz 晶体的典型应用



笔记： OSC32_IN 和 OSC32_OUT 之间无需外接电阻，且禁止外加电阻。

6.3.8 内部时钟源特性

表 33 中给出的参数源自表 18：一般操作条件中总结的环境温度和电源电压条件下执行的测试。提供的曲线是表征结果，未经生产测试。

高速内部 (HSI) RC 振荡器

表 33. HSI 振荡器特性 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency		-	8		MHz
TRIM	HSI user trimming step		-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle		45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)(3)	T_A = –40 to 85 °C	-	±5	-	%
		T_A = 25 °C	-	±1	-	%
$t_{su(HSI)}$	HSI oscillator startup time		1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption		-	80	-	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. With user calibration.

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 34. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency		-	14		MHz
TRIM	HSI14 user-trimming step		-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle		45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 85 °C	-	±5	-	%
$t_{su(HSI14)}$	HSI14 oscillator startup time		1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption		-	100	-	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 35. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	-	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 36* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18: General operating conditions*.

高速内部 14 MHz (HSI14) RC 振荡器（ADC 专用）

表 34. HSI14 振荡器特性 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency		-	14		MHz
TRIM	HSI14 user-trimming step		-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle		45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 85 °C	-	±5	-	%
$t_{su(HSI14)}$	HSI14 oscillator startup time		1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption		-	100	-	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

低速内部 (LSI) RC 振荡器

Table 35. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	-	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL 特性

表 36 中给出的参数源自表 18：一般操作条件中总结的环境温度和电源电压条件下执行的测试。

Table 36. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 37. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	-	53.5	-	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +85 °C	-	30	-	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	-	30	-	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA
V_{prog}	Programming voltage		2.4	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 38. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions)	1	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	20	Years

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

表 36. PLL 特性

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 内存特性

闪存

除非另有说明，特性在 TA = –40 至 85 °C 下给出。

表 37. 闪存特性

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	-	53.5	-	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +85 °C	-	30	-	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	-	30	-	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA
V_{prog}	Programming voltage		2.4	-	3.6	V

1. Guaranteed by design, not tested in production.

表 38. 闪存耐用性和数据保留

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions)	1	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	20	Years

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC 特性

在器件表征期间以样本为基础进行敏感性测试 .

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 39*. They are based on the EMS levels and classes defined in application note AN1709.

Table 39. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-4	3B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

功能性 EMS （电磁敏感性）

在设备上执行一个简单的应用程序（通过 I/O 端口切换 2 个 LED ）。该设备受到两次电磁事件的压力，直到发生故障。故障由 LED 指示：

- 静电放电 (ESD) （正和负）作用于所有器件引脚，直至发生功能干扰。该测试符合 IEC 61000-4-2 标准。• FTB：通过 100 pF 电容器向 VDD 和 VSS 施加快速瞬变电压突发（正和负），直到发生功能干扰。该测试符合 IEC 61000-4-4 标准。

设备重置允许恢复正常操作。

测试结果如表 39 所示。它们基于应用笔记 AN1709 中定义的 EMS 级别和类别。

表 39. EMS 特性

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-4	3B

设计强化软件以避免噪音问题

EMC 表征和优化是通过典型应用环境和简化的 MCU 软件在组件级别执行的。应该指出的是，良好的 EMC 性能高度依赖于用户应用程序，特别是软件。

因此，建议用户根据其应用所需的 EMC 级别应用 EMC 软件优化和资格预审测试。

软件推荐

软件流程图必须包括失控条件的管理，例如：

- 程序计数器损坏 • 意外重置 • 关键

数据损坏（控制寄存器 … ）

资格预审试验

大多数常见故障（意外复位和程序计数器损坏）可以通过手动强制 NRST 引脚或振荡器引脚处于低状态 1 秒来重现。

为了完成这些试验，可以在规格值范围内直接在器件上施加 ESD 应力。当检测到意外行为时，可以强化软件以防止发生不可恢复的错误（请参阅应用笔记 AN1015 ）。

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 40. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	-3	dBµV
			30 to 130 MHz	28	
			130 MHz to 1GHz	23	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 41. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	500	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 42. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

电磁干扰（ EMI ）

在执行一个简单的应用程序（通过 I/O 端口切换 2 个 LED ）时，会监控设备发出的电磁场。该发射测试符合 IEC 61967-2 标准，该标准指定了测试板和引脚负载。

表 40. EMI 特性

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	-3	dBµV
			30 to 130 MHz	28	
			130 MHz to 1GHz	23	
			SAE EMI Level	4	-

6.3.12 电气灵敏度特性

基于使用特定测量方法的三种不同测试（ ESD 、 LU ），对器件施加压力以确定其电气灵敏度方面的性能。

静电放电（ ESD ）

根据每个引脚组合，对每个样品的引脚施加静电放电（正脉冲，然后负脉冲，间隔 1 秒）。样本大小取决于器件中电源引脚的数量（ 3 个部分 × (n+1) 个电源引脚）。该测试符合 JESD22-A114/C101 标准。

表 41. ESD 绝对最大额定值

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	500	

1. Data based on characterization results, not tested in production.

静态闩锁

需要对六个部件进行两次互补的静态测试来评估闩锁性能：

- 向每个电源引脚施加电源过压
- 向每个输入、输出和可配置 I/O 引脚施加电流注入

这些测试符合 EIA/JESD 78A IC 闩锁标准。

表 42. 电气灵敏度

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (more than 5 LSB TUE), out of conventional limits of current injection on adjacent pins (more than –5 µA) or other functional failure (reset occurrence or oscillator frequency deviation, for example).

The characterization results are given in *Table 43*.

Table 43. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on all FT and FTf pins with induced leakage current on adjacent pins less than –5 µA	–5	NA	
	Injected current on all TTa pins with induced leakage current on adjacent pins less than –5 µA	–5	+5	
	Injected current on all TC and RESET pins with induced leakage current on adjacent pins less than –5 µA	–5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the conditions summarized in *Table 18: General operating conditions*. All I/Os are designed as CMOS and TTL compliant.

Table 44. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DD}+0.07(1)	V
		FT and FTf I/O	-	-	0.475 V_{DD}–0.2(1)	
		BOOT0	-	-	0.3 V_{DD}–0.3(1)	
		All I/Os except BOOT0 pin	-	-	0.3 V_{DD}	

6.3.13 I/O 电流注入特性

一般而言，在产品正常运行期间，应避免由于外部电压低于 VSS 或高于 VDD （对于标准的支持 V 的 I/O 引脚）而向 I/O 引脚注入电流。然而，为了在意外发生异常注入的情况下表明微控制器的鲁棒性，在器件表征期间对样本进行了敏感性测试。

Functional susceptibility to I/O current injection

当在器件上执行简单的应用程序时，器件会因将电流注入到以浮动输入模式编程的 I/O 引脚而承受压力。当电流一次注入 I/O 引脚时，会检查器件是否存在功能故障。

故障由超出范围的参数指示：ADC 错误超过特定限制（超过 5 LSB TUE ）、超出相邻引脚上电流注入的常规限制（超过 –5 µA ）或其他功能故障（例如发生复位或振荡器频率偏差）。

The characterization results are given in *Table 43*.

表 43. I/O 电流注入敏感性

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on all FT and FTf pins with induced leakage current on adjacent pins less than –5 µA	–5	NA	
	Injected current on all TTa pins with induced leakage current on adjacent pins less than –5 µA	–5	+5	
	Injected current on all TC and RESET pins with induced leakage current on adjacent pins less than –5 µA	–5	+5	

6.3.14 I/O 端口特性

一般输入 / 输出特性

除非另有说明，表 44 中给出的参数源自在表 18：一般操作条件中总结的条件下进行的测试。所有 I/O 均设计为符合 CMOS 和 TTL 标准。

表 44. I/O 静态特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DD}+0.07(1)	V
		FT and FTf I/O	-	-	0.475 V_{DD}–0.2(1)	
		BOOT0	-	-	0.3 V_{DD}–0.3(1)	
		All I/Os except BOOT0 pin	-	-	0.3 V_{DD}	

Table 44. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	TC and TTa I/O	0.445 V_{DD}+0.398(1)	-	-	V
		FT and FTf I/O	0.5 V_{DD}+0.2(1)	-	-	
		BOOT0	0.2 V_{DD}+0.95(1)	-	-	
		All I/Os except BOOT0 pin	0.7 V_{DD}	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
		BOOT0	-	300(1)	-	
I_{lkg}	Input leakage current (2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O (3) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor (4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor (4)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. Leakage could be higher than maximum value, if negative current is injected on adjacent pins. Refer to *Table 43: I/O current injection susceptibility*.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 16* for standard I/Os, and in *Figure 17* for 5 V tolerant I/Os.

表 44. I/O 静态特性（续）

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	TC and TTa I/O	0.445 V_{DD}+0.398(1)	-	-	V
		FT and FTf I/O	0.5 V_{DD}+0.2(1)	-	-	
		BOOT0	0.2 V_{DD}+0.95(1)	-	-	
		All I/Os except BOOT0 pin	0.7 V_{DD}	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
		BOOT0	-	300(1)	-	
I_{lkg}	Input leakage current (2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O (3) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor (4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor (4)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance		-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. Leakage could be higher than maximum value, if negative current is injected on adjacent pins. Refer to *Table 43: I/O current injection susceptibility*.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

所有 I/O 均符合 CMOS 和 TTL 标准（无需软件配置）。它们的特性不仅仅涵盖严格的 CMOS 技术或 TTL 参数。对于标准 I/O，这些要求的覆盖范围如图 16 所示；对于 5 V 耐受 I/O，这些要求的覆盖范围如图 17 所示。

Figure 16. TC and TTa I/O input characteristics

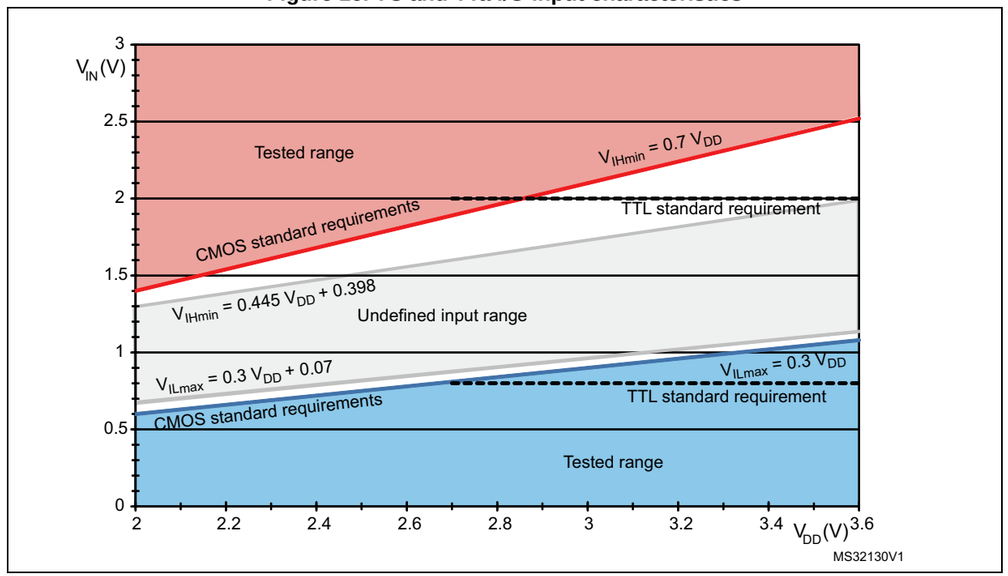


Figure 17. Five volt tolerant (FT and FTf) I/O input characteristics

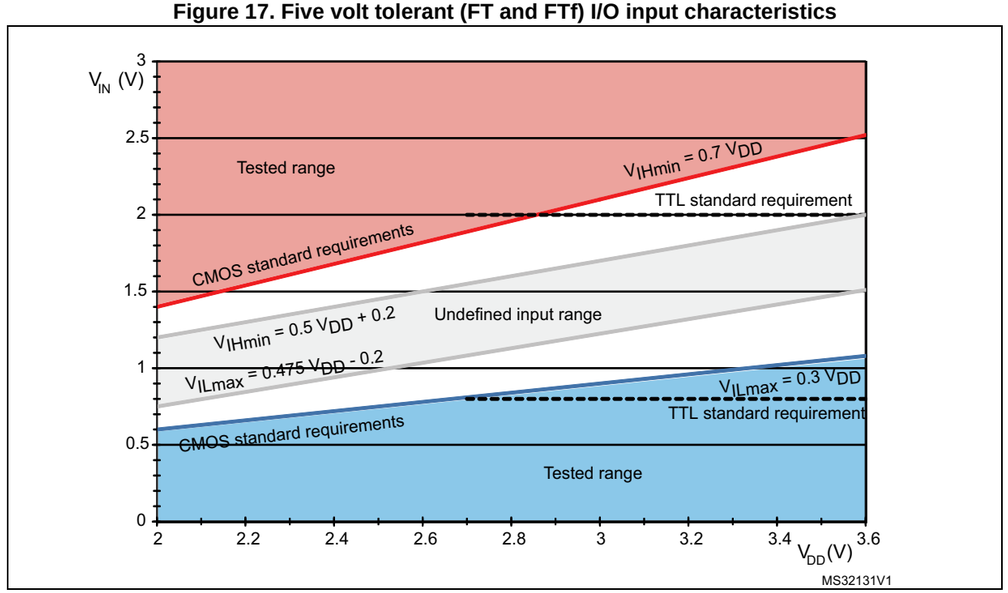


Figure 16. TC and TTa I/O input characteristics

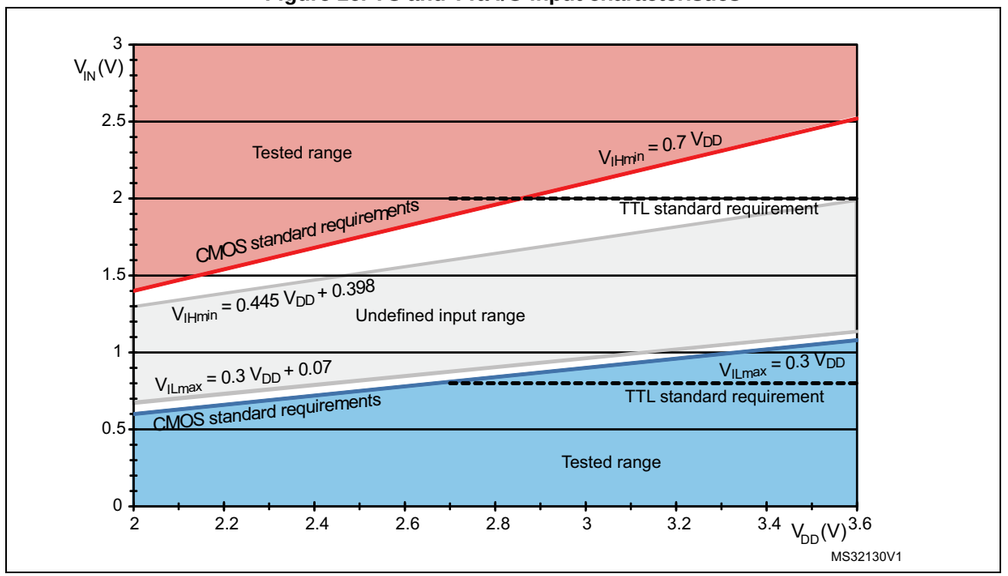
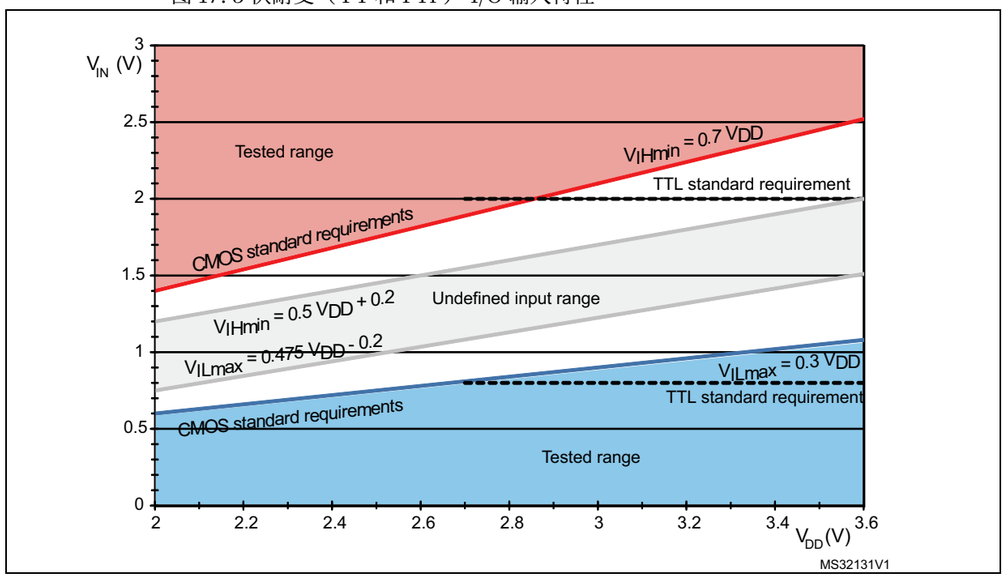


图 17. 5 伏耐受（ FT 和 FTf ） I/O 输入特性



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 16: Current characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 16: Current characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

Table 45. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 5 pins are sunk at the same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 5 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA 2.4 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OLFM+}(1)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA	-	0.4	V

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 16: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 16: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Data based on characterization results. Not tested in production.

输出驱动电流

GPIO （通用输入 / 输出）可以灌入或拉出高达 +/-8 mA 的电流，灌入或拉出高达 +/- 20 mA 的电流（使用宽松的 VOL/VOH ）。

在用户应用中，必须限制可驱动电流的 I/O 引脚数量，以遵守第 6.2 节中指定的绝对最大额定值：

- VDD 上所有 I/O 提供的电流总和，加上 VDD 提供的 MCU 最大运行消耗，不能超过绝对最大额定值 ΣIVDD （参见表 16：电流特性）。
- VSS 上所有 I/O 吸收的电流加上 VSS 上 MCU 吸收的最大运行消耗的总和，不能超过绝对最大额定值。绝对最大额定值 ΣIVSS （参见表 16：电流特性）。

输出电压电平

除非另有说明，下表中给出的参数均来自于表 18：一般工作条件中总结的环境温度和 VDD 电源电压条件下执行的测试。所有 I/O 均符合 CMOS 和 TTL 标准（ FT 、 TTa 或 TC，除非另有说明）。

Table 45. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 5 pins are sunk at the same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 5 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA 2.4 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OLFM+}(1)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA	-	0.4	V

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 16: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 16: Current characteristics* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Data based on characterization results. Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 18* and *Table 46*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 46. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	
			C_L = 50 pF, V_{DD} = 2.4 V to 2.7 V	-	20	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
FM+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	12(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	34(3)	
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0091 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 18*.
3. Guaranteed by design, not tested in production.
4. When FM+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xx reference manual RM0091 for a detailed description of FM+ I/O configuration.

输入 / 输出交流特性

输入 / 输出交流特性的定义和值分别如图 18 和表 46 所示。

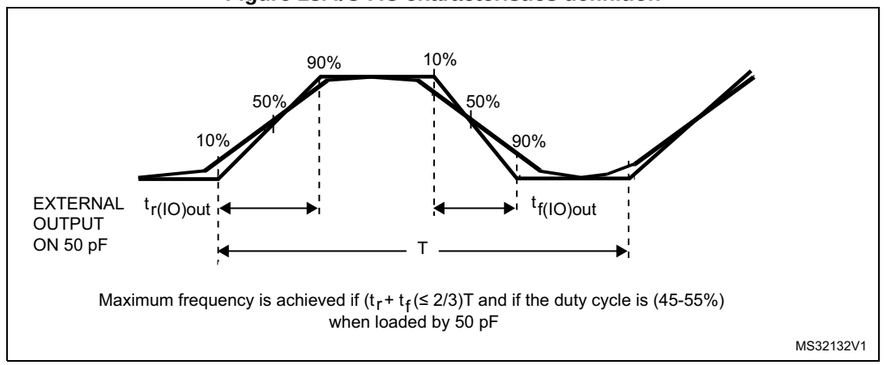
除非另有说明，给出的参数均来自于表 18：一般工作条件中总结的环境温度和 VDD 电源电压条件下进行的测试。

表 46. I/O 交流特性 (1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	
			C_L = 50 pF, V_{DD} = 2.4 V to 2.7 V	-	20	
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
FM+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	12(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} = 2.4 V to 3.6 V	-	34(3)	
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0091 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 18*.
3. Guaranteed by design, not tested in production.
4. When FM+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xx reference manual RM0091 for a detailed description of FM+ I/O configuration.

Figure 18. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 44: I/O static characteristics*).

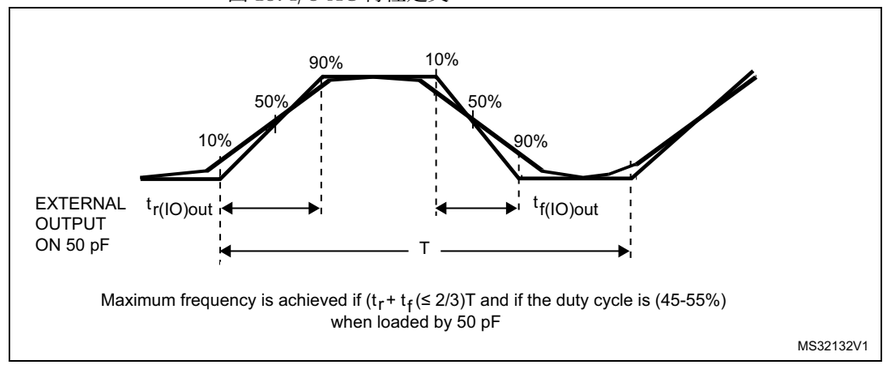
Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 18: General operating conditions*.

Table 47. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		–0.3	-	0.8(1)	V
$V_{IH(NRST)}$	NRST input high level voltage		2	-	V_{DD}+0.3(1)	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$	NRST input filtered pulse		-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse		300(1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

图 18. I/O AC 特性定义



6.3.15 NRST 引脚特性

NRST 引脚输入驱动器采用 CMOS 技术。它连接到永久上拉电阻 RPU （参见表 44：I/O 静态特性）。

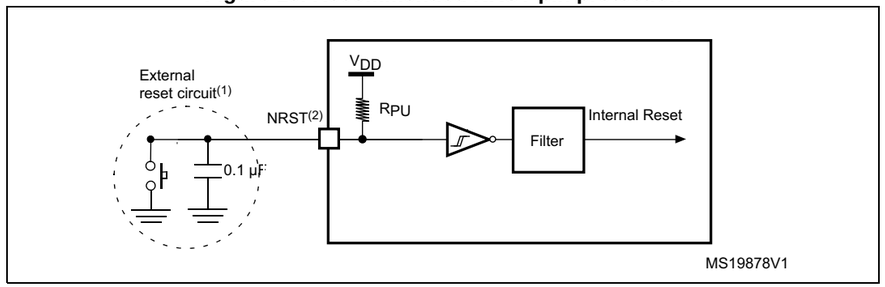
除非另有说明，下表中给出的参数均来自于表 18：一般工作条件中总结的环境温度和 VDD 电源电压条件下执行的测试。

表 47. NRST 引脚特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		–0.3	-	0.8(1)	V
$V_{IH(NRST)}$	NRST input high level voltage		2	-	V_{DD}+0.3(1)	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$	NRST input filtered pulse		-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse		300(1)	-	-	ns

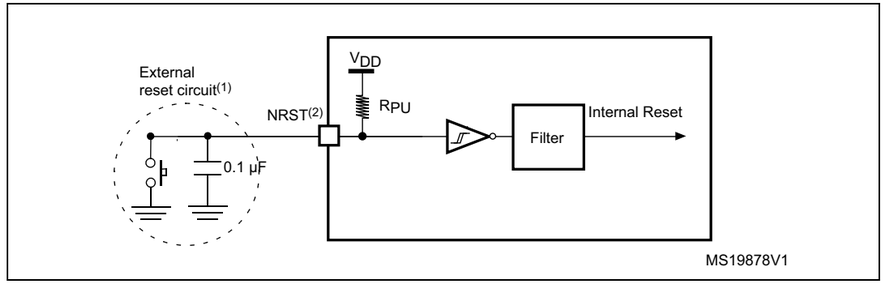
1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 47: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

图 19. 推荐的 NRST 引脚保护



1. 复位网络可保护器件免受寄生复位的影响。2。用户必须确保 NRST 引脚上的电平可以低于表 47：NRST 引脚特性中指定的 VIL(NRST) 最大电平。否则设备将不会考虑重置。

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 48* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 18: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 48. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON		2.4	-	3.6	V
f_{ADC}	ADC clock frequency		0.6	-	14	MHz
f_S (1)	Sampling rate		0.05	-	1	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	See *Equation 1* and *Table 49* for details	-	-	50	kΩ
R_{ADC} (1)	Sampling switch resistance		-	-	1	kΩ
C_{ADC} (1)	Internal sample and hold capacitor		-	-	8	pF
t_{CAL} (1)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{latr} (1)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 14 MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 12 MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.188	-	0.259	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (1)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (1)	Power-up time		0	0	1	µs
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.

6.3.16 12 位 ADC 特性

除非另有说明，表 48 中给出的参数是在表 18：一般工作条件中总结的环境温度、 fPCLK2 频率和 VDDA 电源电压条件下进行的测试得出的初步值。

注意：建议每次通电后进行校准。

表 48. ADC 特性

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON		2.4	-	3.6	V
f_{ADC}	ADC clock frequency		0.6	-	14	MHz
f_S (1)	Sampling rate		0.05	-	1	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	See *Equation 1* and *Table 49* for details	-	-	50	kΩ
R_{ADC} (1)	Sampling switch resistance		-	-	1	kΩ
C_{ADC} (1)	Internal sample and hold capacitor		-	-	8	pF
t_{CAL} (1)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{latr} (1)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 14 MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 12 MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.188	-	0.259	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (1)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (1)	Power-up time		0	0	1	µs
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 49. R_{AIN} max for f_{ADC} = 14 MHz

T_S (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 50. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.7 V to 3.6 V T_A = −40 to 85 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

上面的公式（公式 1）用于确定误差低于 1/4 LSB 时允许的最大外部阻抗。这里是 N = 12 （来自 12 位分辨率）。

表 49. fADC **= 14** MHz 的 RAIN 最大值

T_S (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

表 50. ADC 精度 (1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.7 V to 3.6 V T_A = −40 to 85 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC 精度与负注入电流：应避免在任何标准（非稳健）模拟输入引脚上注入负电流，因为这会显着降低在另一个模拟输入上执行的转换的精度。建议在标准模拟引脚上添加一个肖特基二极管（引脚接地），这可能会注入负电流。第 6.3.14 节中为 IINJ(PIN) 和 ΣIINJ(PIN) 指定的限值内的任何正注入电流都不会影响 ADC 精度。
3. 。在受限的 VDDA 、频率和温度范围内可以实现更好的性能。
4. 数据基于表征结果，未经生产测试。

Figure 20. ADC accuracy characteristics

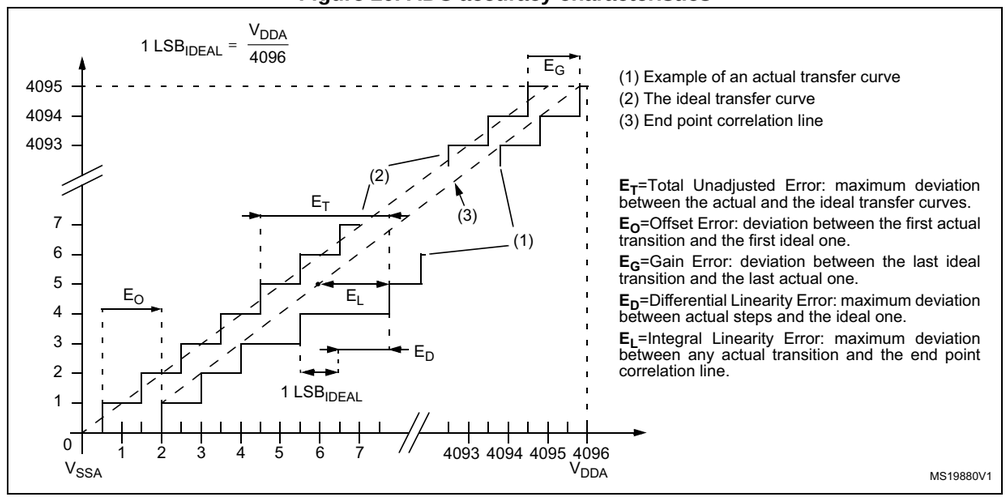
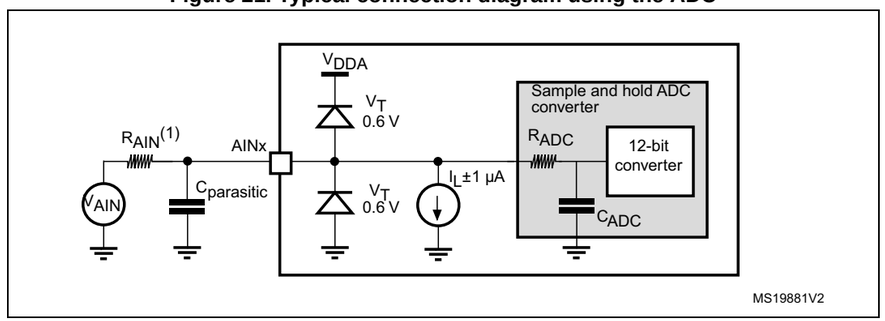


Figure 21. Typical connection diagram using the ADC



1. Refer to *Table 48: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

图 20. ADC 精度特性

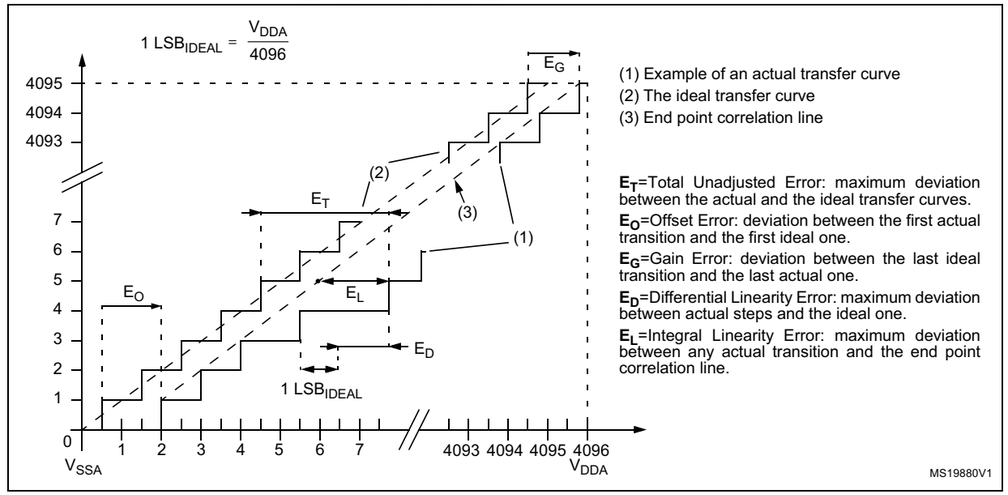
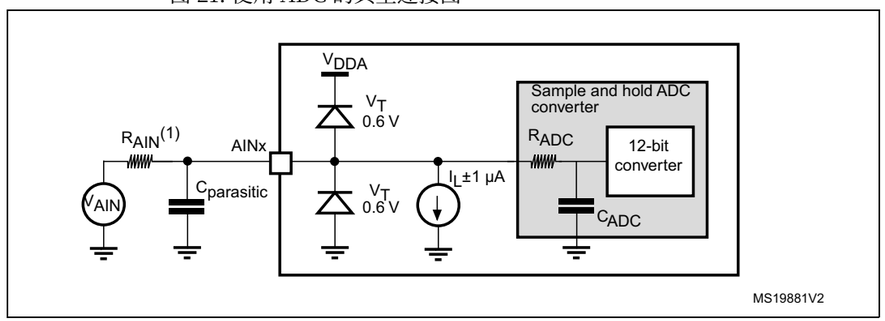


图 21. 使用 ADC 的典型连接图



1. 请参阅表 48：ADC 特性，了解 RAIN 、 RADC 和 CADC 的值。2。 Cparasitic 表示 PCB 的电容（取决于焊接和 PCB 布局质量）加上焊盘电容（大约 7 pF ）。高 Cparasitic 值会降低转换精度。为了解决这个问题，应该减少 fADC。

一般 PCB 设计指南

应按照图 10：电源方案所示执行电源去耦。 10 nF 电容器应该是陶瓷电容器（质量好），并且应尽可能靠近芯片放置。

6.3.17 Temperature sensor characteristics

Table 51. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	17.1	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.18 Timer characteristics

The parameters given in *Table 52* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 52. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx	-	16	bit
$t_{COUNTER}$	16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter		-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	s

1. TIMx is used as a general term to refer to the TIM1, TIM3, TIM6, TIM14, TIM15, TIM16 and TIM17 timers.

6.3.17 温度传感器特性

表 51. TS 特性

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	17.1	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.18 定时器特性

表 52 中给出的参数由设计保证。

有关输入 / 输出复用功能特性（输出比较、输入捕捉、外部时钟、 PWM 输出）的详细信息，请参阅第 6.3.14 节：I/O 端口特性。

表 52. TIMx(1) 特性

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx	-	16	bit
$t_{COUNTER}$	16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter		-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	s

1. TIMx is used as a general term to refer to the TIM1, TIM3, TIM6, TIM14, TIM15, TIM16 and TIM17 timers.

Table 53. IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 54. WWDG min-max timeout value @48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

表 53. 40 kHz 时的 IWDG 最小 / 最大超时周期 (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

表 54. WWDG 最小 - 最大超时值 @48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.19 Communication interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 55*. Refer also to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 55. I2C characteristics(1)

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4		0.6		0.26	-	µs
tr	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
tf	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26		µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF

1. The I2C characteristics are the requirements from the I2C bus specification rev03. They are guaranteed by design when the I2Cx_TIMING register is correctly programmed (refer to reference manual). These characteristics are not tested in production.
2. The maximum $t_{HD;DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.

6.3.19 通讯接口

I²C 接口特性

I²C 接口满足标准 I²C 通信协议的要求，但具有以下限制：映射的 I/O 引脚 SDA 和 SCL 不是 “ 真正的 ” 开漏。当配置为开漏时，连接在 I/O 引脚和 VDD 之间的 PMOS 被禁用，但仍然存在。

I²C 特性如表 55 所示。有关输入 / 输出复用功能特性（ SDA 和 SCL ）的更多详细信息，另请参阅第 6.3.14 节：I/O 端口特性。

表 55. I2C 特性 (1)

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4		0.6		0.26	-	µs
tr	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
tf	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26		µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF

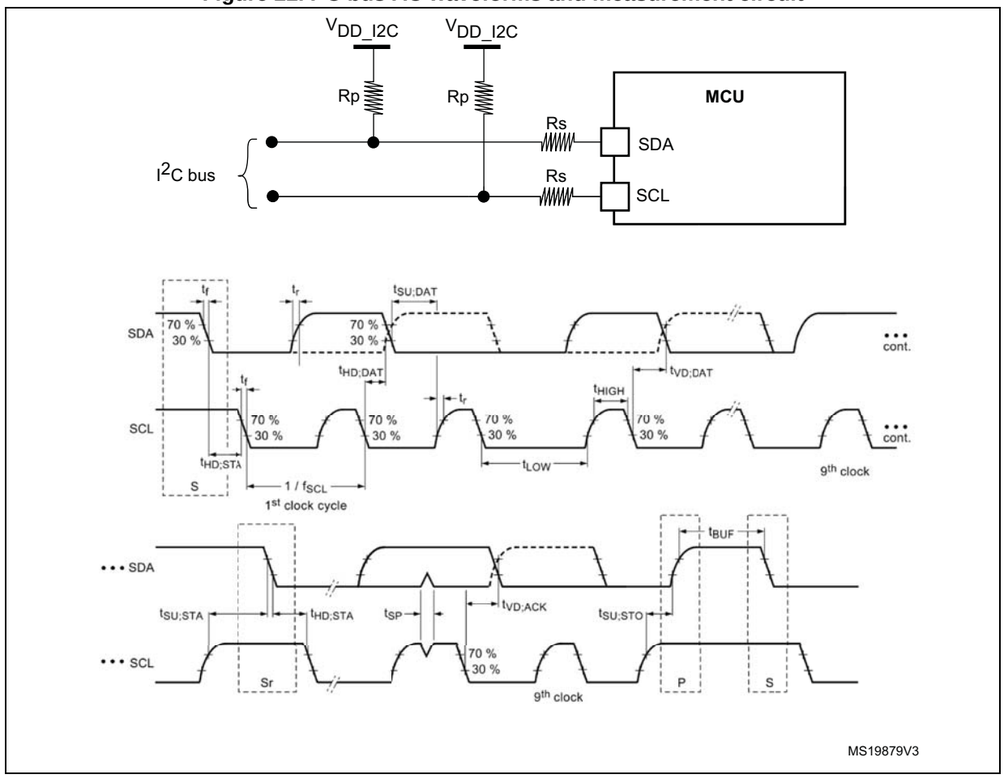
1. The I2C characteristics are the requirements from the I2C bus specification rev03. They are guaranteed by design when the I2Cx_TIMING register is correctly programmed (refer to reference manual). These characteristics are not tested in production.
2. The maximum $t_{HD;DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.

Table 56. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 22. I²C bus AC waveforms and measurement circuit



Legend: Rs: Series protection resistors. Rp: Pull-up resistors. V_{DD_I2C}: I²C bus supply.

SPI characteristics

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 18: General operating conditions*.

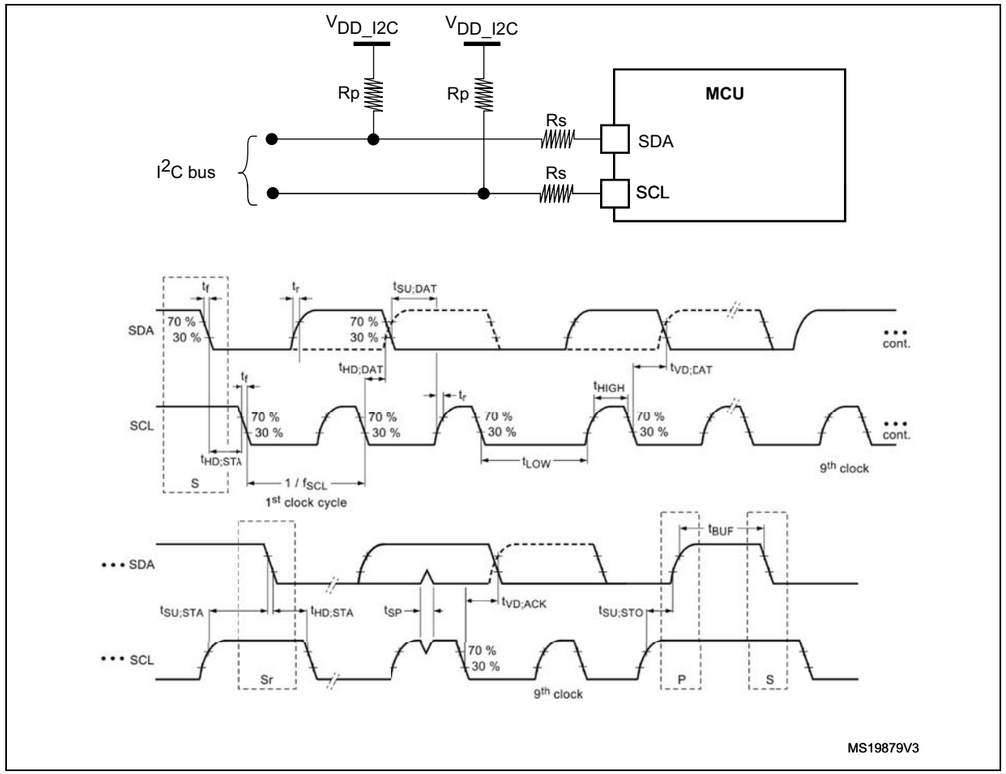
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK).

表 56. I2C 模拟滤波器特性 (1)

Symbol	Parameter	Min	Max	Unit
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

图 22. I²C 总线交流波形和测量电路



图注： Rs：串联保护电阻。 Rp：上拉电阻。 VDD_I2C：I2C 总线电源 .

SPI 特性

除非另有说明，表 57 中给出的参数源自在表 18：一般工作条件中总结的环境温度、fPCLKx 频率和 VDD 电源电压条件下执行的测试。

有关输入 / 输出复用功能特性（ SPI 的 NSS 、 SCK 、 MOSI 、 MISO 和 WS 、 CK ）的更多详细信息，请参阅第 6.3.14 节：I/O 端口特性。

Table 57. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	4	-	
$t_{h(SI)}$ (1)		Slave mode	5	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

表 57. SPI 特性

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	4	-	
$t_{h(SI)}$ (1)		Slave mode	5	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 23. SPI timing diagram - slave mode and CPHA = 0

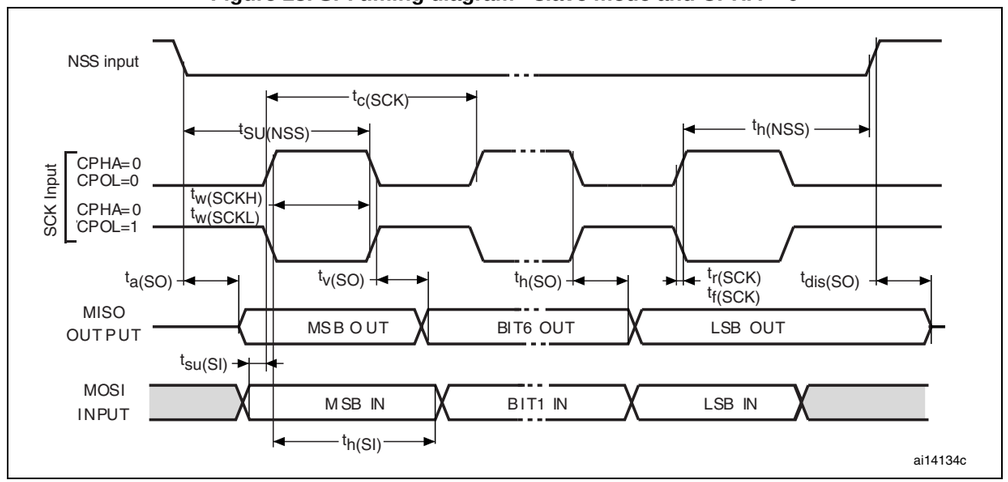
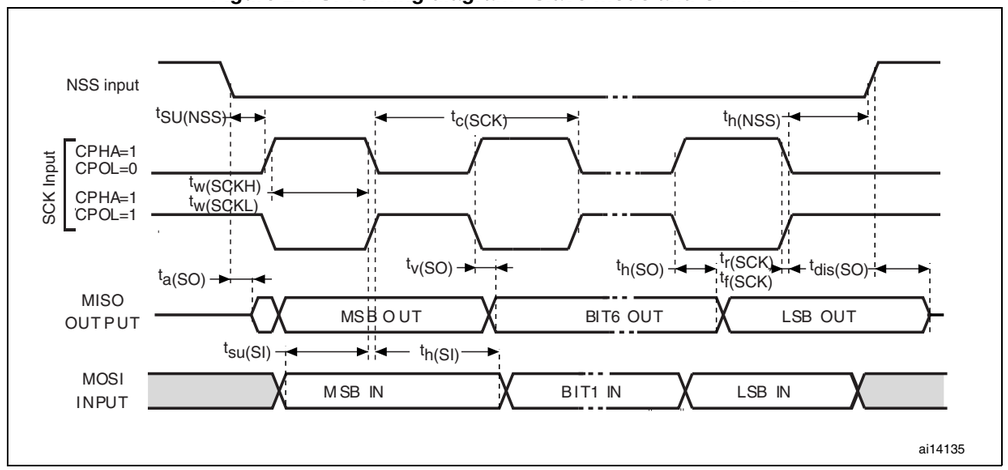


Figure 24. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

图 23. SPI 时序图 - 从机模式和 CPHA **= 0**

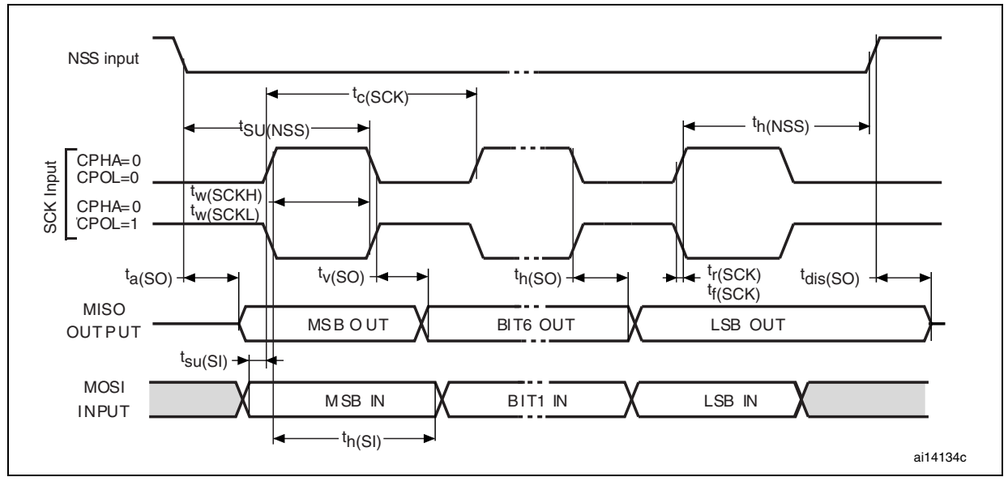
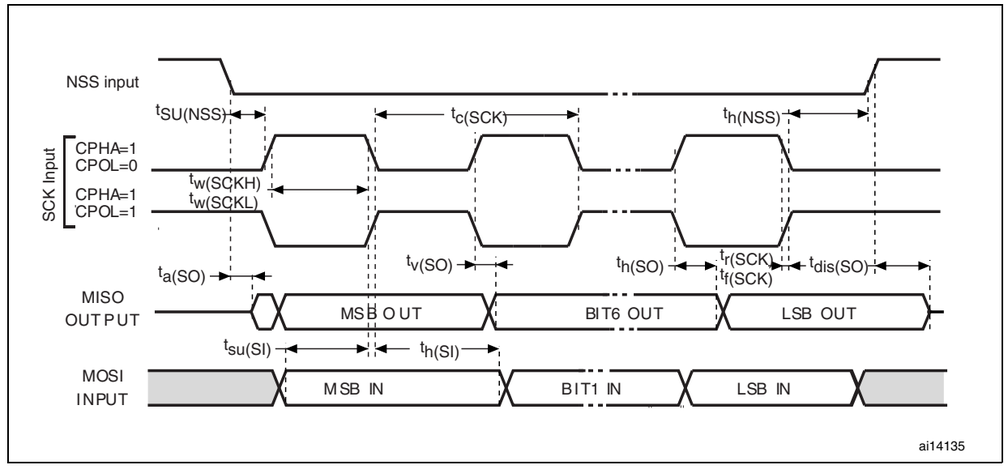
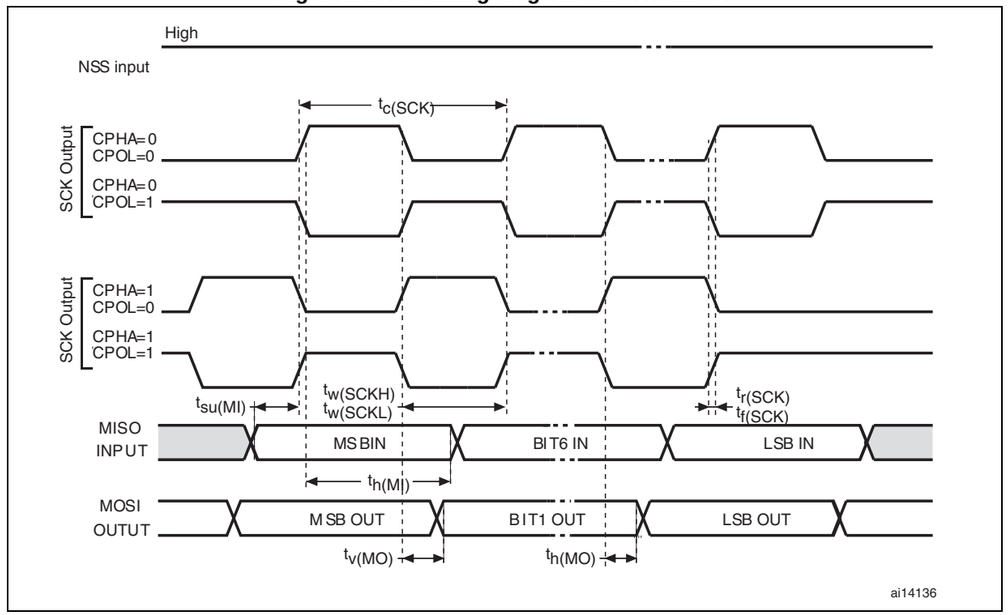


图 24. SPI 时序图 - 从机模式和 CPHA **= 1**



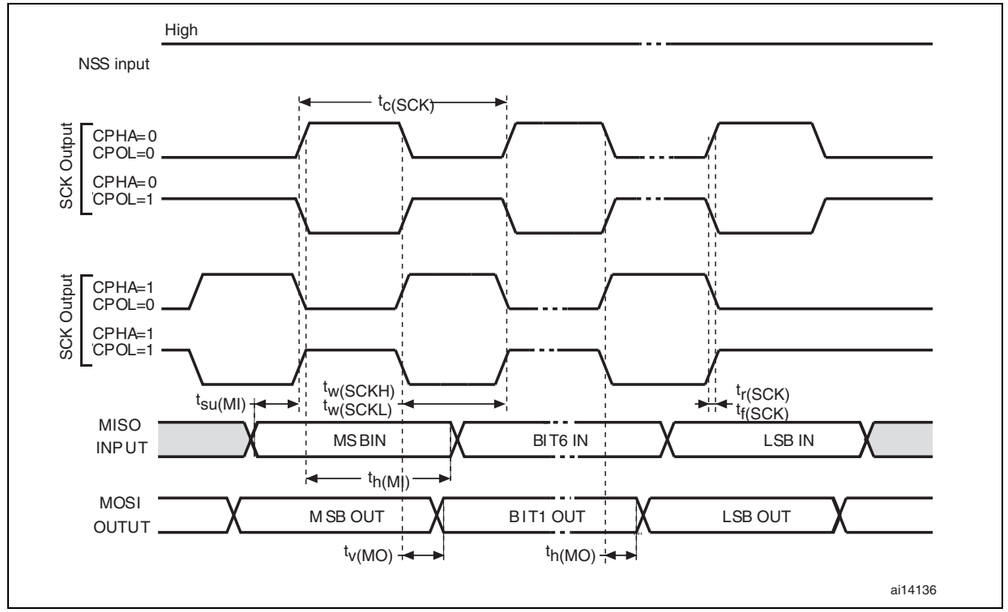
1. 测量点在 CMOS 电平上完成：$0.3V_{DD}$ 和 $0.7V_{DD}$。

Figure 25. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

图 25. SPI 时序图 - 主模式



1. 测量点在 CMOS 电平上完成：$0.3V_{DD}$ 和 $0.7V_{DD}$。

7 Package characteristics

7.1 Package mechanical data

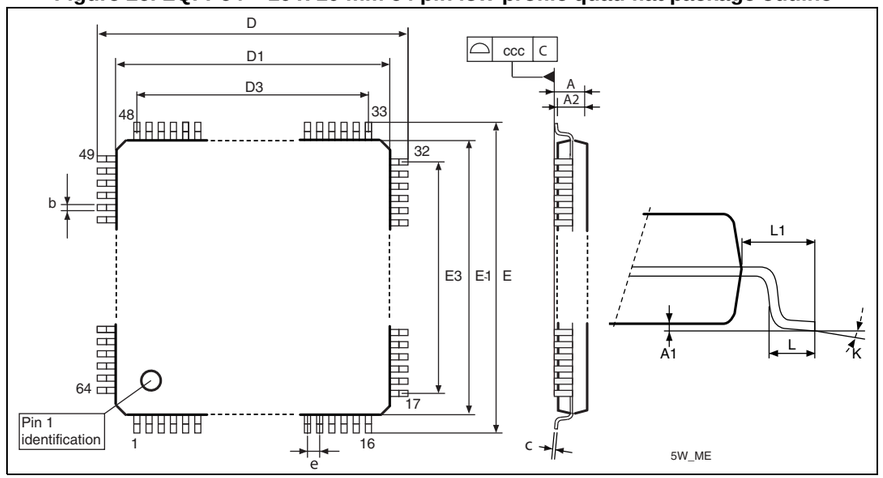
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7 封装特性

7.1 封装机械数据

为了满足环境要求，意法半导体根据这些器件的环境合规级别，提供不同等级的 ECOPACK® 封装。 ECOPACK®规格、等级定义和产品状态可在以下网址获取：www.st.com。ECOPACK® 是 ST 商标。

Figure 26. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



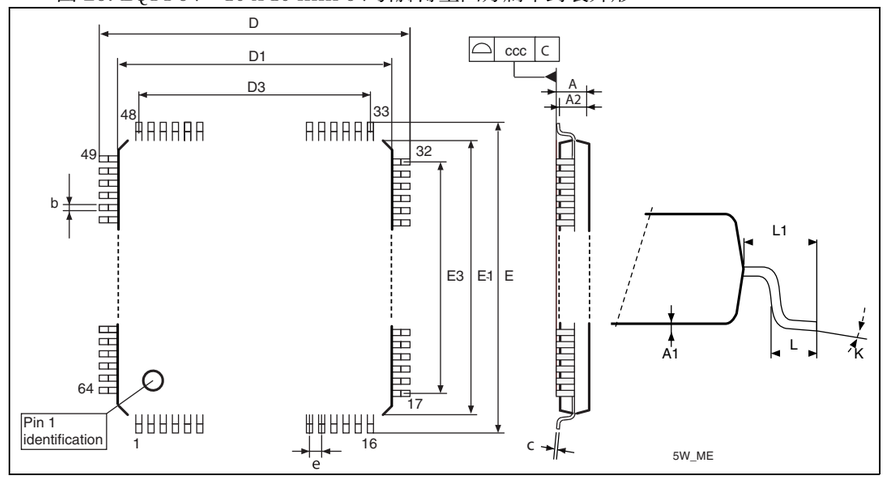
1. Drawing is not to scale.

Table 58. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D.		7.500				
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.00	10.200	0.3858	0.3937	0.4016
e		0.500			0.0197	
k	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.75	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

图 26. LQFP64 – 10 x 10 mm 64 引脚薄型四方扁平封装外形



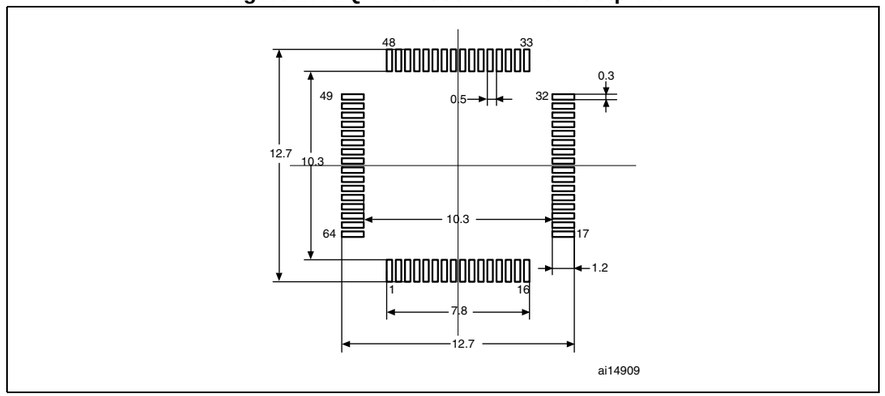
1. Drawing is not to scale.

Table 58. LQFP64 – 10 x 10 mm 64 引脚薄型四方扁平封装机械数据 **a**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D.		7.500				
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.00	10.200	0.3858	0.3937	0.4016
e		0.500			0.0197	
k	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.75	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc		0.080			0.0031	

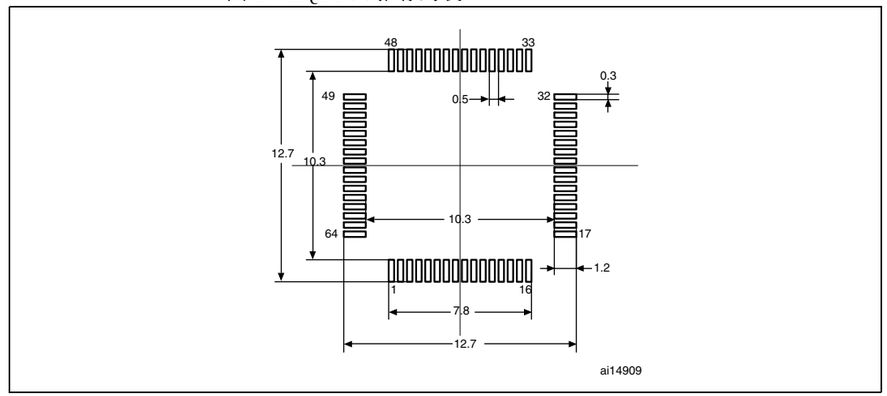
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. LQFP64 recommended footprint



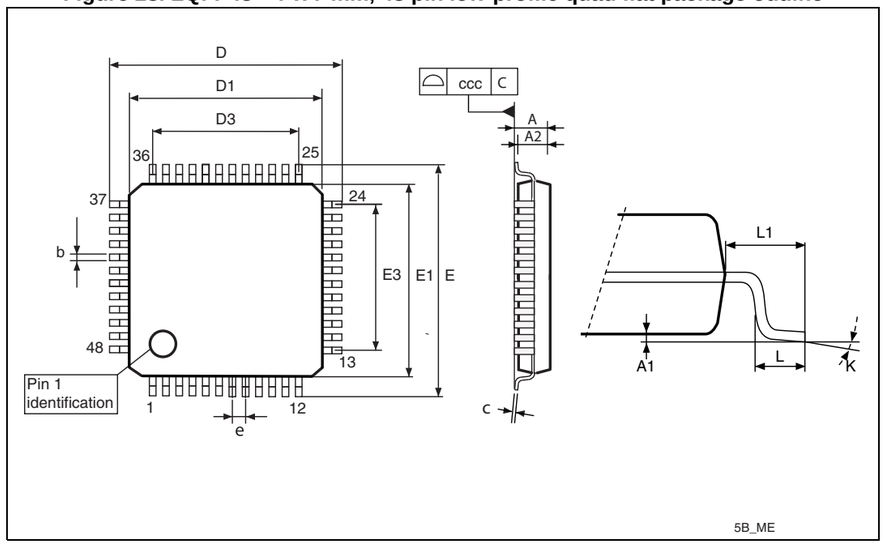
1. Drawing is not to scale.
2. Dimensions are in millimeters.

图 27. LQFP64 推荐封装



1. 绘图未按比例绘制。 2. 尺寸单位为毫米。

Figure 28. LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline



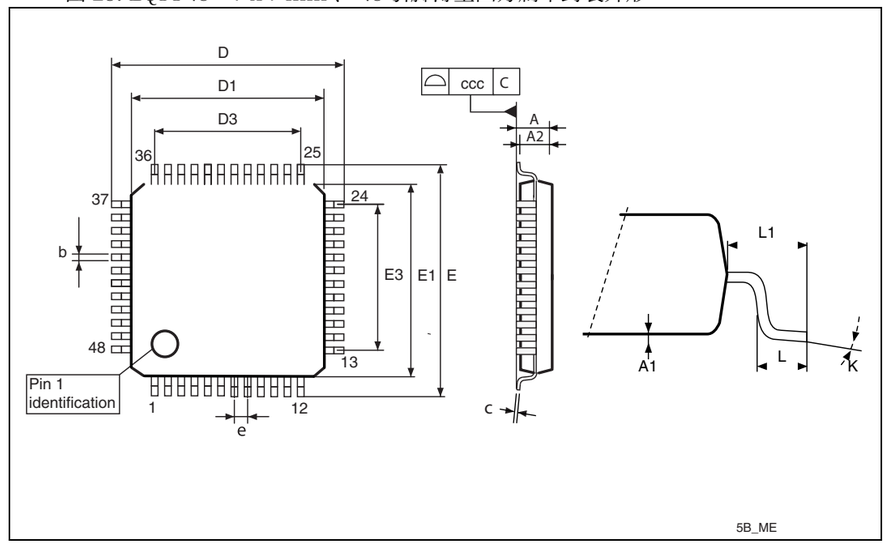
1. Drawing is not to scale.

Table 59. LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

图 28. LQFP48 – 7 x 7 mm、 48 引脚薄型四方扁平封装外形



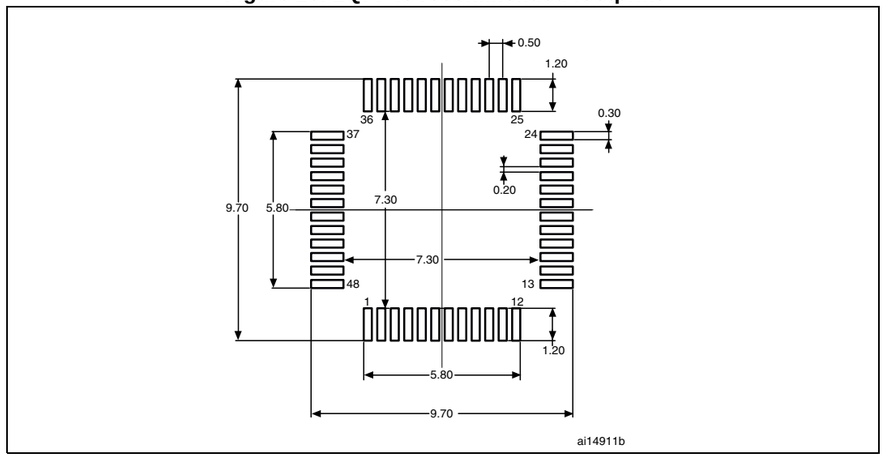
1. 绘图未按比例绘制。

表 59. LQFP48 – 7 x 7 mm、 48 引脚薄型四方扁平封装机械数据

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

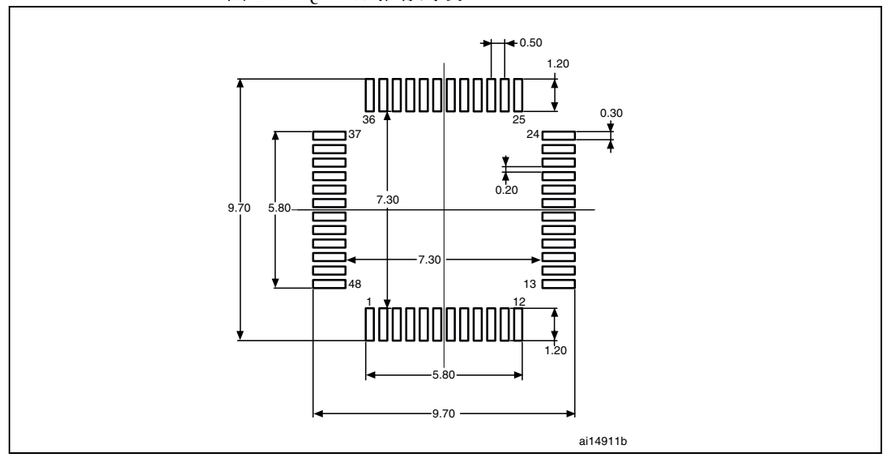
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 29. LQFP48 recommended footprint



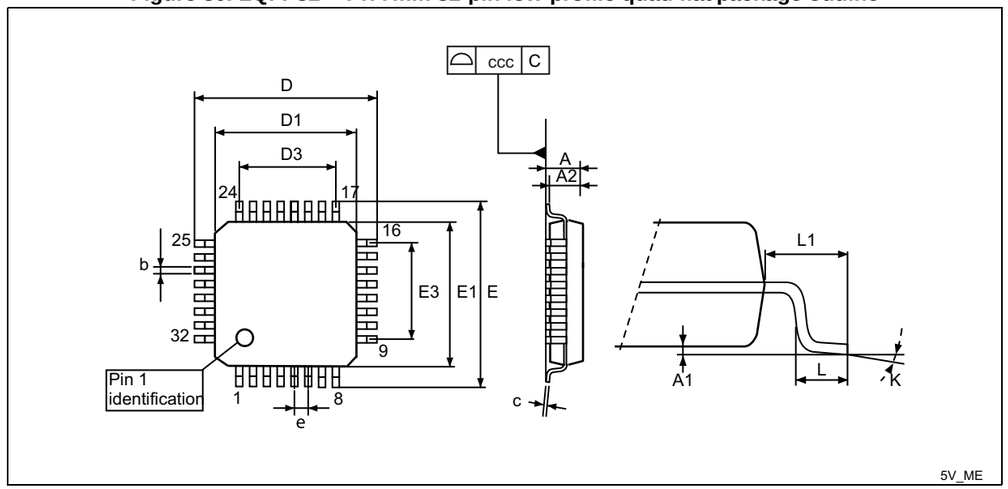
1. Drawing is not to scale.
2. Dimensions are in millimeters.

图 29. LQFP48 推荐封装



1. 绘图未按比例绘制。 2. 尺寸单位为毫米。

Figure 30. LQFP32 – 7 x 7mm 32-pin low-profile quad flat package outline



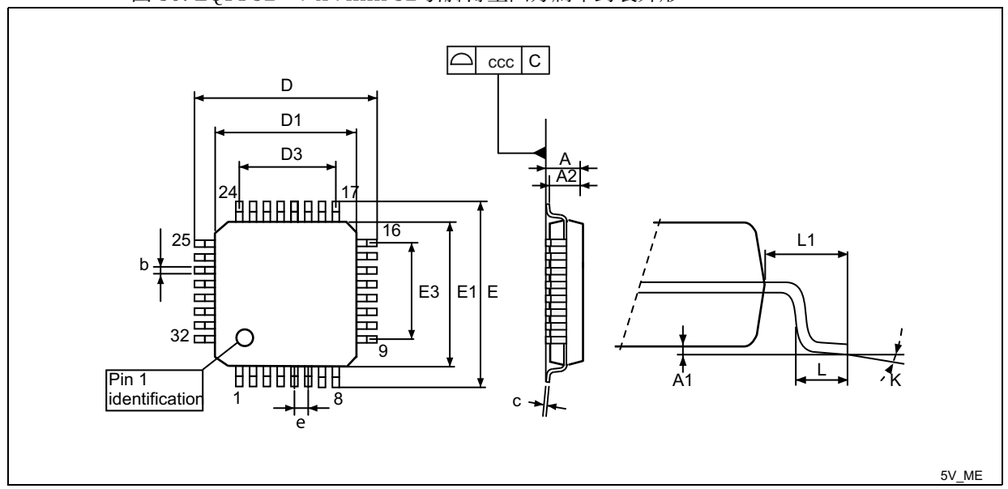
1. Drawing is not to scale.

Table 60. LQFP32 – 7 x 7mm 32-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.600			0.2205	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.600			0.2205	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc			0.100			0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

图 30. LQFP32 – 7 x 7mm 32 引脚薄型四方扁平封装外形



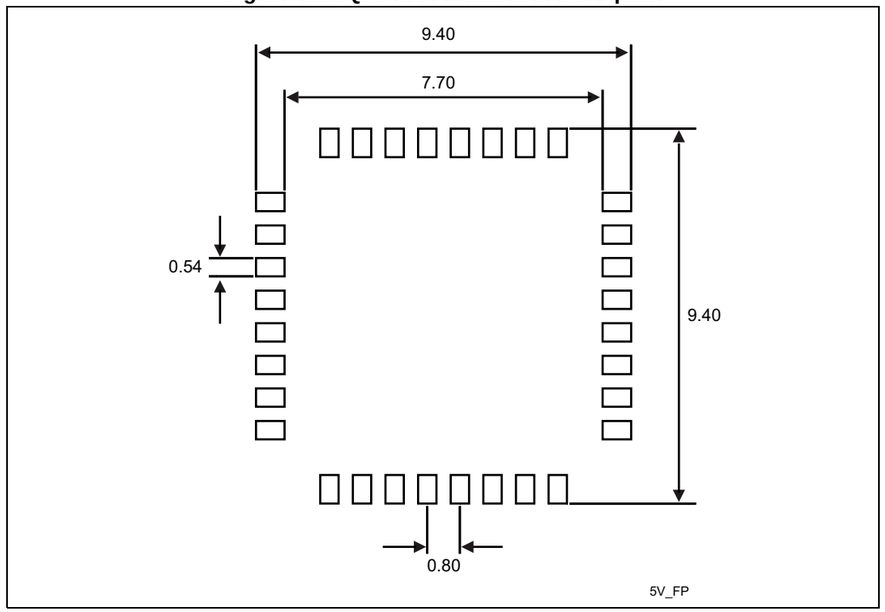
1. 绘图未按比例绘制。

表 60. LQFP32 – 7 x 7mm 32 引脚薄型四方扁平封装机械数据

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.600			0.2205	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.600			0.2205	
e		0.800			0.0315	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc			0.100			0.0039

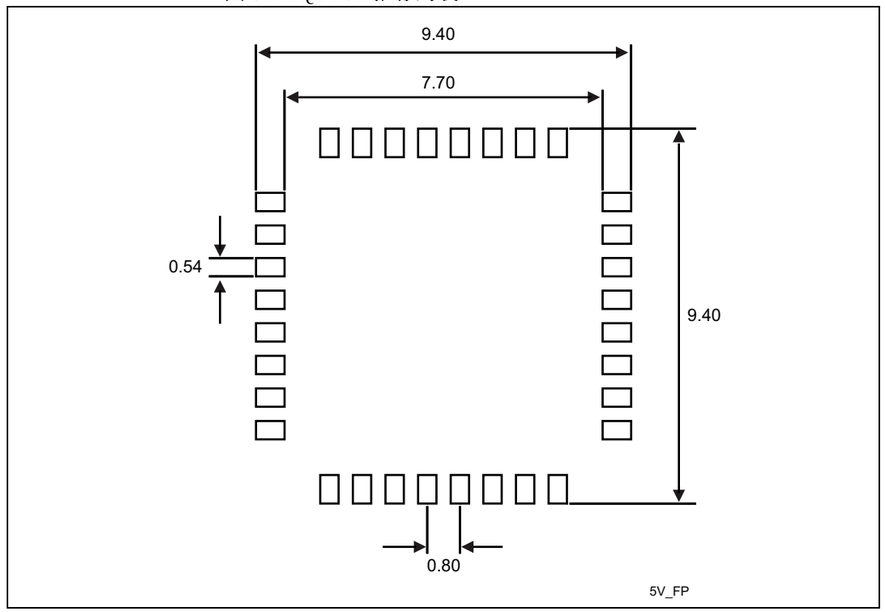
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 31. LQFP32 recommended footprint



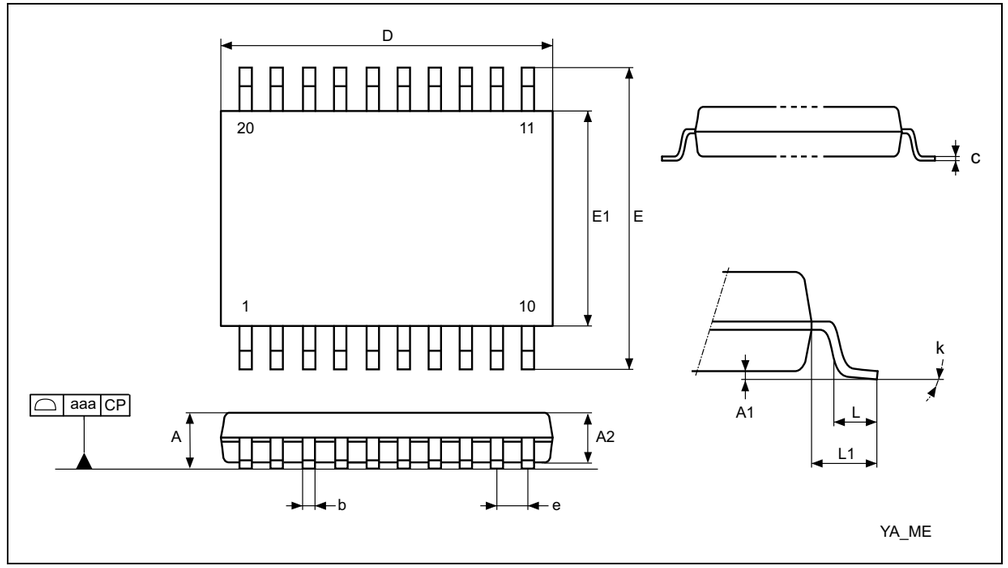
1. Drawing is not to scale.
2. Dimensions are in millimeters.

图 31. LQFP32 推荐封装



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Figure 32. TSSOP20 - 20-pin thin shrink small outline



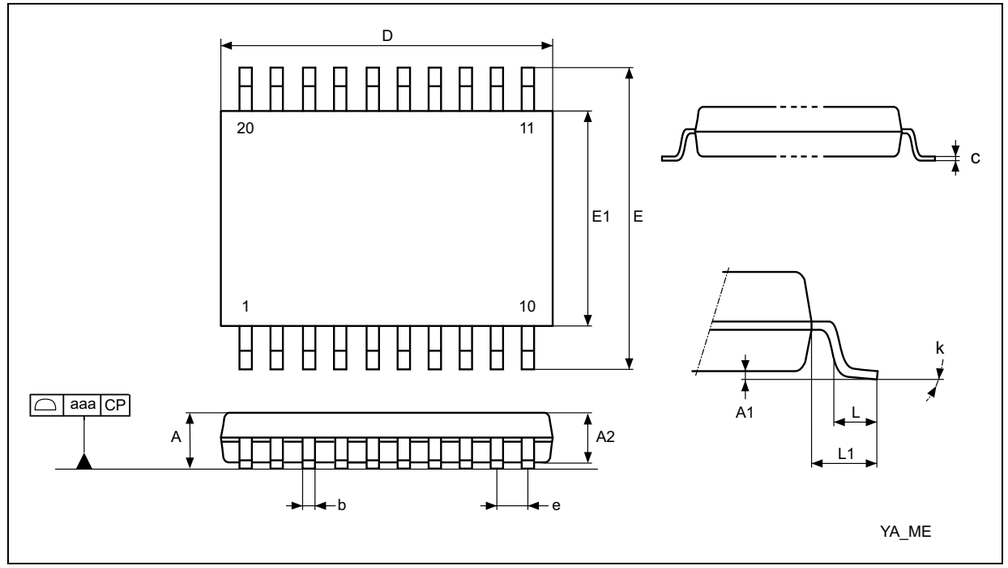
1. Drawing is not to scale.

Table 61. TSSOP20 – 20-pin thin shrink small outline package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	
A			1.2			0.0472
A1	0.05		0.15	0.002		0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19		0.3	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1	4.3	4.4	4.5	0.1693	0.1732	0.1772
e		0.65			0.0256	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0°		8.0°	0.0°		8.0°
aaa			0.1			0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

图 32. TSSOP20 - 20 引脚薄型收缩小外形



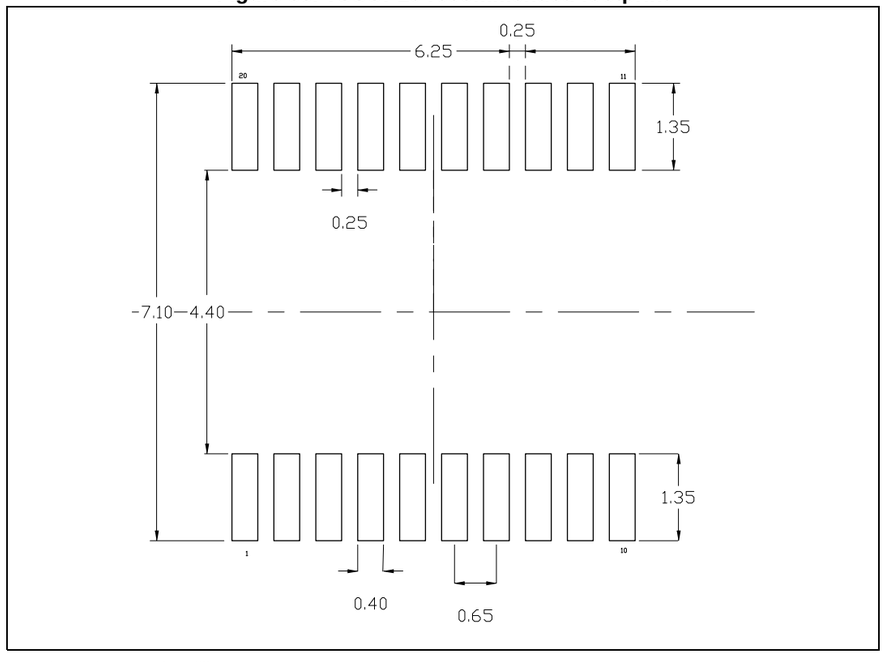
1. Drawing is not to scale.

表 61. TSSOP20 – 20 引脚薄型收缩小外形封装机械数据 a

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	
A			1.2			0.0472
A1	0.05		0.15	0.002		0.0059
A2	0.8	1	1.05	0.0315	0.0394	0.0413
b	0.19		0.3	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.2559	0.2598
E	6.2	6.4	6.6	0.2441	0.252	0.2598
E1	4.3	4.4	4.5	0.1693	0.1732	0.1772
e		0.65			0.0256	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0°		8.0°	0.0°		8.0°
aaa			0.1			0.0039

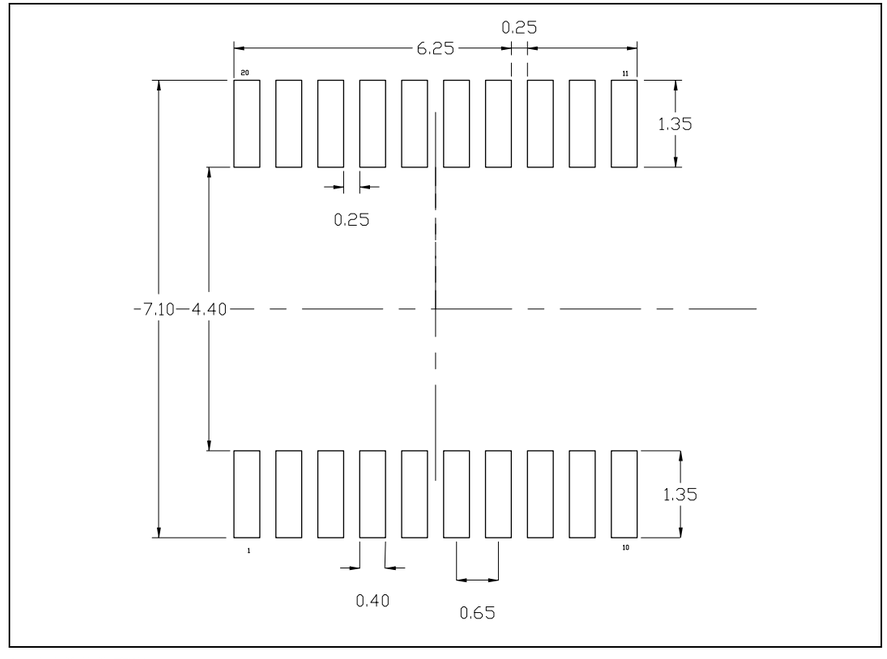
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. TSSOP20 recommended footprint



1. Dimensions are in millimeters

图 33. TSSOP20 推荐封装



1. 尺寸单位为毫米

7.2 Thermal characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 18: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 62. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP32 - 7 × 7 mm	56	
	Thermal resistance junction-ambient TSSOP20	110	

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F0xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

7.2 热特性

最大芯片结温 (TJ max) 不得超过表 18：一般工作条件中给出的值。

最大芯片结温 TJ max （以摄氏度为单位）可以使用以下公式计算：

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

在哪里：

- TA max 是最高环境温度，单位为 °C，
- ΘJA 是封装结点至环境热阻，单位为 °C/W，
- PD max 是 PINT max 和 PI/O max 之和（ PD max = PINT max + PI/Omax），
- PINT max 是 IDD 和 VDD 的乘积，以瓦特表示。这是芯片内部的最大功率。

PI/O max 表示输出引脚上的最大功耗，其中：

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

考虑应用中低电平和高电平 I/O 的实际 VOL / IOL 和 VOH / IOH。

表 62. 封装热特性

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP32 - 7 × 7 mm	56	
	Thermal resistance junction-ambient TSSOP20	110	

7.2.1 参考文件

JESD51-2 集成电路热测试方法环境条件 - 自然对流（静止空气）。可从 www.jedec.org 获取

7.2.2 选择产品温度范围

订购微控制器时，温度范围在第 8 节：部件编号中所示的订购信息方案中指定。

每个温度范围后缀对应于最大耗散时的特定保证环境温度以及特定的最大结温。

由于应用通常不会在最大功耗下使用 STM32F0xx，因此计算准确的功耗和结温以确定最适合应用的温度范围非常有用。

以下示例说明如何计算给定应用所需的温度范围。

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 62* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Table 18: General operating conditions*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 105-20.115 = 84.885 °C

Suffix 7: T_{Amax} = T_{Jmax} - (45°C/W × 447 mW) = 125-20.115 = 104.885 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 62* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6.03 °C = 106.03 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

示例 1：高性能应用

假设应用条件如下：

最高环境温度 TAmax = 82 °C（按 JESD51-2 测量），IDDmax = 50 mA，VDD = 3.5 V，低电平输出时最多同时使用 20 个 I/O，IOL = 8 mA，VOL= 0.4 V，低电平输出时最多同时使用 8 个 I/O 带 IOL = 20 mA，VOL= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

使用表 62 中获得的值，TJmax 计算如下：

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.115 °C = 102.115 °C

这在后缀 6 版本零件 (–40 < TJ < 105 °C) 的范围内，请参见表 18：一般操作条件。

在这种情况下，订购的部件必须至少带有温度范围后缀 6 （请参阅第 8 节：部件编号）。

笔记：通过给定的 PDmax，我们可以找到给定器件温度范围（订购代码后缀 6 或 7 ）允许的 TAmax。

后缀 6：TAmax = TJmax - (*45*°C/W × *447* mW) = *105*-20.*115* = *84.885* °C 后缀 7：TAmax = TJmax - (*45*°C/W × *447* mW) = *125*-20.*115* = *104.885* °C

实施例 2：高温应用

使用相同的规则，只要结温 TJ 保持在指定范围内，就可以解决在高环境温度下运行且功耗低的应用。

假设应用条件如下：

最高环境温度 TAmax = 100 °C（按 JESD51-2 测量），IDDmax = 20 mA，VDD = 3.5 V，低电平输出时最多同时使用 20 个 I/O，IOL = 8 mA，VOL= 0.4 V PINTmax = 20 mA × 3.5 V= 70 mW PIOmax = 20 × 8 mA × 0.4 V = 64 mW 由此得出：PINTmax = 70 mW 和 PIOmax = 64 mW：PDmax = 70 + 64 = 134 mW

因此：PDmax = 134 mW

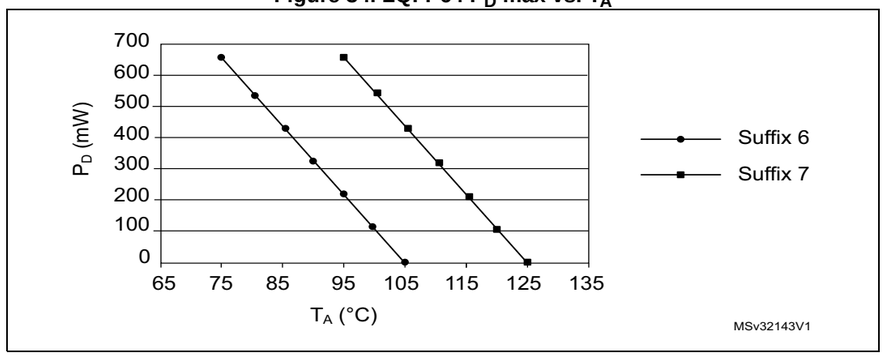
使用表 62 中获得的值，TJmax 计算如下： – 对于 LQFP64， 45 °C/W TJmax = 100 °C + (45 °C/W × 134 mW) = 100 °C + 6。03 °C = 106。03 °C

这超出了后缀 6 版本部件的范围 (–40 < TJ < 105 °C)。

在这种情况下，订购的部件必须至少具有温度范围后缀 7 （请参阅第 8 节：部件编号），除非我们降低功耗以便能够使用后缀 6 部件。

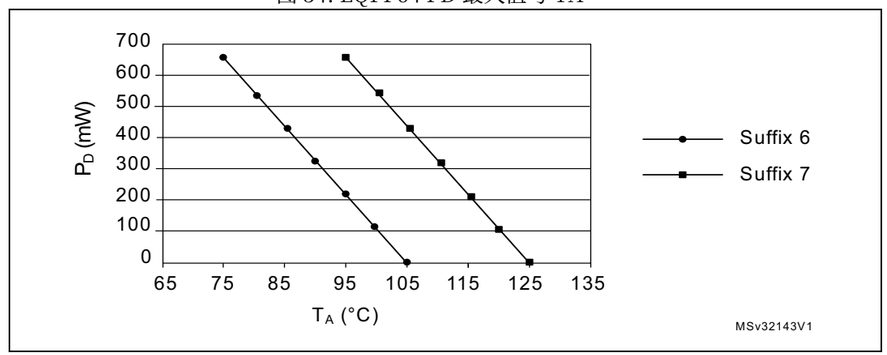
Refer to *Figure 34* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements. For suffix 7, refer to STM32F05x devices.

Figure 34. LQFP64 P_D max vs. T_A



请参阅图 34，根据您的环境温度或功率要求选择所需的温度范围（后缀 6 或 7）。对于后缀 7，请参阅 STM32F05x 器件。

图 34. LQFP64 PD 最大值与 TA



8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 63. Ordering information scheme

Example: STM32 F 030 R 8 T 6 x

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = General-purpose

Sub-family
030 = STM32F030xx

Pin count
F = 20 pins
K = 32 pins
C = 48 pins
R = 64 pins

Code size
4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory
8 = 64 Kbytes of Flash memory

Package
P = TSSOP
T = LQFP

Temperature range
6 = –40 °C to +85 °C

Options
TR = tape and real

8 零件编号

如需可用选项列表（内存、封装等）或有关该器件任何方面的更多信息，请联系离您最近的 ST 销售办事处。

Table 63. Ordering information scheme

Example: STM32 F 030 R 8 T 6 x

Device family
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8 = 64 Kbytes of Flash memory

Package
P = TSSOP
T = LQFP

Temperature range
6 = –40 °C to +85 °C

Options
TR = tape and real

9 Revision history

Table 64. Document revision history

Date	Revision	Changes
04-Jul-2013	1	Initial release

9 修订历史

表 64. 文档修订历史记录

Date	Revision	Changes
04-Jul-2013	1	Initial release

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