1. Description

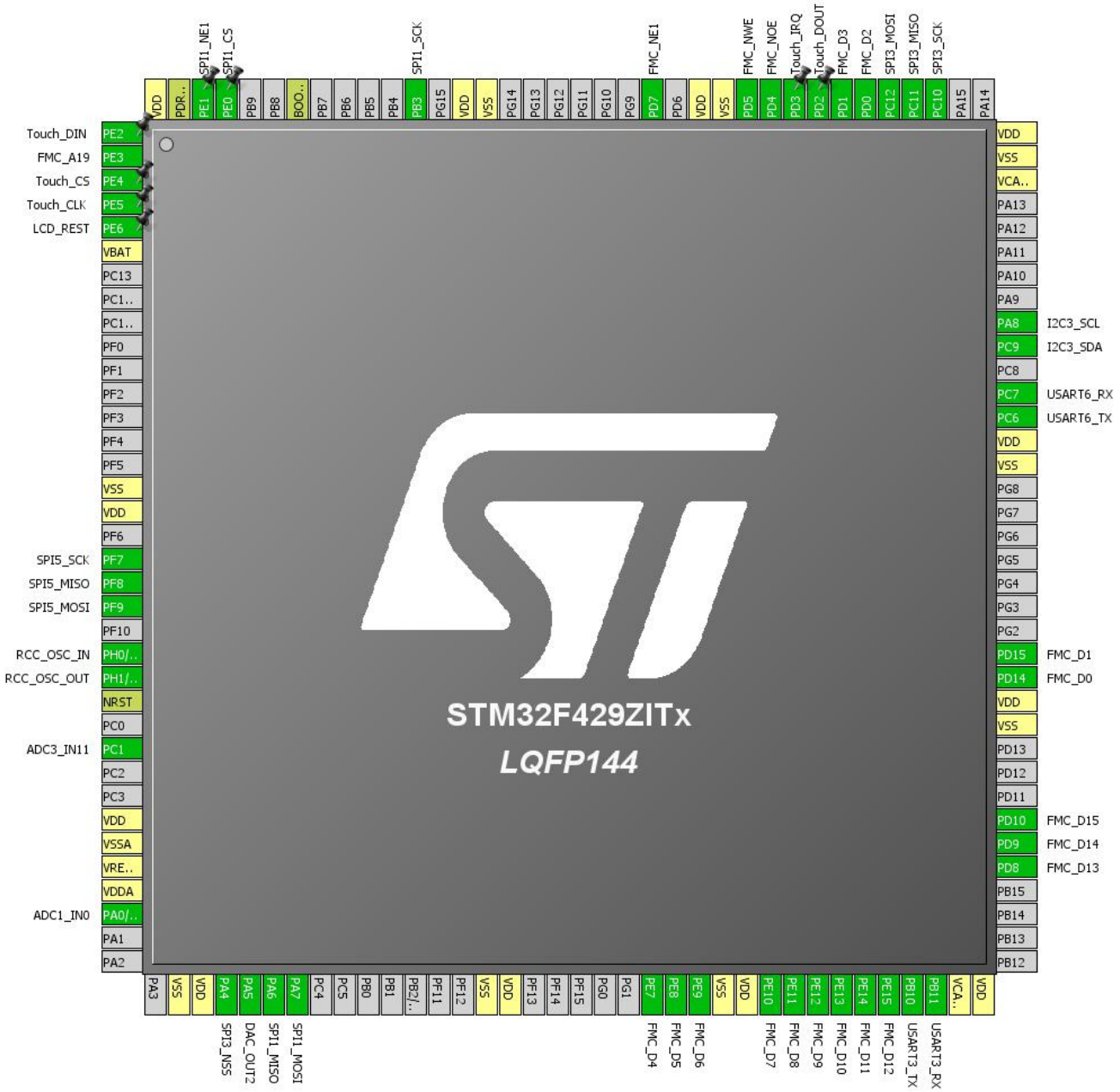
1.1. Project

Project Name	OSC_STM32F429Discovery
Board Name	STM32F429I-DISCO
Generated with:	STM32CubeMX 4.15.0
Date	06/05/2016

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

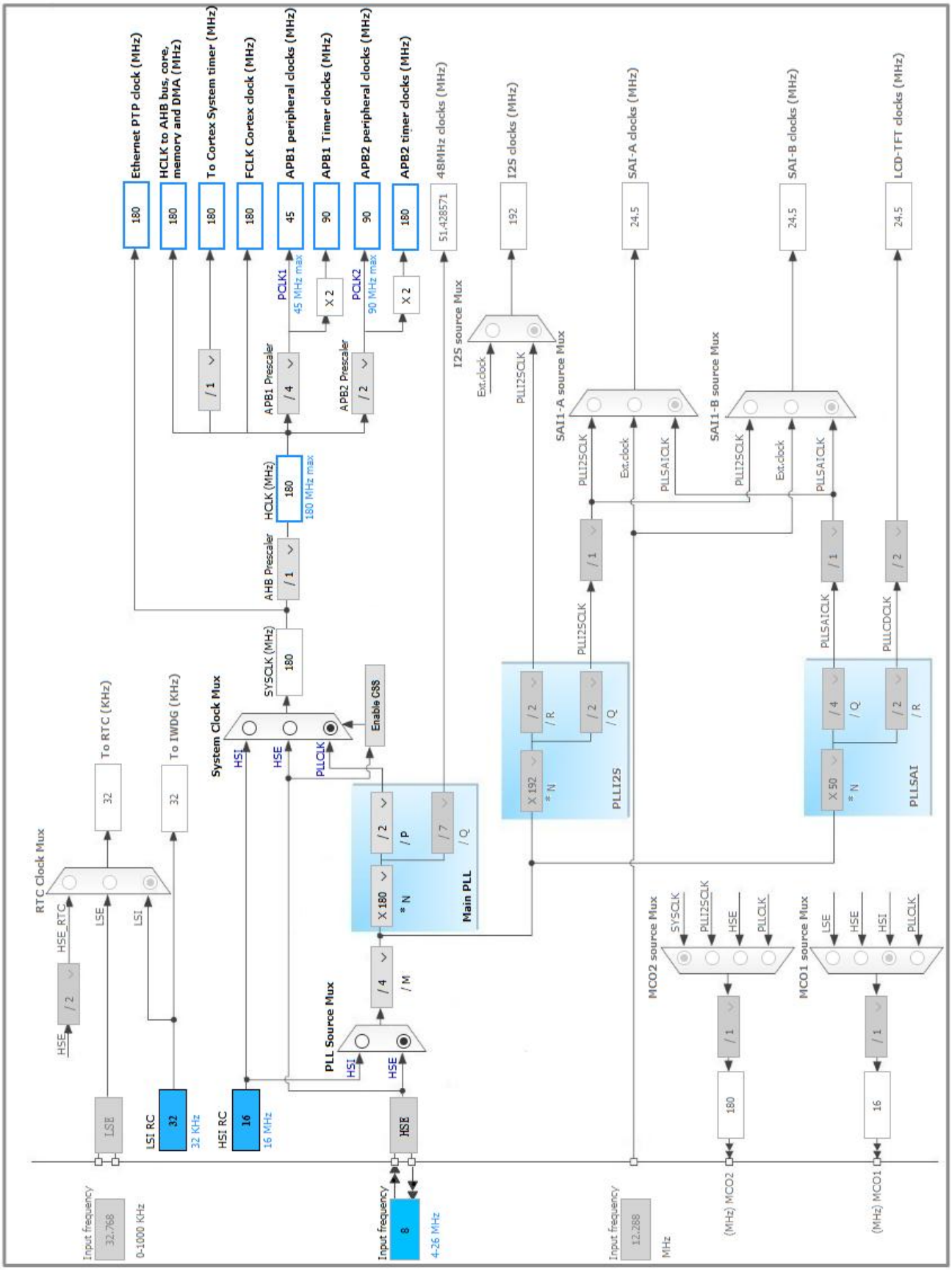
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	Touch_DIN
2	PE3	I/O	FMC_A19	
3	PE4 *	I/O	GPIO_Output	Touch_CS
4	PE5 *	I/O	GPIO_Output	Touch_CLK
5	PE6 *	I/O	GPIO_Output	LCD_REST
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	SPI5_SCK	
20	PF8	I/O	SPI5_MISO	
21	PF9	I/O	SPI5_MOSI	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ADC3_IN11	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	ADC1_IN0	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	SPI3_NSS	
41	PA5	I/O	DAC_OUT2	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	SPI1_MOSI	
51	VSS	Power		
52	VDD	Power		
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	USART3_TX	
70	PB11	I/O	USART3_RX	
71	VCAP_1	Power		
72	VDD	Power		
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	USART6_TX	
97	PC7	I/O	USART6_RX	
99	PC9	I/O	I2C3_SDA	
100	PA8	I/O	I2C3_SCL	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
111	PC10	I/O	SPI3_SCK	
112	PC11	I/O	SPI3_MISO	
113	PC12	I/O	SPI3_MOSI	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
116	PD2 *	I/O	GPIO_Input	Touch_DOUT
117	PD3 *	I/O	GPIO_Input	Touch_IRQ
118	PD4	I/O	FMC_NOE	
119	PD5	I/O	FMC_NWE	
120	VSS	Power		
121	VDD	Power		
123	PD7	I/O	FMC_NE1	
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SPI1_SCK	
138	BOOT0	Boot		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
141	PE0 *	I/O	GPIO_Output	SPI1_CS
142	PE1 *	I/O	GPIO_Output	SPI1_NE1
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC3

mode: IN11

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 11
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. CRC

mode: Activated

5.4. DAC

mode: OUT2 Configuration

5.4.1. Parameter Settings:

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

5.5. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: LCD Interface
LCD Register Select: A19
Data: 16 bits

5.5.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 1
Write operation	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**4 ***
Data setup time in HCLK clock cycles	**45 ***
Bus turn around time in HCLK clock cycles	**0 ***

5.6. I2C3

I2C: I2C

5.6.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.7.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

5.8. SPI1

Mode: Full-Duplex Master

5.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**45.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.9. SPI3

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.9.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**22.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

5.10. SPI5

Mode: Full-Duplex Master

5.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**45.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.11. SYS

Timebase Source: SysTick

5.12. USART3

Mode: Asynchronous

5.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.13. USART6

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC1	ADC3_IN11	Analog mode	No pull-up and no pull-down	n/a	
DAC	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	
FMC	PE3	FMC_A19	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI3	PA4	SPI3_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USART3	PB10	USART3_TX	Alternate Function Push Pull	Pull-up	Very High *	
	PB11	USART3_RX	Alternate Function Push Pull	Pull-up	Very High *	
USART6	PC6	USART6_TX	Alternate Function Push Pull	Pull-up	Very High *	
	PC7	USART6_RX	Alternate Function Push Pull	Pull-up	Very High *	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	Touch_DIN
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	Touch_CS
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	Touch_CLK
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	LCD_REST
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Touch_DOUT
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Touch_IRQ
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_CS
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_NE1

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_RX	DMA2_Stream0	Peripheral To Memory	**High ***
SPI1_TX	DMA2_Stream3	Memory To Peripheral	**High ***
ADC3	DMA2_Stream1	Peripheral To Memory	**High ***

SPI1_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC3: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream1 global interrupt	true	0	0
DMA2 stream3 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
SPI1 global interrupt	unused		
USART3 global interrupt	unused		
SPI3 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
SPI5 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	024030_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	OSC_STM32F429Discovery
Project Folder	D:\Documents\workspace\stm32\OSC_STM32F429Discovery
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.12.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No