BHAGATH SINGH CHEELA

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EDUCATION

University of Pennsylvania, School of Engineering and Applied Science | Philadelphia, PA **12/22**
Master of Science in Electrical & Systems Engineering (ESE) GPA: 3.68/4.00
Selected courses: System on Chip Design, Computer Organization and Design, Hardware Software Co-design for Machine Learning, Applied Machine Learning, IoT and Edge Computing

Manipal University, Manipal Institute of Technology | Manipal, India **06/13 - 06/17**
Bachelor of Technology in Electronics & Communication Engineering GPA: 3.63/4.00

SKILLS

C, C++, Python, OpenCL, Verilog, Linux, Github, VS Code, Microsoft Office Suite, LaTex, PCB Design, RTL, Power Management

PROFESSIONAL EXPERIENCE

Varex Imaging Corporation, *R&D Software & FPGA Intern* | Salt Lake City, UT **05/22 – Present**
- Developing the software flow to integrate HLS and RTL code using Vitis HLS to speed up the design process
- Automating the build and verification test with a commit push to gerrit repository using Jenkins and Python scripting

University of Pennsylvania, *Graduate Research Assistant* | Philadelphia, PA **05/21 – 05/22**
- Demonstrated hardware acceleration of Economic computations using Vitis HLS on AWS F1 instance
- Performed multi-axes design space exploration and achieved x120 speedup compared to single core CPU and
- Constructed a modular host code that can make use of up to 8 FPGAs on AWS F1.16x instance using OpenCL API
- Presenting a research paper titled “Programming FPGAs for Economics” in Big Data & HPC Computing 2022

University of Pennsylvania, *Graduate Lab Leader* | Philadelphia, PA **01/21 – 04/22**
- Drafted the lab course using Node MCU and Raspberry Pi for an undergraduate class of 80 students - “Silicon Garage”
- Perfected the lab course curriculum for several undergraduate courses with more than 200 students
- Taught 6 lectures to a class of 29 students for ESE292 – Electromechanical Prototyping

Bharat Electronics Limited, *Deputy Engineer* | Bangalore, India **10/17 –12/20**
- Spearheaded the hardware design team to develop customized tablets for Indian government
- Designed high speed PCBs consisting of HDMI, USB communication lines and performed signal integrity analysis.
- Co-ordinated with the Mechanical, Marketing and external customers to realize the product within 8 months
- Set up manufacturing test process using ATE’s to speed up the testing process and reduced the testing time by 2x

PROJECTS

LC4 Processor Design using Xilinx Zynq -7000 SoC **01/22 – 05/22**
- Implemented a 5 staged pipelined, superscalar LC4 processor using Verilog in Xilinx Zynq 7000 SoC
- Performed bypassing to handle the data hazards, optimized the pipelines to close the timing requirement at 66 MHz

Deduplication and Compression using Xilinx Zynq MPSoC **09/21 – 12/21**
- Developed a compressor to receive data in real time and compress into memory using deduplication and compression
- Implemented a 5-stage pipeline for deduplication to run on the multiple ARM CPU cores using NEON intrinsics
- Accelerated the compression algorithm and achieved a throughput of 48 Mbps using on-chip FPGA

Hardware Accelerator for Machine Learning using FPGAs **01/21 – 05/21**
- Devised an FPGA-accelerated convolutional layer for accelerating DCNN using AWS F1 instance
- Integrated the kernel into Pytorch using C++ extensions and built the host code using OpenCL API
- Explored the design space using multiple kernels and out of order queue techniques to achieve comparable speed up with single core CPU

Automated Optical Inspection for PCB’s using Machine Learning **01/21 – 05/21**
- Developed a method to identify missing components on a PCB using Machine Learning and accomplished an accuracy of 86%
- Fine-tuned the features and evaluated the performance on various CNNs including ResNet, VGG and Inceptionv3

LEADERSHIP

Penn Technograds, *Co-President* |Philadelphia, PA **01/21 – Present**
- Hosted technical workshops on PCB Design, 3D prototyping for masters’ students in UPenn
- Organized key social events and hackathons by coordination with different student bodies to invite hundreds of students

ACHIEVEMENTS

- Recipient of SEAS Departmental grant for ESE *Graduate Lab Leader* with 50% tuition support
- Young presenter in “IEEE Aerospace Conference, Big Sky, MT”